

# Processors, FPGAs, and ASICs

## Part 1: Full Custom to PLDs

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# Spectrum of IC choices

**Flexible, efficient**

**You choose**



Full Custom

Polygons (Intel)

ASIC

Circuit (Sony)

Gate Array

Wires

FPGA

Logic network

PLD

Logic function

GP Processor

Program (e.g., ARM)

SP Processor

Program (e.g., DSP)

Multifunction

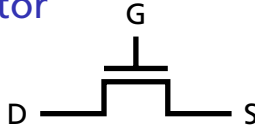
Settings (e.g., Ethernet Ctrl.)

Fixed-function

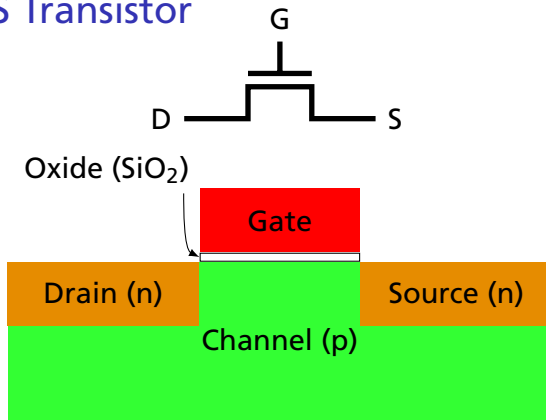
Part number (e.g., 74HCT00)

**Cheap, quick to design**

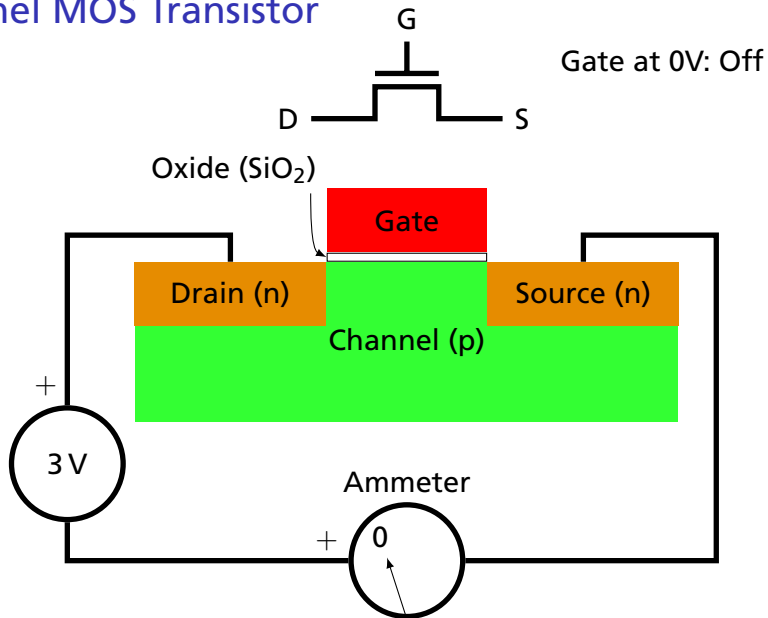
## An N-Channel MOS Transistor



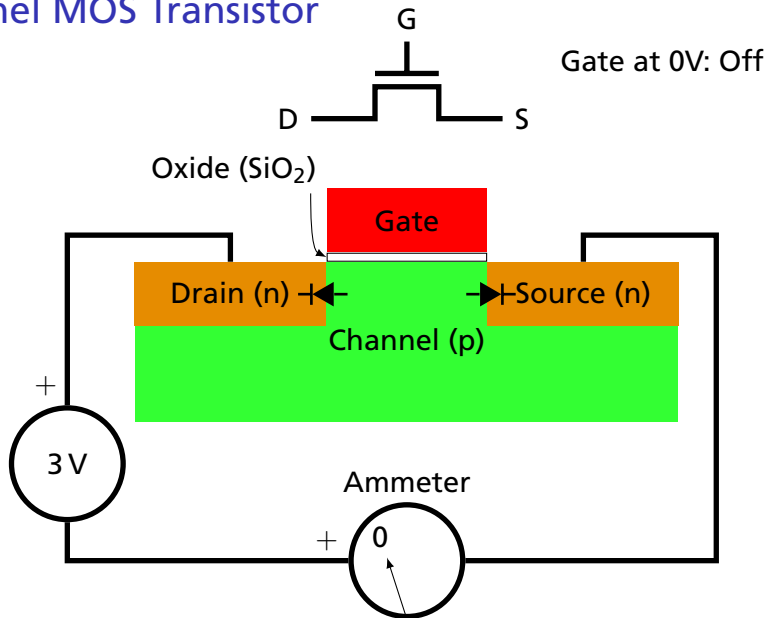
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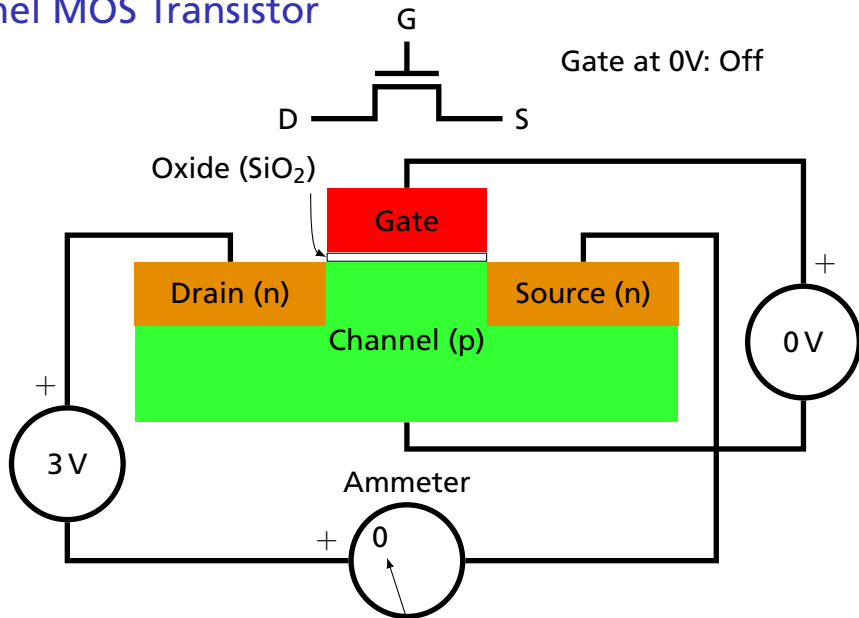
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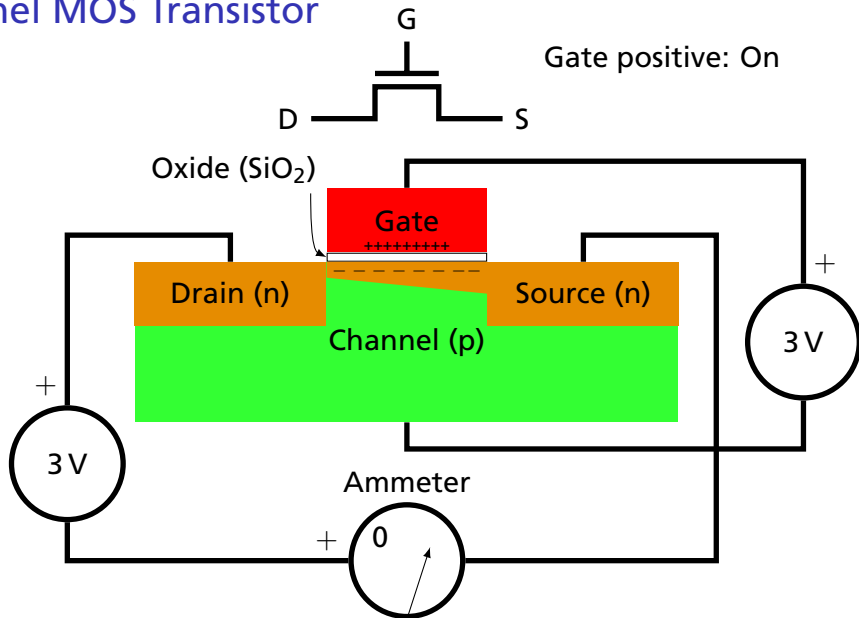
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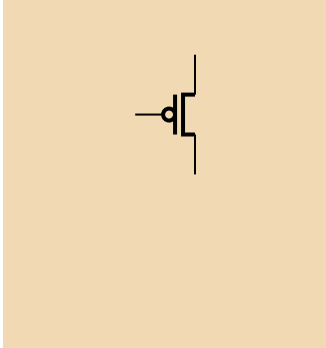


# An N-Channel MOS Transistor

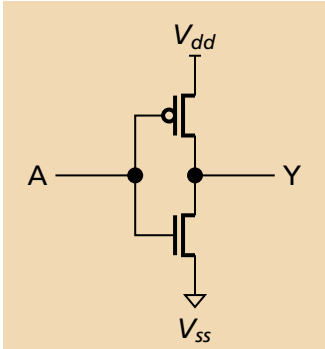




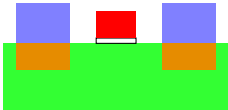
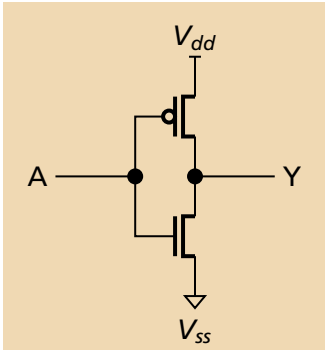
# CMOS Inverter Layout



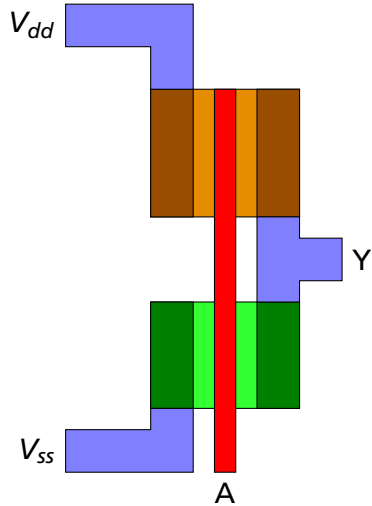
# CMOS Inverter Layout



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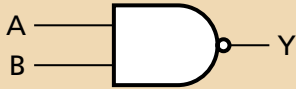


Cross Section Through N-channel FET



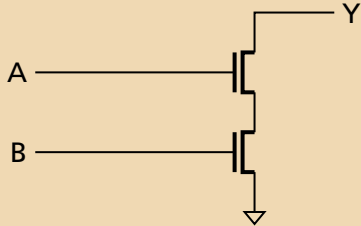
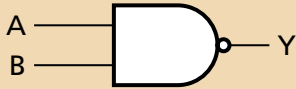
Top View

# The CMOS NAND Gate



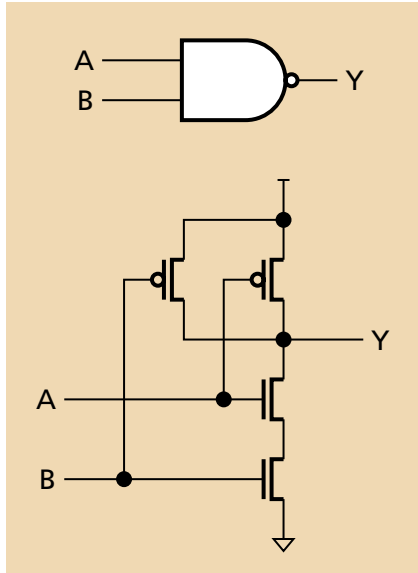
Two-input NAND gate:

# The CMOS NAND Gate



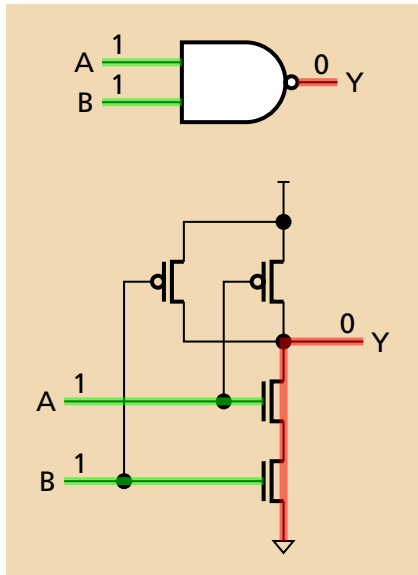
Two-input NAND gate:  
two n-FETs in series;

# The CMOS NAND Gate



Two-input NAND gate:  
two n-FETs in series;  
two p-FETs in parallel

# The CMOS NAND Gate



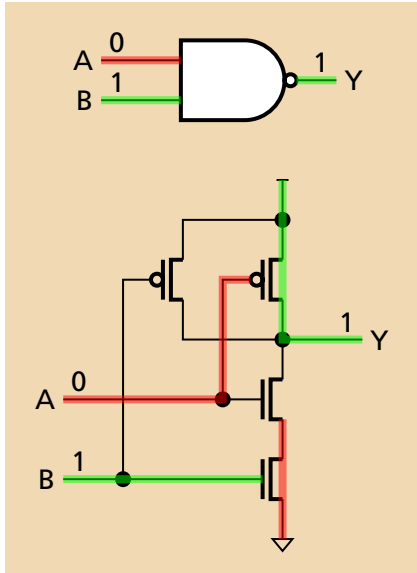
Both inputs 1:

Both n-FETs turned on

Output pulled low

Both p-FETs turned off

# The CMOS NAND Gate



One input 1, the other 0:

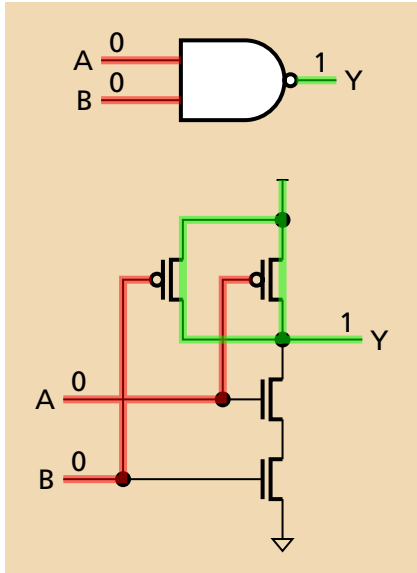
One p-FET turned on

Output pulled high

One n-FET turned on, but does not control output



# The CMOS NAND Gate

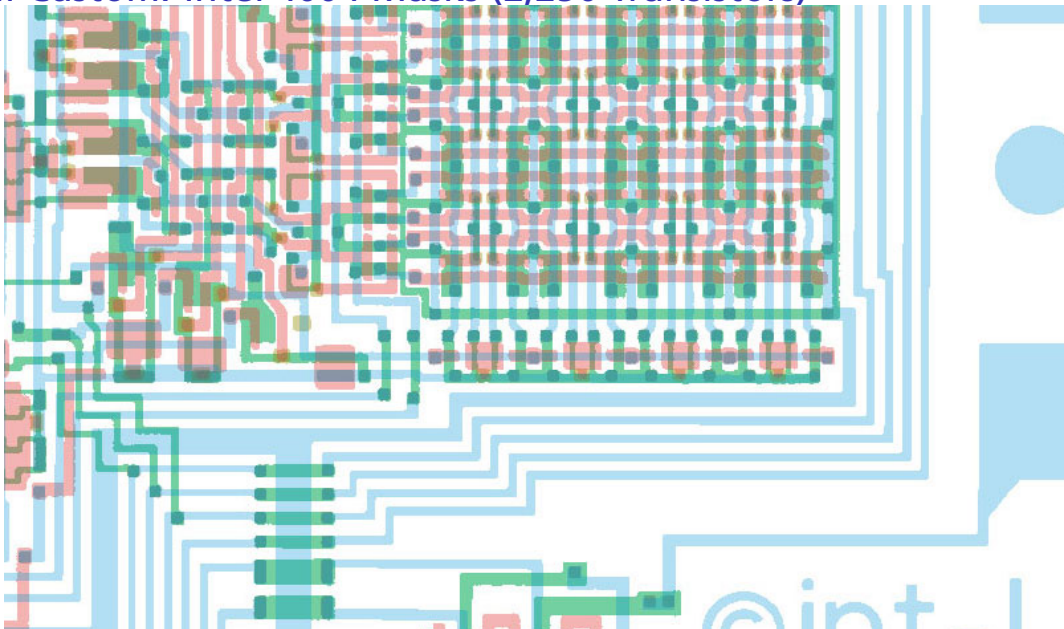


Both inputs 0:

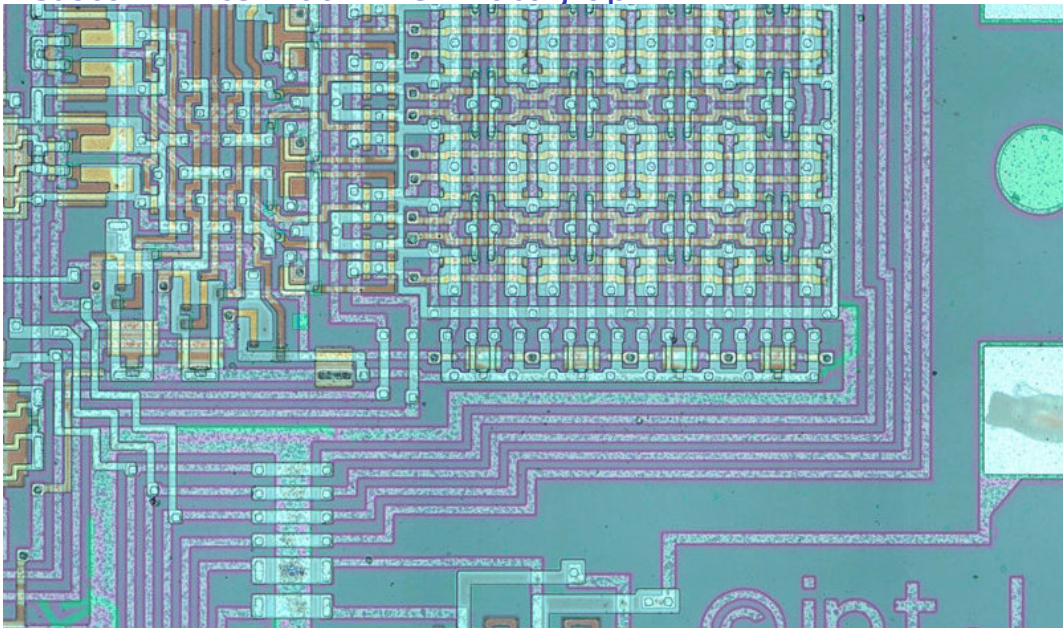
Both p-FETs turned on

Output pulled high

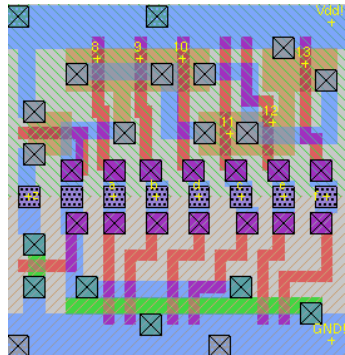
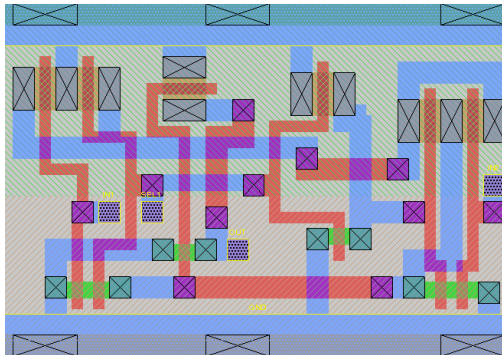
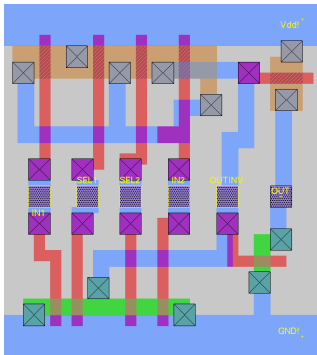
## Full Custom: Intel 4004 Masks (2,250 Transistors)



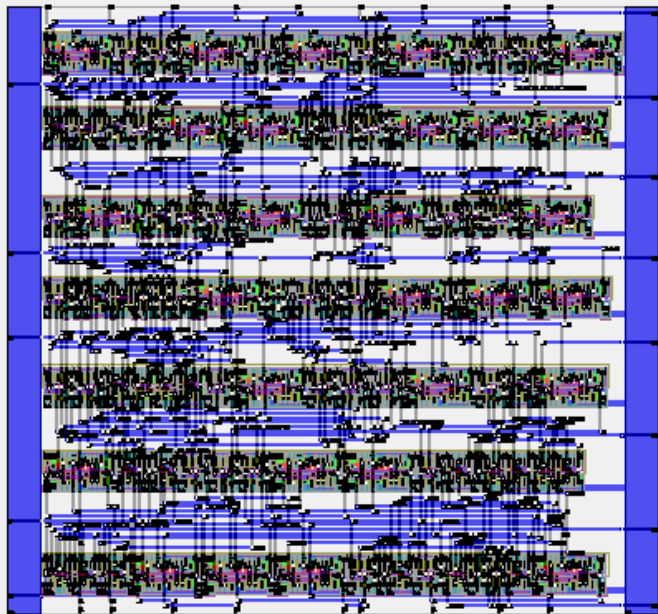
# Full Custom: Intel 4004 Die Photograph



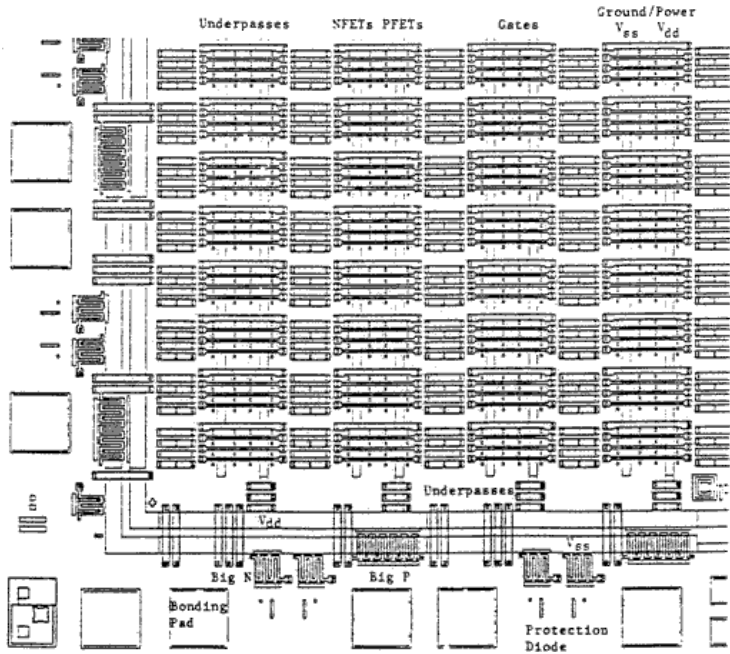
# Standard Cell ASICs



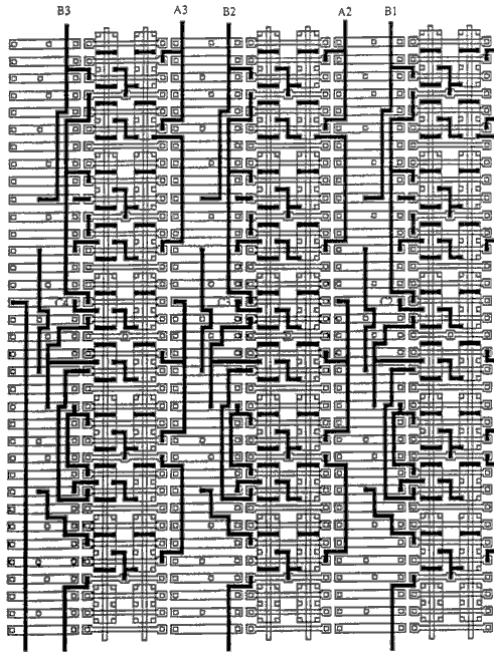
# Standard Cell ASICs



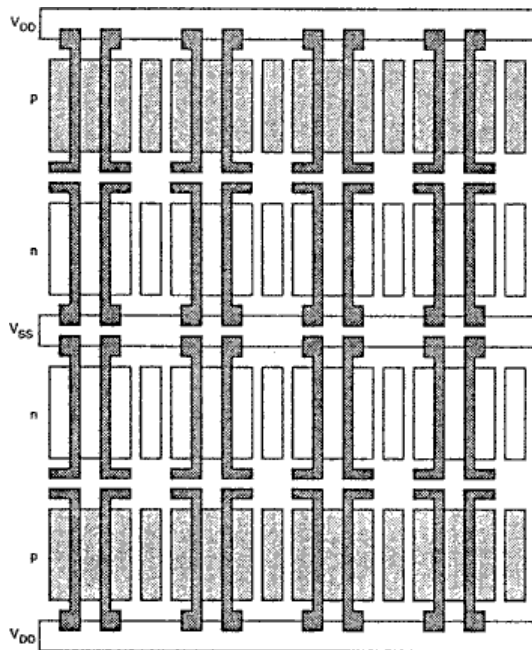
# Channeled Gate Arrays



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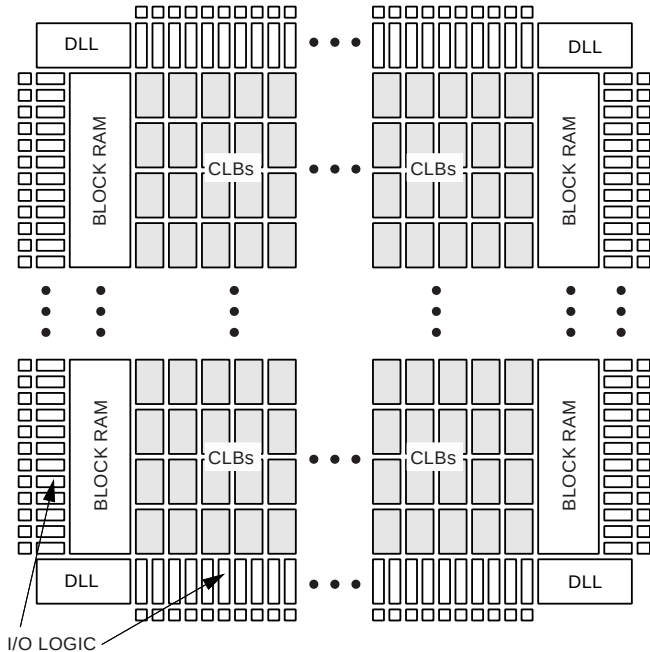


# Sea-of-Gates Gate Arrays

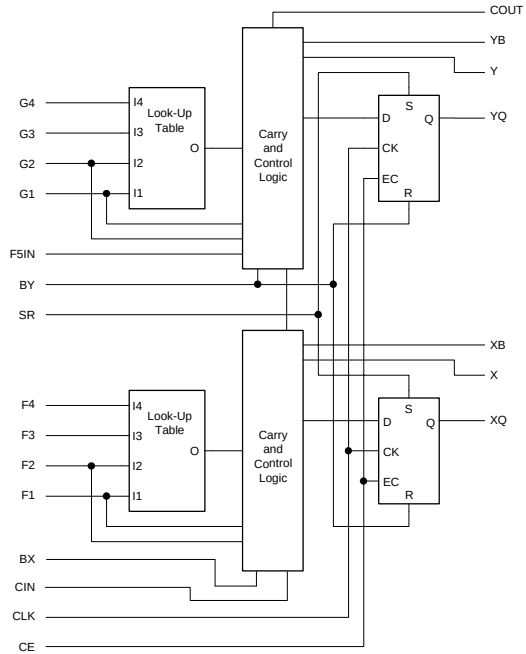




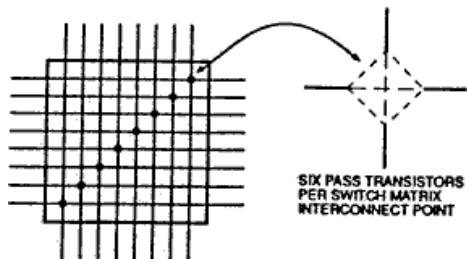
# FPGAs: Floorplan



# FPGAs: CLB

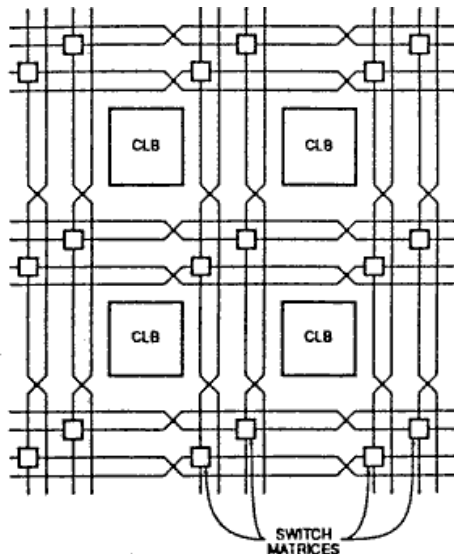


## FPGAs: Routing



SIX PASS TRANSISTORS  
PER SWITCH MATRIX  
INTERCONNECT POINT

Single-length line Switch Matrix connections



Double-length lines in CLB array

# PLAs/CPLDs: The 22v10

