

IP Cores and Platform Designer

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IP Cores

IP Integration with Quartus

IP Integration with Platform Designer

Bus Bridges

Control and Data Planes

IP Cores

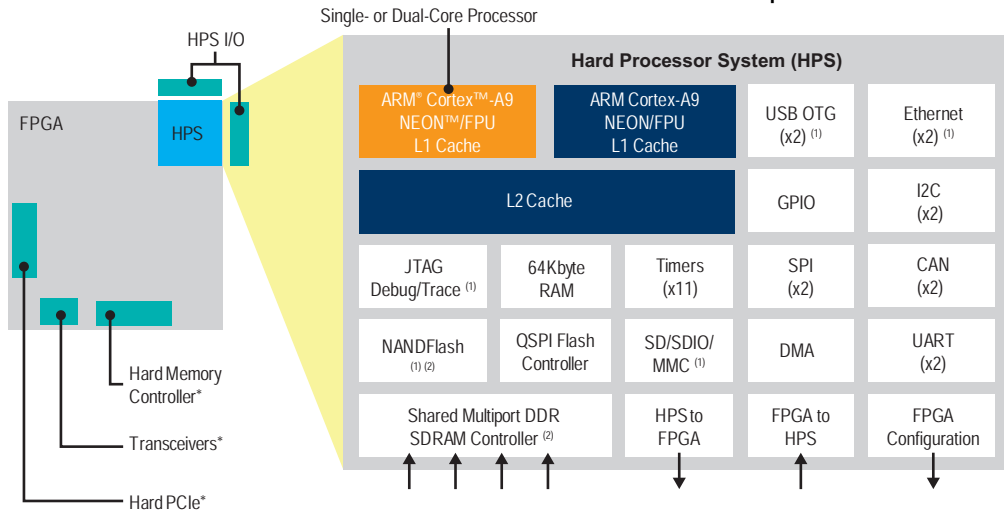
Cyclone V SoC: A Mix of Hard and Soft IP Cores

IP = Intellectual Property

Hard = wires & transistors

Core = block, design, circuit, etc.

Soft = implemented w/ FPGA



Example IP Cores

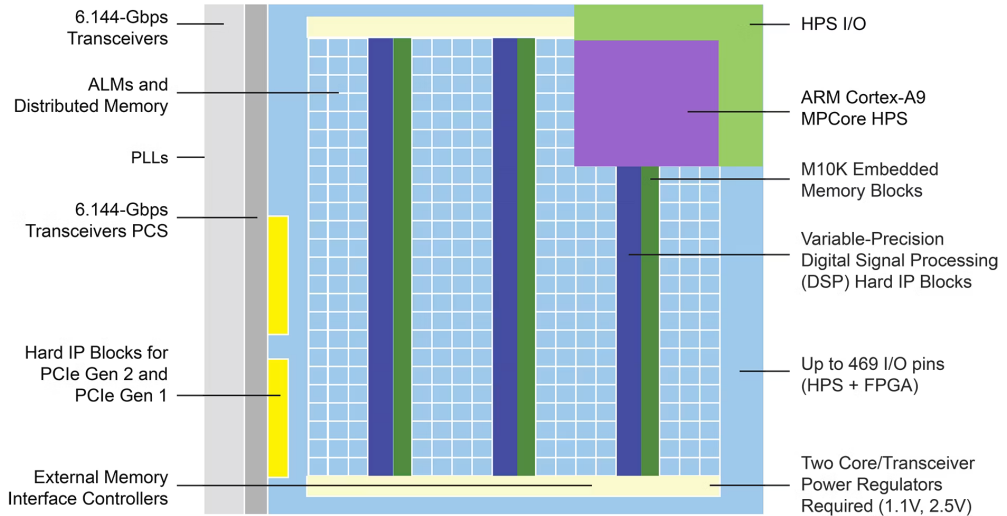
CPUs: ARM (hard), NIOS-II (soft)

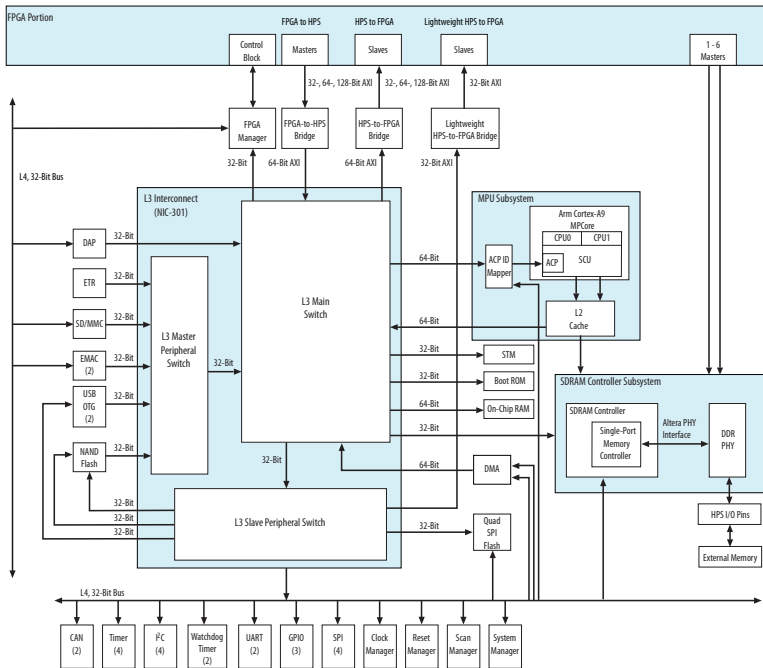
Highspeed I/O: Hard IP Blocks for High Speed Transceivers (PCI Express, 10Gb Ethernet)

Memory Controllers: DDR3

Clock and Reset signal generation: PLLs

Cyclone V SoC: FPGA layout





Cyclone V SoC: HPS Block Diagram

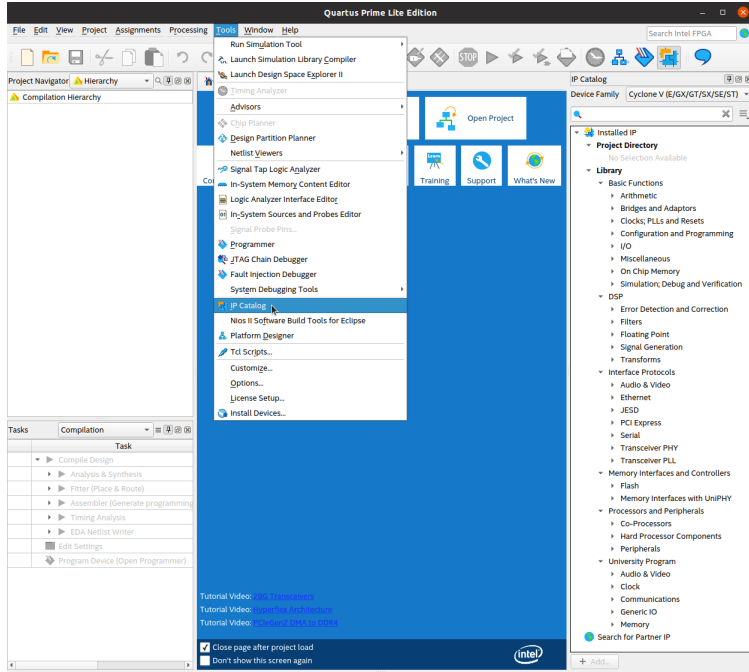
These are all hard
IP cores

Source: Intel/Altera
Cyclone V Hard Processor
System Technical
Reference Manual

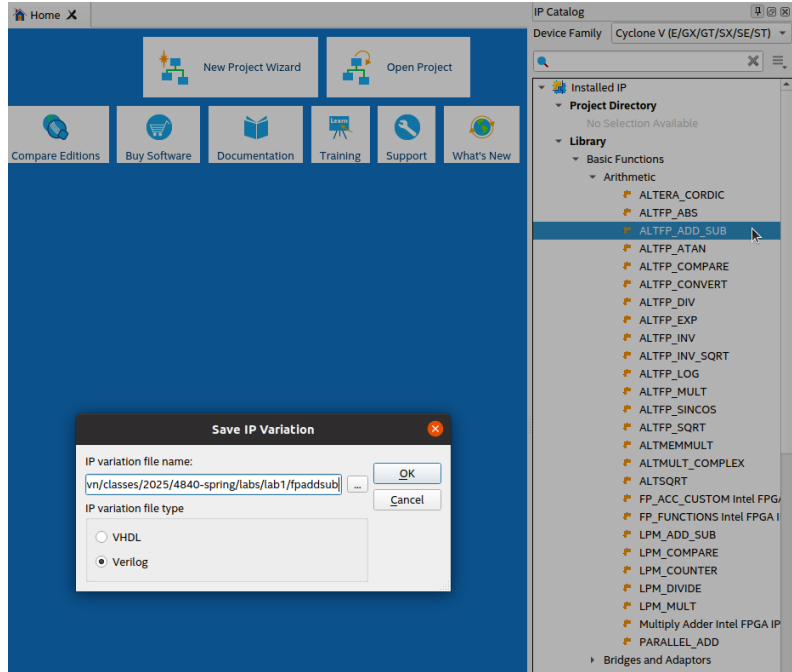
IP Integration with Quartus

The IP Catalog in Quartus

Formerly the “Megawizard”



Selecting a
floating-point
add/sub IP core



Setting its parameters

MegaWizard Plug-In Manager [page 1 of 5]

ALTFP_ADD_SUB [About](#) [Documentation](#)

1 Parameter Settings 2 EDA 3 Summary

General > Optional Input/Exception Ports > Optimization >

Currently selected device family: Cyclone V

☒ Match project/default

What is the floating point format?

☒ Single precision (32 bits)
☐ Double precision (64 bits)
☐ Single extended precision (43 bits to 64 bits)

How wide should the 'dataaa' input, 'datab' input, and 'result' output buses be? 32 bits

How wide should the exponent field be? 8 bits

Mantissa width = (data input width) - (exponent field width) - 1 23 bits

What is the output latency in clock cycles? 14

Which operating mode do you want for the adder/subtractor?

☐ Addition only
☐ Subtraction only
☒ Create an 'add_sub' input port to do both

Resource Usage

Cancel < Back Next > Finish

fpaddsub

dataaa[31..0] result[31..0]
datab[31..0]
add_sub
clock
Clock Cycles: 14
Single Precision
Exponent Width: 8
Mantissa Width: 23
Optimization: Speed

Resulting fpaddsub.v

```
module fpaddsub ( add_sub, clock, dataa, datab, result);
  input          add_sub, clock;
  input  [31:0]  dataa, datab;
  output [31:0]  result;

  wire [31:0] sub_wire0;
  wire [31:0] result = sub_wire0[31:0];

  altfp_add_sub    altfp_add_sub_component (.add_sub (add_sub),
                                              .clock (clock),
                                              .dataa (dataa),
                                              .datab (datab),
                                              .result (sub_wire0));

  defparam altfp_add_sub_component.denormal_support = "NO",
           altfp_add_sub_component.direction = "VARIABLE",
           altfp_add_sub_component.optimize = "SPEED",
           altfp_add_sub_component.pipeline = 14,
           altfp_add_sub_component.reduced_functionality = "NO",
           altfp_add_sub_component.width_exp = 8,
           altfp_add_sub_component.width_man = 23;

endmodule
```

Megawizard IP Cores

Core-specific interfaces on each

Arithmetic: $+$, $-$, \times , \div , Multiply-Accumulate, ECC

Floating Point: $+$, $-$, \times , \div

Gate Functions: Shift Registers, Decoders, Multiplexers

I/O Functions: PLL, temp sensor, remote update, high speed transceivers

Memory: Single/Dual-port RAMs, Single/Dual-clock FIFOs, Shift registers

DSP: FFT, ECC, FIR, etc.

Video: large suite

Some megafunctions are only available on certain FPGAs

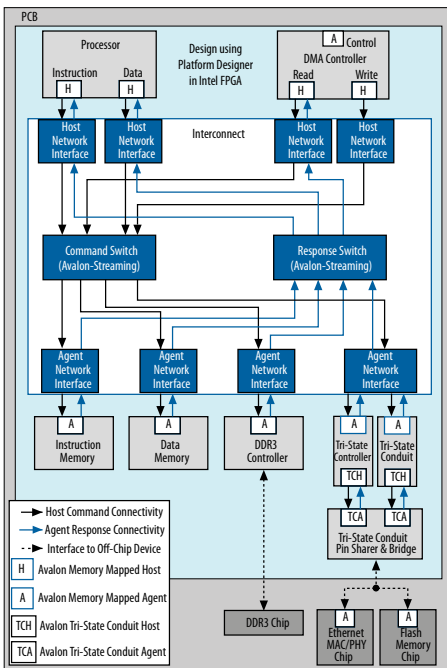
IP Integration with Platform Designer

Altera/Intel Platform Designer

Generates the interconnect logic for connecting a mix of IP Cores with **Avalon/AXI/APB/ACE** interfaces

You specify the components and their connections and Platform Designer generates the Verilog for it all

Formerly "Qsys"



Platform Designer



















Platform Designer - soc_system.qsys (/mnt/sedwards/svn/classes/2025/4840-spring/labs/lab3-hw/soc_system.qsys)

File Edit System Generate View Tools Help

IP Catalog System Contents Address Map Interconnect Requirements

System: soc_system Path: clk_0

Use Connections Name Description Export Clock Base End IRQ

<input checked="" type="checkbox"/>		clk_0	Clock Source	clk	exported			
<input checked="" type="checkbox"/>		clk_in	Clock Input	reset	clk_0			
<input checked="" type="checkbox"/>		clk_in_reset	Reset Input	Double-click to Double-click to				
<input checked="" type="checkbox"/>		clk	Clock Output	Double-click to Double-click to				
<input checked="" type="checkbox"/>		clk_reset	Reset Output	Double-click to Double-click to				
<input checked="" type="checkbox"/>		hps_0	Arria V/Cyclone V Hard Proces...	Double-click to Double-click to				
<input checked="" type="checkbox"/>		h2f_user1_clock	Clock Output	Double-click to Double-click to				
<input checked="" type="checkbox"/>		memory	Conduit	Double-click to Double-click to				
<input checked="" type="checkbox"/>		hps_io	Conduit	Double-click to Double-click to				
<input checked="" type="checkbox"/>		h2f_reset	Reset Output	Double-click to Double-click to				
<input checked="" type="checkbox"/>		h2f_axi_clock	Clock Input	Double-click to Double-click to				
<input checked="" type="checkbox"/>		h2f_axi_master	AXI Master	Double-click to Double-click to				
<input checked="" type="checkbox"/>		f2h_axi_clock	Clock Input	Double-click to Double-click to				
<input checked="" type="checkbox"/>		f2h_axi_slave	AXI Slave	Double-click to Double-click to				
<input checked="" type="checkbox"/>		h2f_lw_axi_clock	Clock Input	Double-click to Double-click to				
<input checked="" type="checkbox"/>		h2f_lw_axi_master	AXI Master	Double-click to Double-click to				
<input checked="" type="checkbox"/>		f2h_irq0	Interrupt Receiver	Double-click to Double-click to				
<input checked="" type="checkbox"/>		f2h_irq1	Interrupt Receiver	Double-click to Double-click to				

Current filter:

Messages

Type	Path	Message
Warning	2 Warnings	
Warning	soc_system.hps_0	"Configuration/HPS-to-FPGA user 0 clock frequency" (desired_cfg_clk_mhz) requested 100.0 MHz, but only achieve
Warning	soc_system.hps_0	1 or more output clock frequencies cannot be achieved precisely, consider revising desired output clock frequencies.
Info	2 Info Messages	

0 Errors, 2 Warnings

Generate HDL... Finish

Bus Bridges

Bus Bridges

A bus bridge connects two, often different, buses.

Enables multiple clock domains, different protocols (e.g., AXI \leftrightarrow Avalon), bus widths, etc.

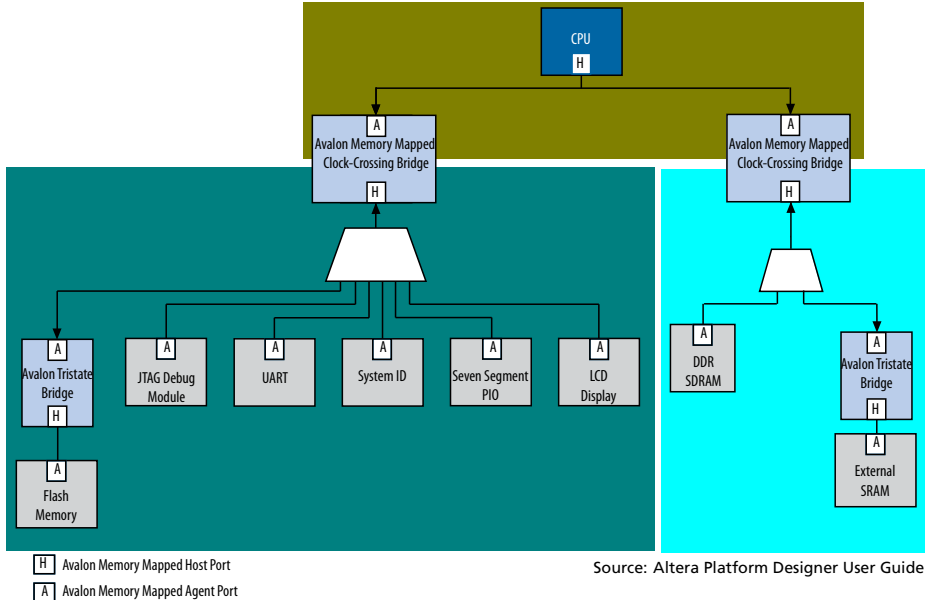
Example Bridge Types:

SOC HPS \leftrightarrow FPGA Bridge

Avalon MM Clock Crossing Bridge

Avalon MM Pipeline Bridge

Clock Crossing Bridge Example

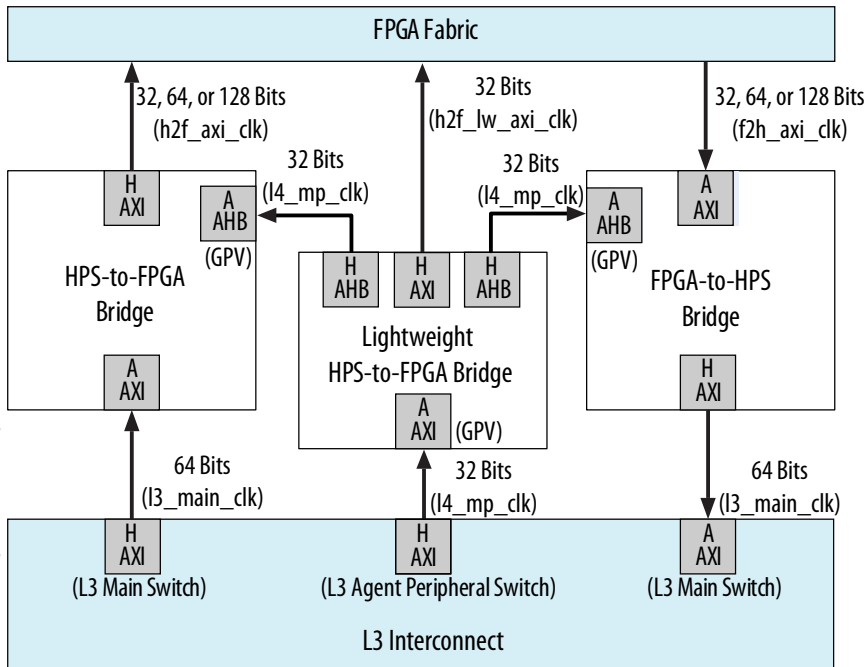


Cyclone V HPS-FPGA Bridges

32-bit
lightweight for
configuration

32/64/128 high-
performance
FPGA agents

32/64/128 high-
performance
FPGA hosts



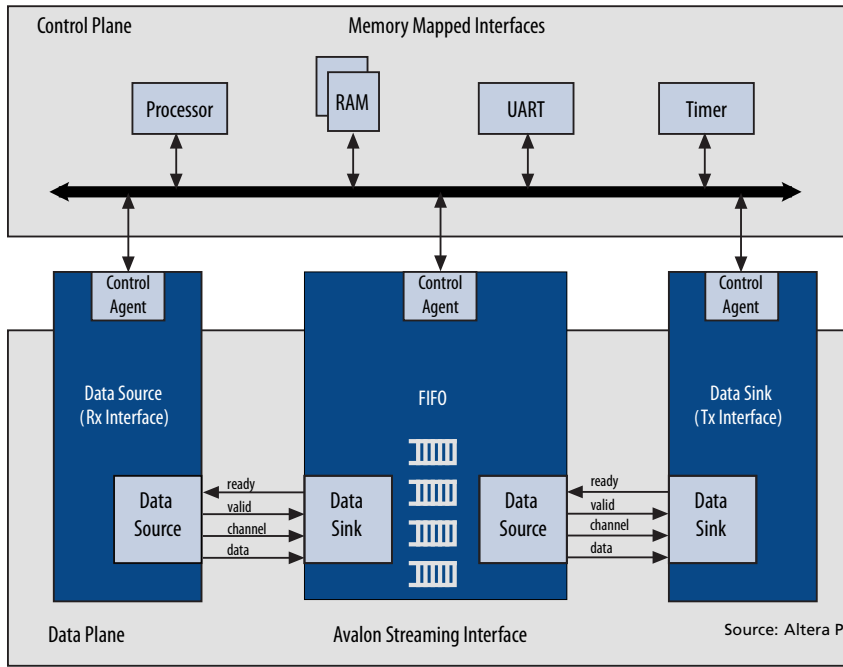
Control and Data Planes

Control vs. Data Planes

Control Plane: Memory mapped registers typically used for configuring devices, querying status, initiating transactions, etc (low bandwidth)

Data Plane: Streaming directed graphs for actually moving and processing large amounts of data (audio/video, network packets, etc); high bandwidth

A single IP core can have both MM and ST interfaces (including multiple of each).



References to Altera/Intel Documentation

Cyclone V Device Handbook: Volume 1: Device Interfaces and Integration

<https://www.intel.com/content/www/us/en/docs/programmable/683375/current/logic-array-blocks-and-adaptive-logic-24877.html>

Cyclone V Hard Processor System Technical Reference Manual

<https://www.intel.com/content/www/us/en/docs/programmable/683126/21-2/hard-processor-system-technical-reference.html>

Intel Quartus Prime Standard Edition User Guide: Platform Designer

<https://www.intel.com/content/www/us/en/docs/programmable/683364/18-1/creating-a-system-with.html>