Processors, FPGAs, and ASICs

Part 1: Full Custom to PLDs

Stephen A. Edwards

Columbia University

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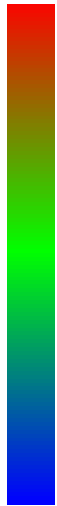
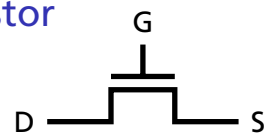
Spectrum of IC choices

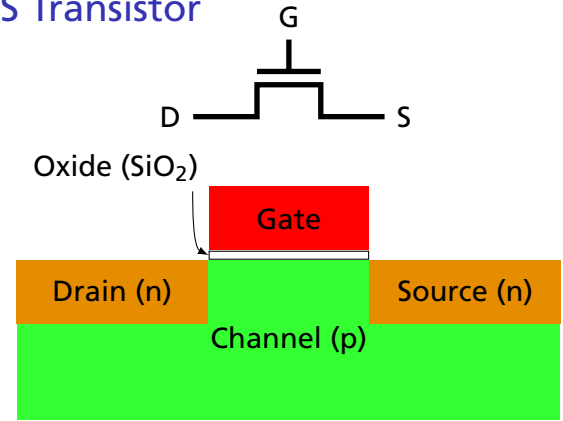


Flexible, efficient	**You choose**
Full Custom	Polygons (Intel)
ASIC	Circuit (Sony)
Gate Array	Wires
FPGA	Logic network
PLD	Logic function
GP Processor	Program (e.g., ARM)
SP Processor	Program (e.g., DSP)
Multifunction	Settings (e.g., Ethernet Ctrl.)
Fixed-function	Part number (e.g., 74HCT00)
Cheap, quick to design	

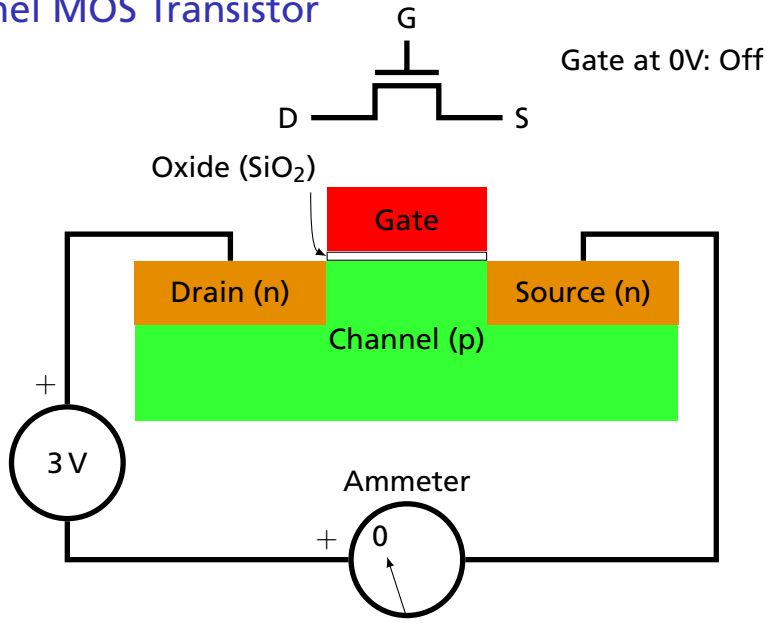
An N-Channel MOS Transistor



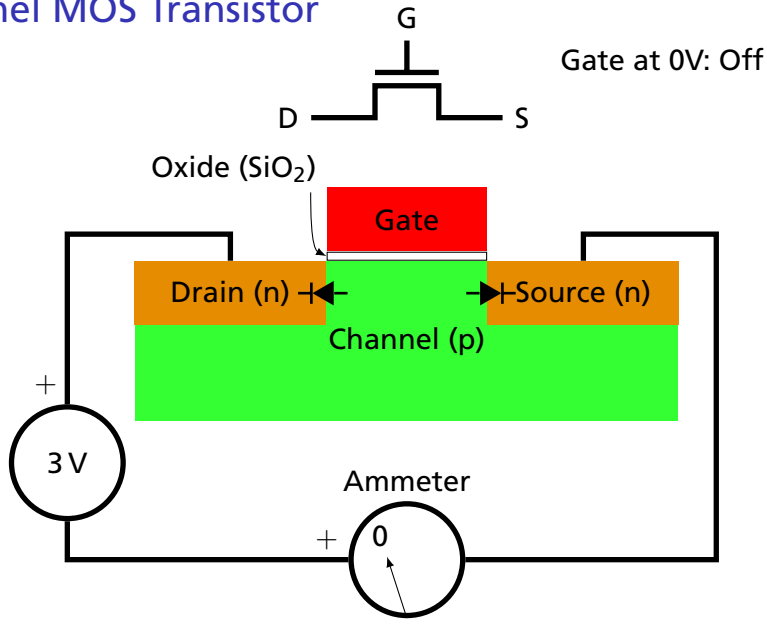
An N-Channel MOS Transistor



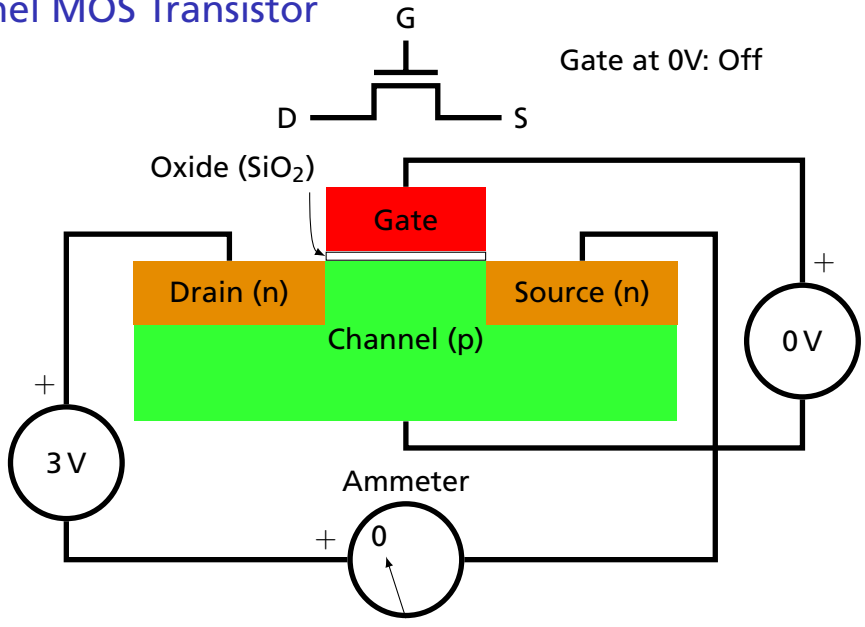
An N-Channel MOS Transistor



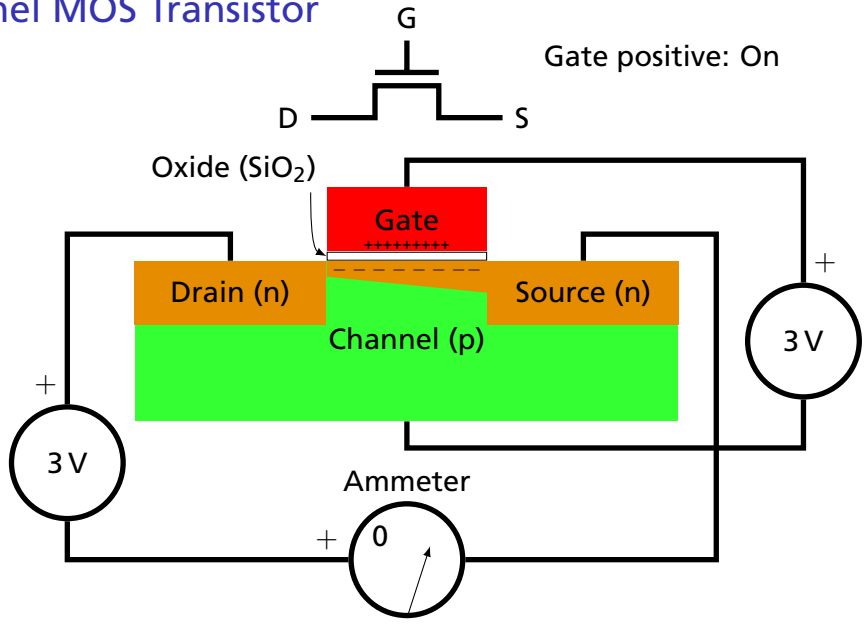
An N-Channel MOS Transistor



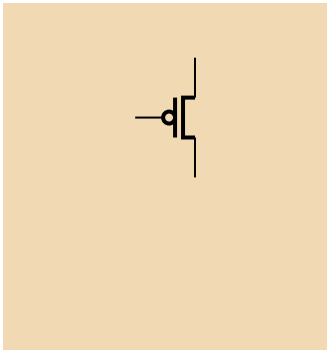
An N-Channel MOS Transistor



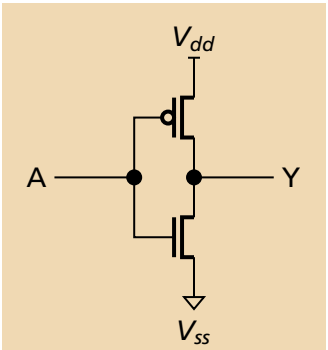
An N-Channel MOS Transistor



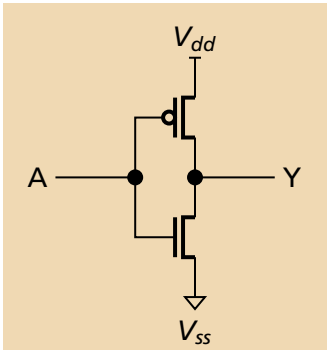
CMOS Inverter Layout

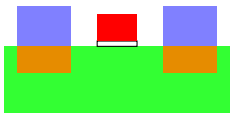


CMOS Inverter Layout

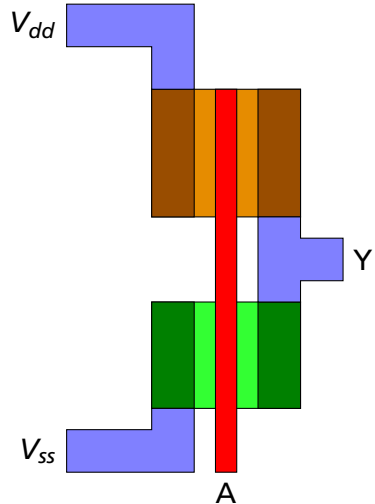


CMOS Inverter Layout



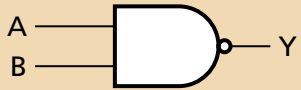


Cross Section Through N-channel FET



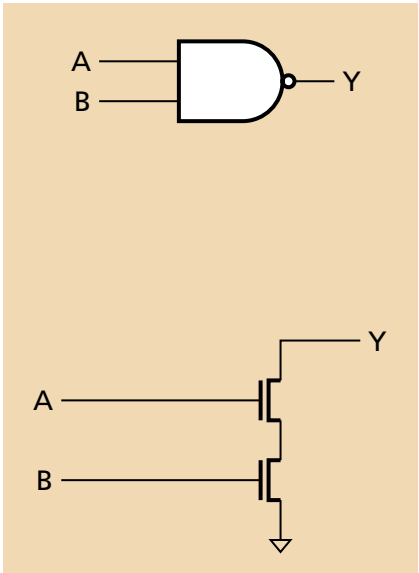
Top View

The CMOS NAND Gate



Two-input NAND gate:

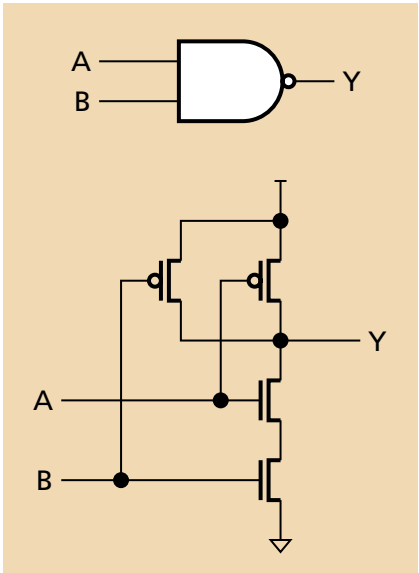
The CMOS NAND Gate



Two-input NAND gate:

two n-FETs in series;

The CMOS NAND Gate

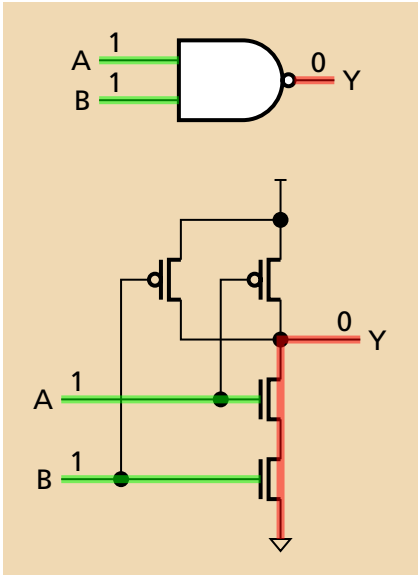


Two-input NAND gate:

two n-FETs in series;

two p-FETs in parallel

The CMOS NAND Gate



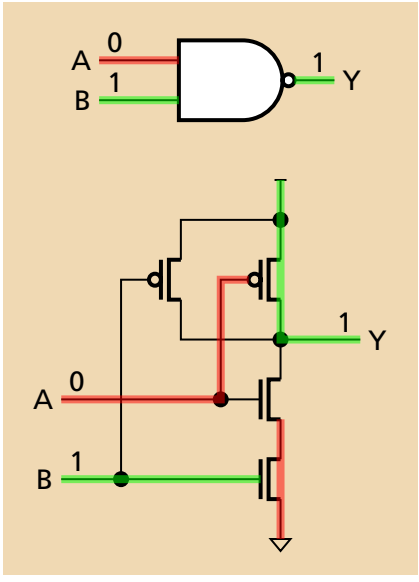
Both inputs 1:

Both n-FETs turned on

Output pulled low

Both p-FETs turned off

The CMOS NAND Gate



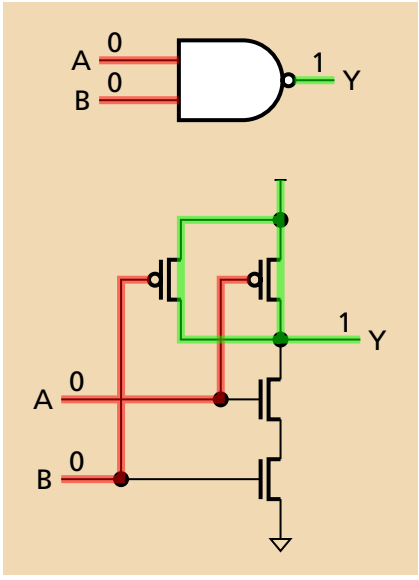
One input 1, the other 0:

One p-FET turned on

Output pulled high

One n-FET turned on, but does not control output

The CMOS NAND Gate

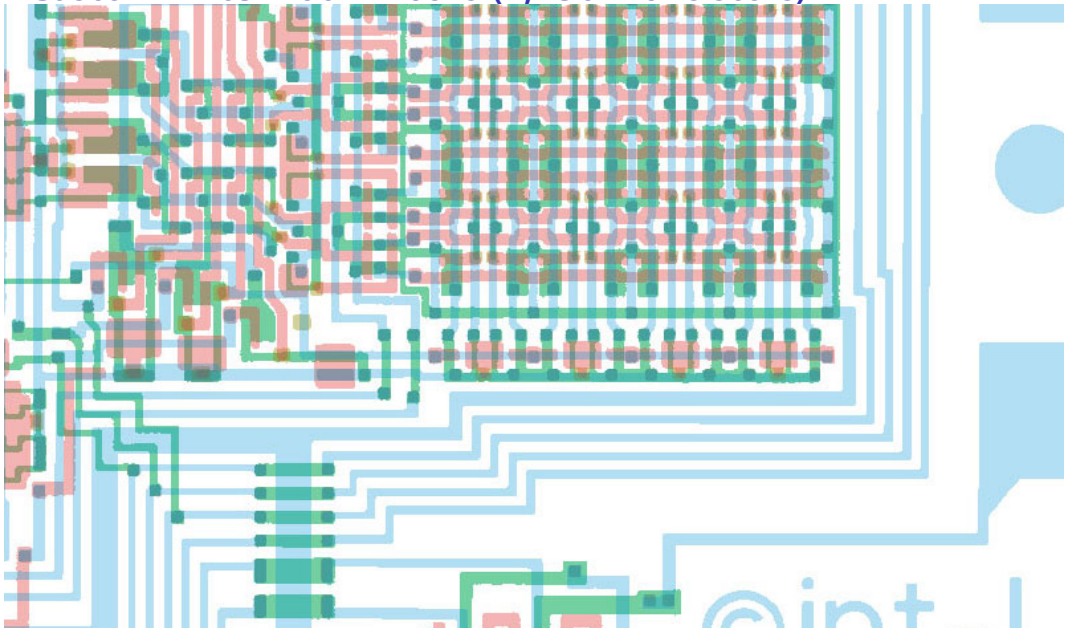


Both inputs 0:

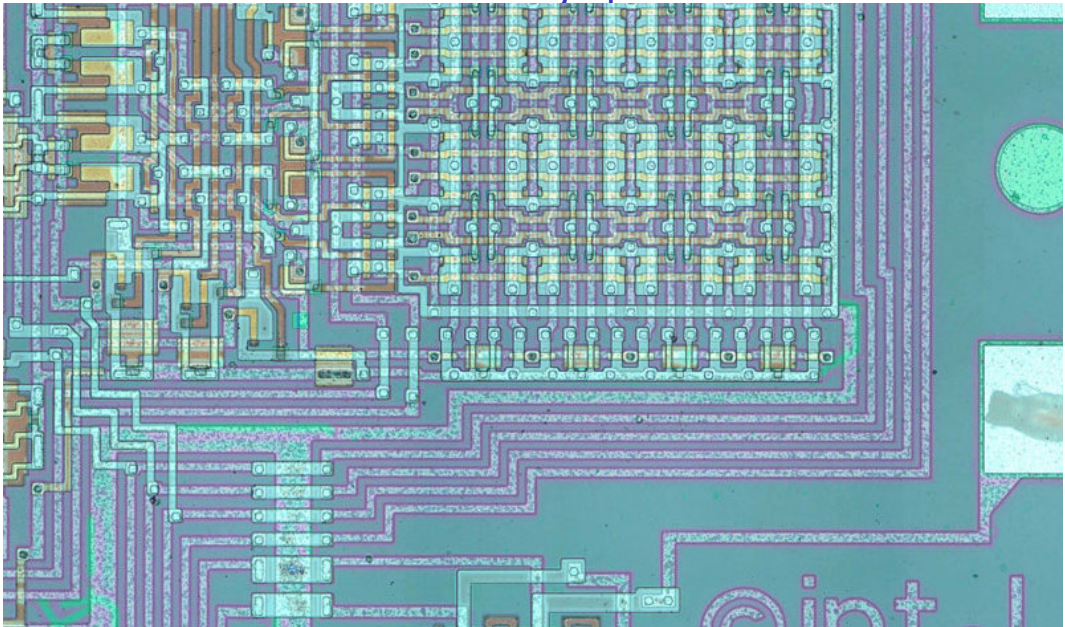
Both p-FETs turned on

Output pulled high

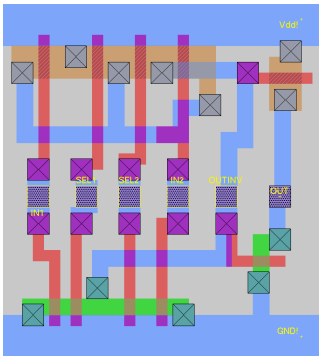
Full Custom: Intel 4004 Masks (2,250 Transistors)

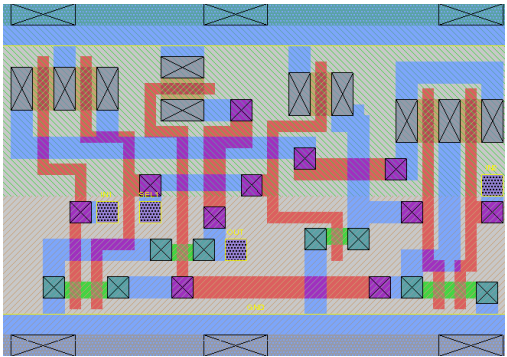


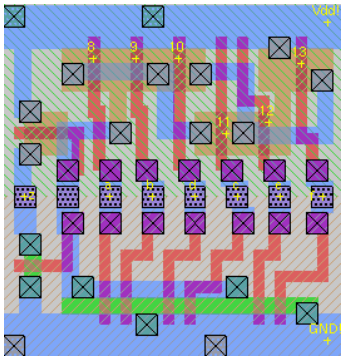
Full Custom: Intel 4004 Die Photograph



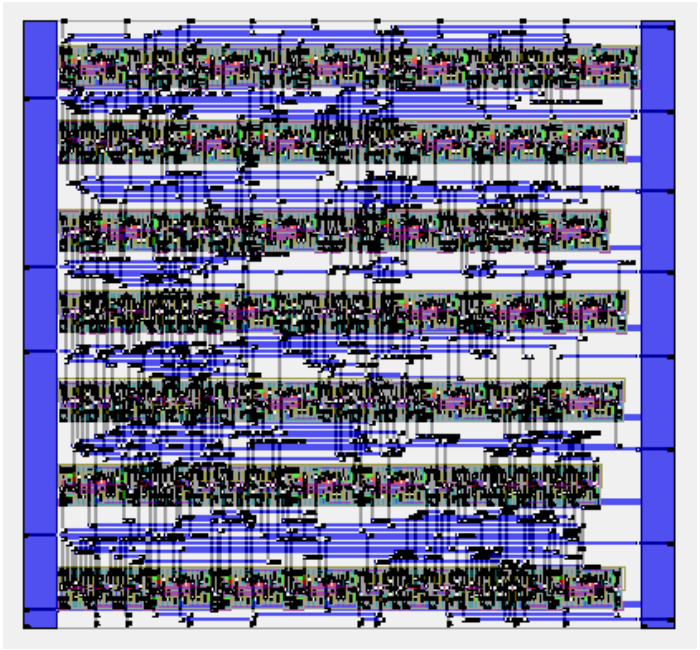
Standard Cell ASICs



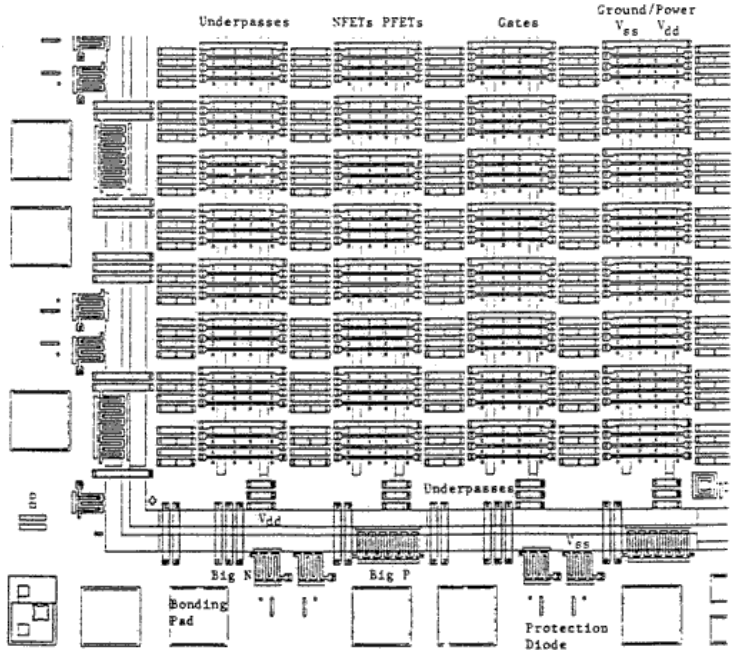




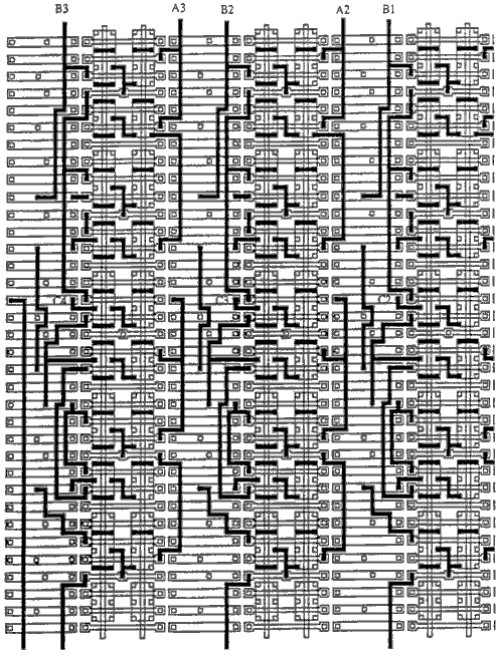
Standard Cell ASICs



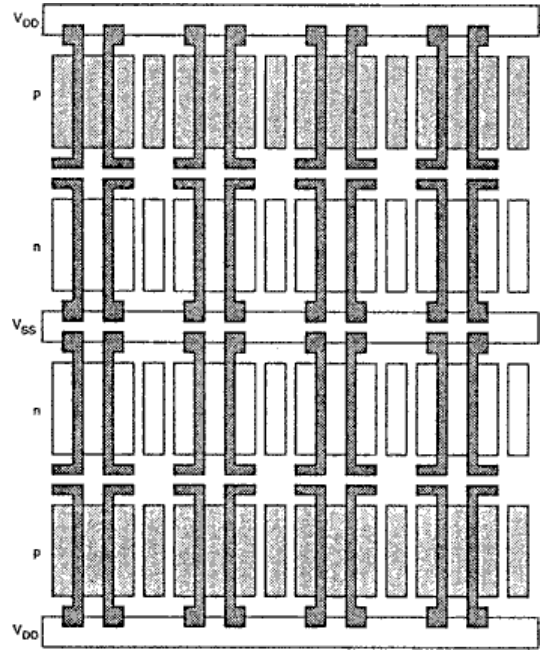
Channeled Gate Arrays



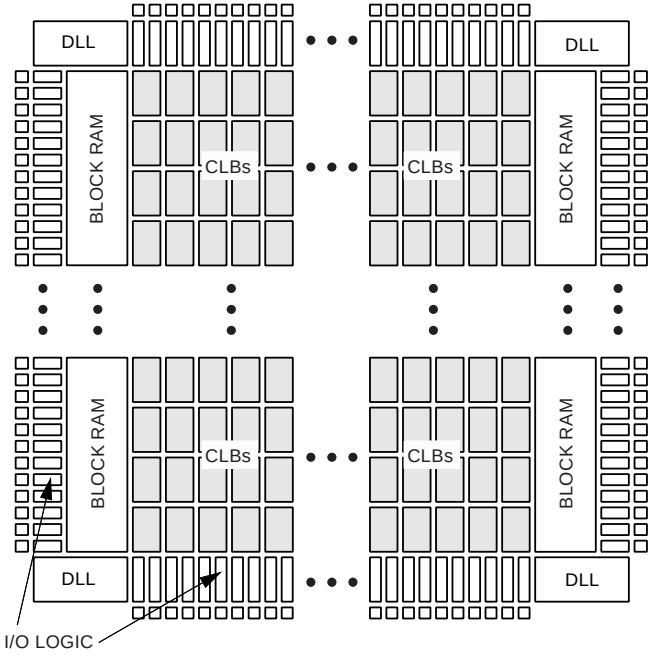
Channeled Gate Arrays



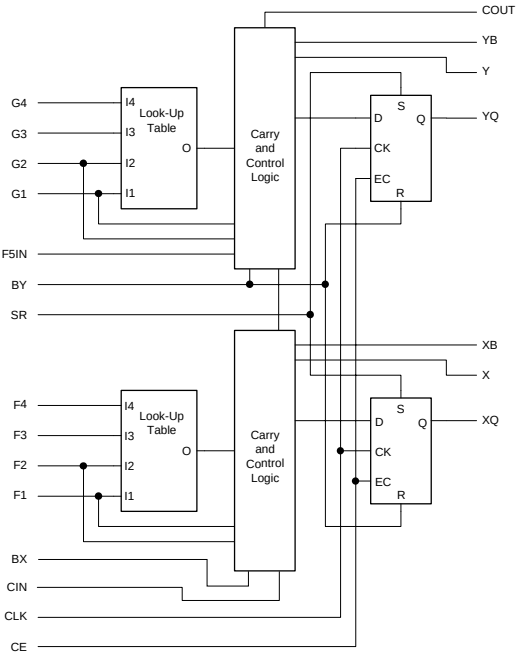
Sea-of-Gates Gate Arrays



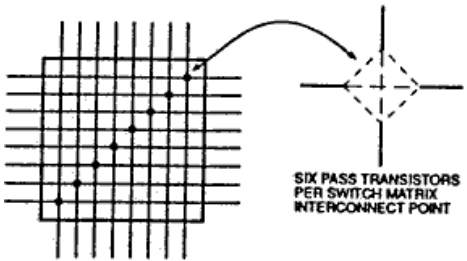
FPGAs: Floorplan



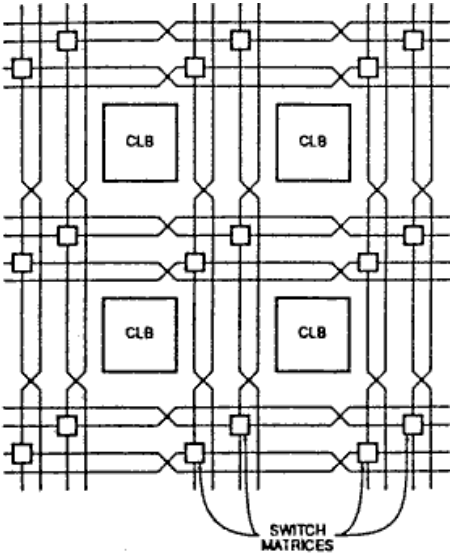
FPGAs: CLB


COUT
YB
Y
G4
G3
G2
G1
I4
I3
I2
I1
Look-Up Table
O
Carry and Control Logic
S
D
Q
YQ
CK
EC
R
F5IN
BY
SR
XB
X
F4
F3
F2
F1
XQ
BX
CIN
CLK
CE

FPGAs: Routing



Single-length line Switch Matrix connections



Double-length lines in CLB array

PLAs/CPLDs: The 22v10