Switch ON

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1 Aim

The project aims to simulate a virtual Network Switch that generates IP packets using software and interfaces with the memory of FPGA for switching and scheduling.

2 Description

The motivation of the project comes from our interest in optimum packet scheduling to maximise throughput. The project is also a means towards gaining more familiarity with FPGA programming in System Verilog. The idea borrows heavily from **Head of Line Blocking** in a switching fabric.

2.1 Implementation

Packet traffic will be simulated by using a packet generator which will be fed into the simulated ports on software. These packets would then be decoded and processed by the FPGA to determine the destination port for each packet. The motive would be to optimise throughput by rescheduling packets at the input and output ports.

3 Milestones

3.1 Milestone 1

Creating packet generator in C and storing the packets in the memory accessible by FPGA for decoding.

3.2 Milestone 2

Interfacing the generated packets with the in memory binary search tree and generating longest prefix match for the input packets.

3.3 Milestone 3

Creating scheduling algorithm to address the head-of-line (HoL) blocking problem for achieving maximum throughput.

3.4 Milestone 4

Completely integrating the various components of the previous milestones into a fully functional virtual network switch. Performance benchmarks and evaluation of the scheduling algorithm will be done in this step.