

A UDP packet Memcached Server Design Using FPGA

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Introduction

The speed of decoding UDP packet is concerned in many aspects. Comparing to traditional X86 structure, FPGA has a significant advantage in data processing speed due to its flexibility in design logic structure. On the other hand, the Memcached on FPGA can be used for UDP packet decoding more efficiently. Hence, we here bring this idea to generate a memcached FPGA server to decode UDP packet and provide attainable hash map on memcached.

Implementation

The memcached will take standard form of UDP packet as input. An internal processing algorithm to quickly decode the UDP packet is critical in this design. The specific algorithm is under developing for the time being. After process UDP packet and store it in hash map, the hash map will be available for the external clients to acquire.

The server administrator should be able to control some basic parameter of this memcached server, for example, the frequency of automatically receiving UDP packet.

An advanced version, if within the time allowance, will let the client has the option to write back to the FPGA server's hash map. This will require additional function that the FPGA server can send UDP package back to Internet.