ELEN E4080 - Embedded System - Project Proposal

10Gb/s Packet Processing on Hybrid SoC/FPGA Platform

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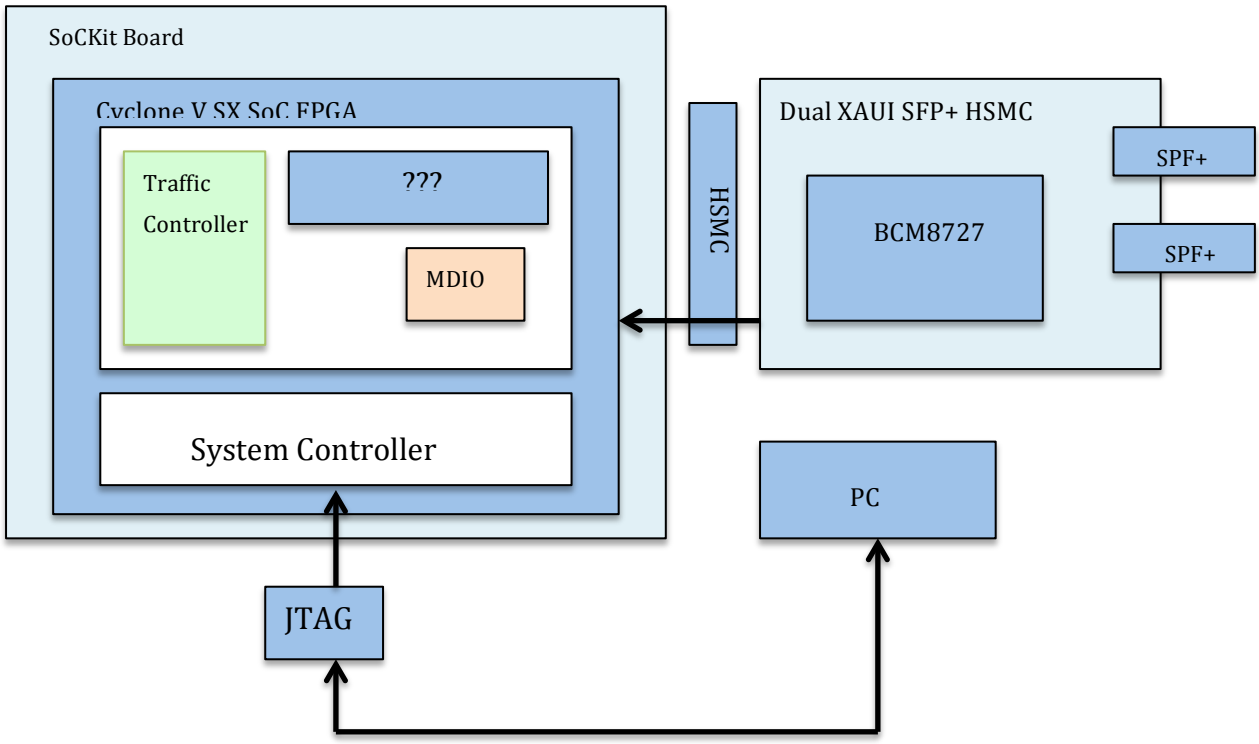
I. Background and Objective

High frequency trading (HFT) is more and more popular both in academic research and financial market for the couple of years. Firms are willing to pay huge amount of money for high speed HFT processor rely on advanced computer systems, the processing speed of their trades and their access to the market. Value is incredibly huge when each second been accelerated in stock exchange market. Based on the current HFT market, FPGA is usually implemented in many cases such as stock market data processing, large data package compression etc.

The primary purpose of this project is to successfully integrate the SoCKit ARM / FPGA platform with an external 10Gb/s Ethernet daughter card for creating a platform to enable low cost ultra high speed packet processing through both FPGA and Software.

II. SoCKit + Dual XAUI Board Platform

Architecture:



The flow chart is shown as above. The main work will be modify/generate “10GbE MAC and XAUI PHY” part which is marked as “???” and successfully make the SoCKit support XAUI communication.

The purpose of this project is to write certain IP cores in the FPGA to make it achieve the goal of 10 Gbs data transmission speed.

III. Project Schedule

Feb 25-Mar 17:

Learn the basic knowledge of the HFT, use the 10-Gbps Ethernet MAC and XAUI PHY Interoperability demonstration from Altera to understand the functionality of each block in this design.

Mar 18- Apr 1:

Build the IP core and do simulation on PC.

Apr 1- Apr 15:

Build the other peripheral components on FPGA and move the IP core from PC to FPGA (Verilog).

Apr 15- May 9:

Test the functionality and performance of the system.