CSEE W3827

Fundamentals of Computer Systems

Homework Assignment 3

Solutions

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Due February 27th, 2012 at 1:10 PM

Write your name **and UNI** on your solutions

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

1. (25 pts.) A sequential circuit with two D flip-flops S_0 and S_1, two inputs X and Y, and one output Z behaves according to these equations:

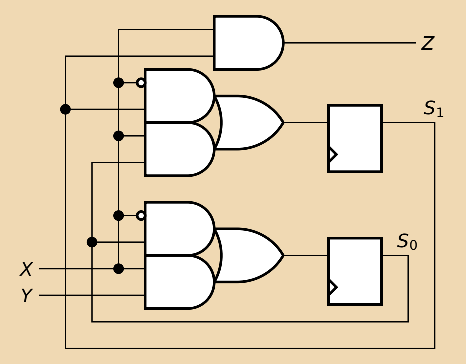
$$S_0' = \overline{X}S_0 + XY \quad S_1' = \overline{X}S_1 + XS_0 \quad Z = XS_1$$

(a) Draw the corresponding circuit. Label each of the signals mentioned above.

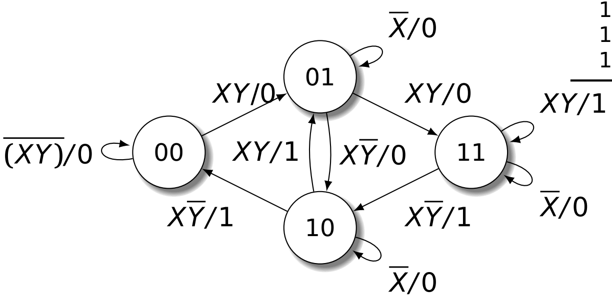
(b) Derive the state table (next state and output as a function of present state and input).

(c) Draw the corresponding bubble-and-arc diagram.

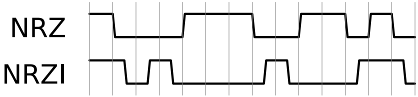
$$S_0' = \overline{X}S_0 + XY \quad S_1' = \overline{X}S_1 + XS_0 \quad Z = XS_1$$



S_1S_0	**X**	**Y**	$S_1'S_0'$	**Z**
00	0	0	00	0
00	0	1	00	0
00	1	0	00	0
00	1	1	01	0
01	0	0	01	0
01	0	1	01	0
01	1	0	10	0
01	1	1	11	0
10	0	0	10	0
10	0	1	10	0
10	1	0	00	1
10	1	1	01	1
11	0	0	11	0
11	0	1	11	0
11	1	0	10	1
11	1	1	11	1



2. (15 pts.) Many serial communication protocols, such as USB, use a signaling protocol known as “non return to zero, inverted” (NRZI) in which a “0” is represented as a transition and a “1” as no transition. Below is an example of a normal bit stream (NRZ) and how it would be encoded in NRZI as a waveform on the left and the corresponding bit streams on the right.



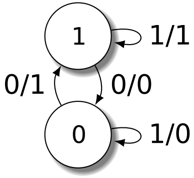
10001110011010

10100001000110

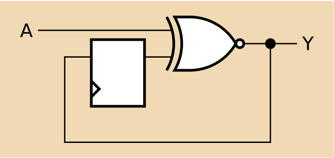
(a) Draw a Mealy bubble-and-arc diagram for an NRZ-to-NRZI protocol converter.

(b) Choose an encoding for your state machine and write its (encoded) state table.

(c) Design and draw a circuit implementation of your converter using D flip-flops and gates.



S	**A**	**Y**	**S′**
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1



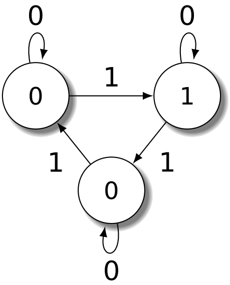
3. (15 pts.) Determine the logic for a synchronous 4-bit decimal counter that counts 0,1,. . . ,9,0,1,. . . in binary. It should have four outputs Q_1, Q_2, Q_4, Q_8, (the subscripts indicate the value of each bit) each driven directly by a flip-flop.

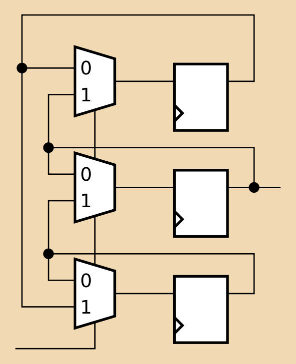
Write Boolean expressions of the form $D_i = Q_i \oplus (\cdots)$ for each flip-flop's input. ($\oplus$ is XOR)

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
0000
0001

$$
\begin{aligned}
D_1 &= Q_1 \oplus 1 \\
D_2 &= Q_2 \oplus (\overline{Q_8} Q_1) \\
D_4 &= Q_4 \oplus (Q_2 Q_1) \\
D_8 &= Q_8 \oplus (Q_4 Q_2 Q_1 + Q_8 Q_1)
\end{aligned}
$$

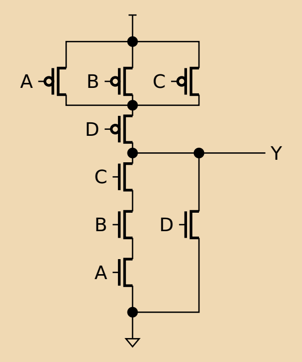
4. (15 pts.) Using just three flip-flops and three two-input muxes, draw a circuit for the following Moore state machine with a single input and single output. Use a one-hot encoding. Each state is labeled with the value of the output.

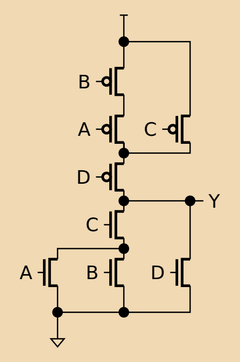




5. (15 pts.)

(a) Write a Boolean expression for the function of the following static CMOS gate.



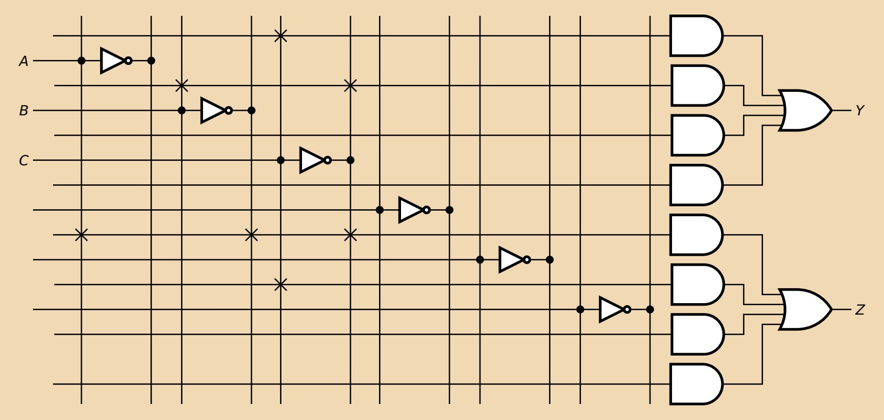


$Y = \overline{ABC + D}$

(b) Draw the schematic for a static CMOS gate that implements $Y = \overline{(A+B)C + D}$

6. (15 pts.) Show how to implement a two-bit priority encoder using the PLA drawn below.
Hint: write the expressions for Y and Z in sum-of-products form then draw crosses to indicate connections on the AND plane.

A	**B**	**C**	**YZ**
0	0	0	00
1	0	0	01
X	1	0	10
X	X	1	11



$Y = C + B\overline{C}$ or $Y = B + C$

$Z = A\overline{B}\,\overline{C} + C$ or $Z = A\overline{B} + C$