

CSEE W3827

Fundamentals of Computer Systems

Homework Assignment 2

Solutions

Prof. Stephen A. Edwards

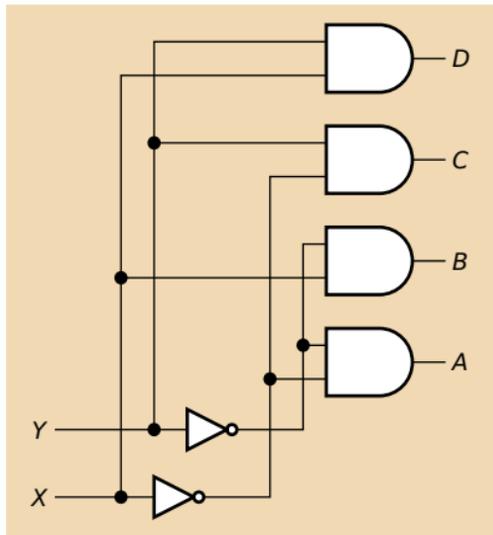
Columbia University

Due September 29th, 2011 at 10:35 AM

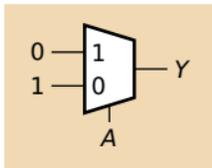
Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

1. (10 pts.) Draw the circuit for a 2-to-4 decoder using AND gates and inverters.

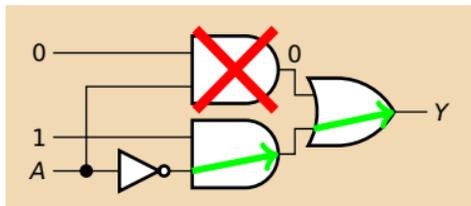
It should have two inputs X and Y and four outputs A , B , C , and D . Only one of the outputs should be true at one time.



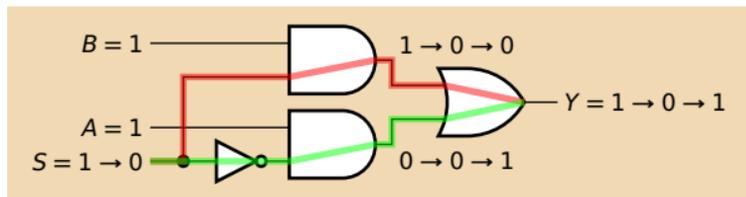
2. (a) (10 pts.) Show how to implement an inverter using just a two-input mux (no additional gates).



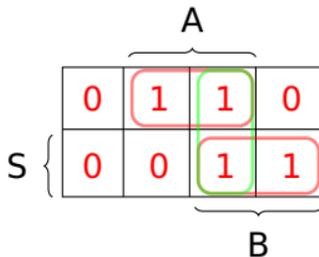
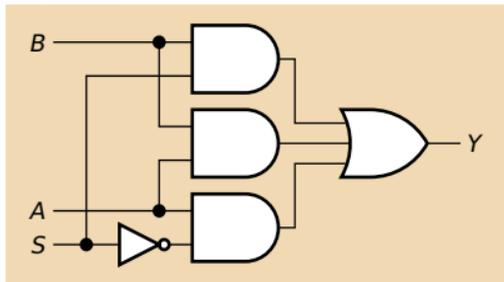
- (b) Show how your solution, when the mux2 is implemented as shown below, can be simplified into a single inverter.



3. (20 pts.) Consider the following circuit for a two-input mux.



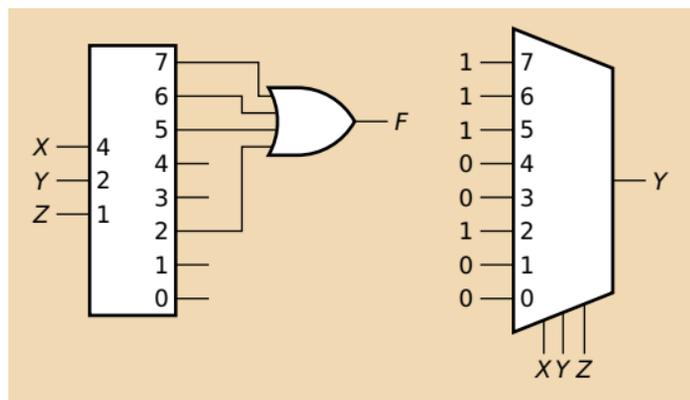
- Under what conditions could the output of this circuit glitch low? I.e., for what assignment of input values would changing one input's value cause the output to briefly transition from 1 to 0 to 1?
- Show how adding a two-input AND gate and widening the OR gate could eliminate this glitch.
- Draw the Karnaugh map corresponding to your new glitch-free circuit.



4. (15 pts.) Show how to implement $F = XY + X\bar{Y}Z + Y\bar{Z}$ using

(a) a 3-to-8 decoder and an OR gate;

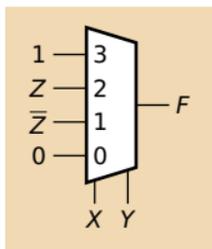
X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



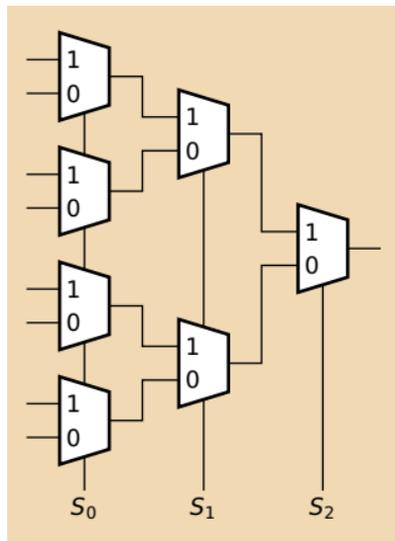
(b) an 8 input mux; and

(c) a 4 input mux whose select inputs are X and Y and an inverter.

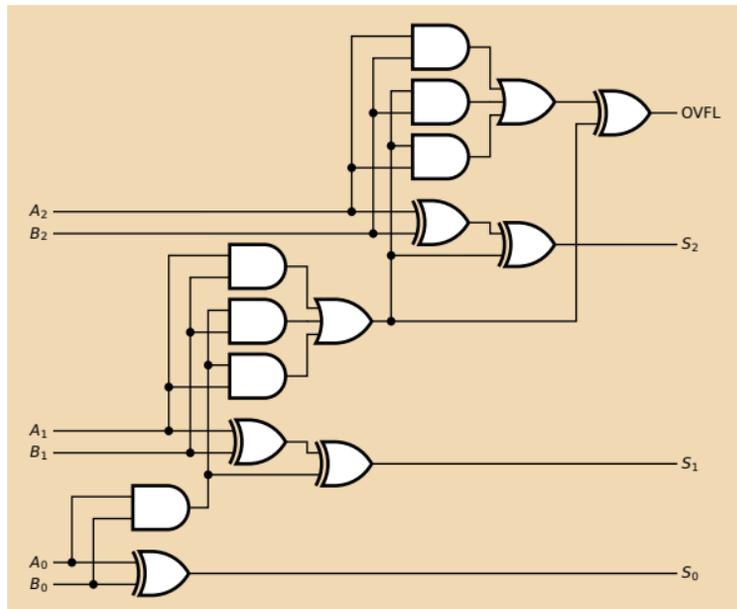
X	Y	F
0	0	0
0	1	\bar{Z}
1	0	Z
1	1	1



5. (10 pts.) Draw a circuit for an eight-input mux using seven two-input muxes and no other gates.



6. (20 pts.) Using AND, OR, and XOR gates only, draw the circuit for a three-bit two's complement ripple carry adder with an overflow output. Your circuit should have six inputs (three bits for each addend) and four outputs (three results bits; one indicating overflow).



7. (15 pts.) Write the carry-out function in sum-of-products form for a five-bit binary adder in terms of

- C_0 , the incoming carry;
- G_0 through G_4 , the carry-generate signals for the five bits; and
- P_0 through P_4 , the carry-propagate signals for the five bits.

$$C_{i+1} = G_i + C_i P_i$$

$$C_1 = G_0 + C_0 P_0$$

$$\begin{aligned} C_2 &= G_1 + C_1 P_1 \\ &= G_1 + G_0 P_1 + C_0 P_0 P_1 \end{aligned}$$

$$\begin{aligned} C_3 &= G_2 + C_2 P_2 \\ &= G_2 + G_1 P_2 + G_0 P_1 P_2 + C_0 P_0 P_1 P_2 \end{aligned}$$

$$\begin{aligned} C_4 &= G_3 + C_3 P_3 \\ &= G_3 + G_2 P_3 + G_1 P_2 P_3 + G_0 P_1 P_2 P_3 + C_0 P_0 P_1 P_2 P_3 \end{aligned}$$

$$\begin{aligned} C_5 &= G_4 + C_4 P_4 \\ &= G_4 + G_3 P_4 + G_2 P_3 P_4 + G_1 P_2 P_3 P_4 + G_0 P_1 P_2 P_3 P_4 + \\ &\quad C_0 P_0 P_1 P_2 P_3 P_4 \end{aligned}$$