Gianfranco Bonanome CS4995
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Literature Survey

Generally a comparison between two computer languages is based on the number of lines of code and execution time required to achieve a specific task, using the two languages. A number of additional parameters can be observed, such as features, existence or absence of constructs that facilitate coding, availability of optimization techniques, as well as others. This criteria varies slightly when attempting to compare two hardware description languages (HDLs). For instance, execution time is no longer a valid parameter, since simulated models are usually written to run in a specific number of clock cycles or for a set delay, and will therefore be the same. What can be utilized as a basis for comparison is overall code length, efficiency of methods and language constructs, signal behavior description, and ease of implementation.

In this paper I will be comparing different aspects between the Verilog and SystemC HDLs, according to the measures mentioned above. The code that will be used to base this comparison will implement an alarm clock controller.

The existing work in this specific topic is scarce at best, to my knowledge. In terms of an actual comparison between two HDLs, I have found no papers written on this topic itself, but a few that touch on Verilog vs. VHDL[5]. These papers may not help directly with my paper, but offer great points of comparison. Since SystemC is a relatively new language, I was able to find several papers about it, some of which I listed below, along with the rest of my current references.

The actual implementation of the project consists in modeling an alarm clock controller in both Verilog and SystemC, to expose their benefits and flaws. The controller will have all standard functions of an alarm clock, such as setting time, alarm, and a "snooze" button. To compile and simulate Verilog, I will be using Synapticad’s Verilogger Pro. To compile SystemC an updated version of Microsoft Visual Studio 6.0 with SystemC libraries will be utilized. The objective of this simulation is to deepen my understanding of the languages and expose their differences, as described above.

In order to better acquaint myself with the two languages I will be using the following materials:

[1] S. Edwards. Languages for Embedded Systems. Kluwer 2000.
[2] T. Kropf. The Verilog Hardware Description Language. Kluwer 1996.
[3] G. DeMicheli. Synthesis and Optimization of digital circuits. McGraw Hill 1994.
[4] Synopsys. SystemC version 1.1 User’s guide. 2000.
[5] D. Smith. VHDL & Verilog Compared & Contrasted. VeriBest Incorporated 199?
[6] System-on-Chip Specification and Modeling Using C++. ICCAD 2000 Roundtable.
[7] W. Mueller. The Simulation Semantics of SystemC. Paderborn University.
[8] On the Reuse of VHDL Modules into SystemC Designs. N.Agliada, A.Fin. F.Fummi M.Martignagno. G.Pravadelli. Universita di Verona, Italy.
[9] Behavioral Synthesis with SystemC. G. Economakos. P. Oikonomakos. I. Panagopoulos. I. Poulakis. G. Papakonstantinou. National Technical University of Athens.