

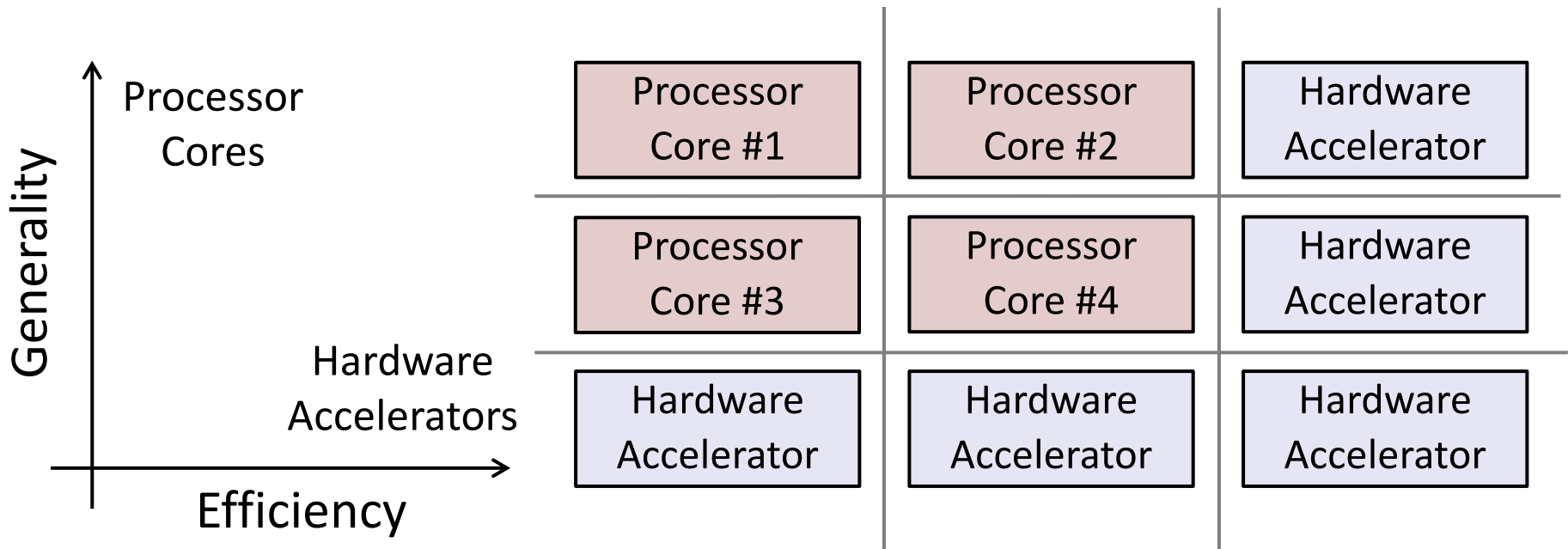
IEEE High Performance Extreme Computing Conference (HPEC), 2017

Broadening the Exploration of the Accelerator Design Space in Embedded Scalable Platforms

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Why Hardware Accelerators?

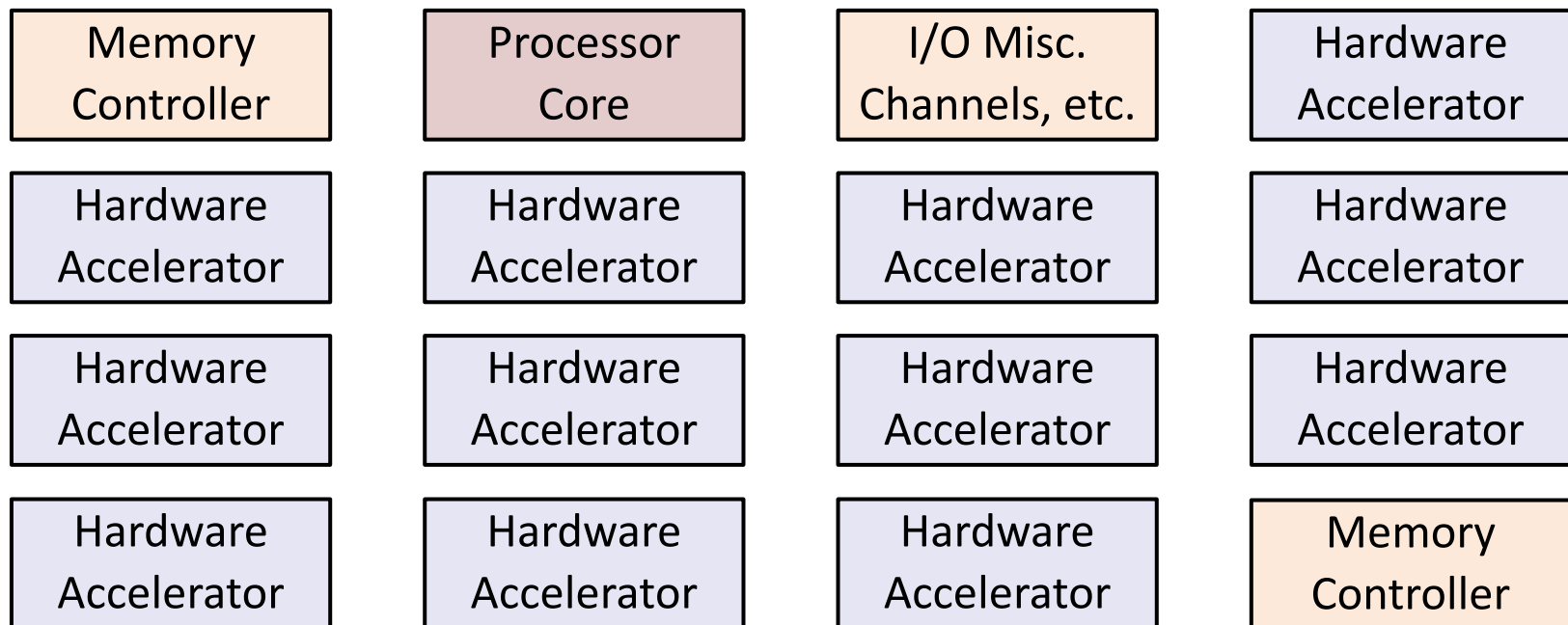
- High-performance embedded systems are heterogeneous:
 - they include multiple general-purpose processor cores
 - they include special-function hardware accelerators



Embedded Scalable Platforms (ESP)

- To balance the demand for hardware specialization with the need of maintaining helpful degrees of regularity and modularity we proposed: **Embedded Scalable Platforms**

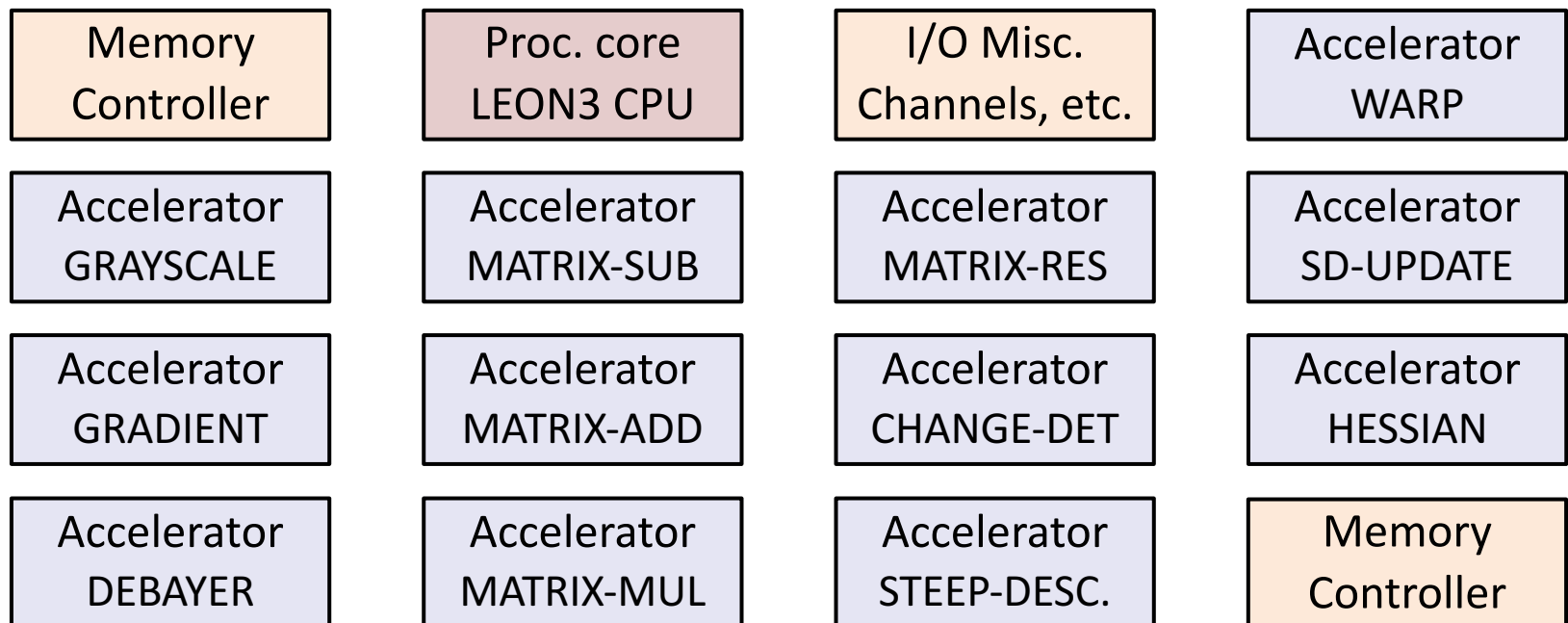
[L. Carloni, “*The Case for Embedded Scalable Platforms*”, DAC 2016]



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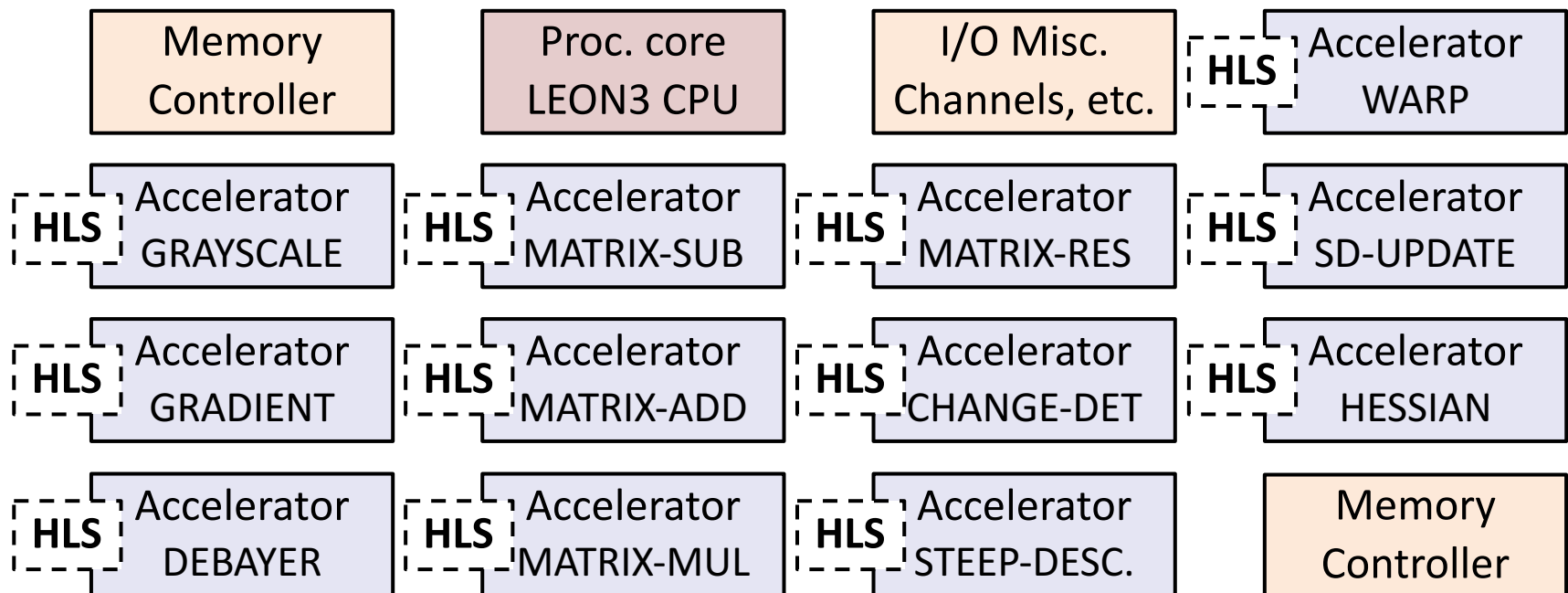
ESP instance for **WAMI (Wide-Area Motion Imagery)**



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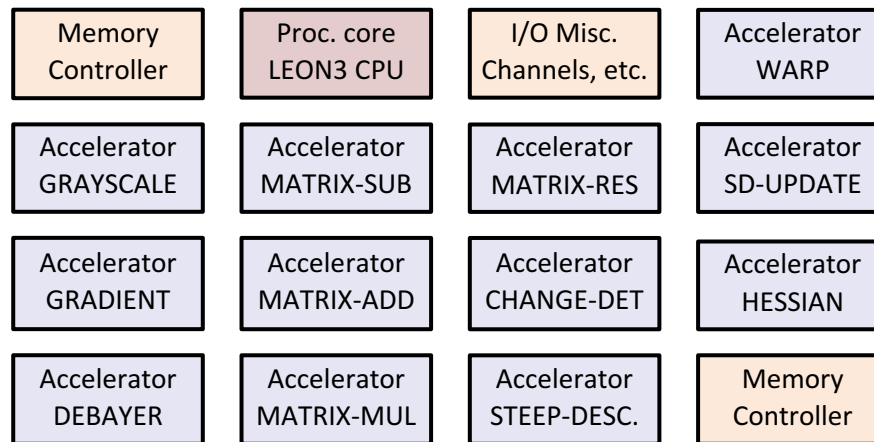
System-Level Design with **High-Level Synthesis (HLS)**



Embedded Scalable Platforms (ESP)

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System-Level Design with High-Level Synthesis (HLS)



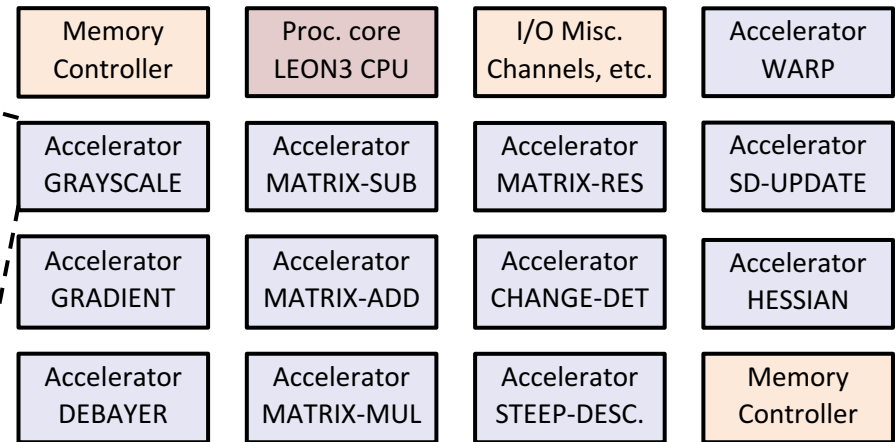
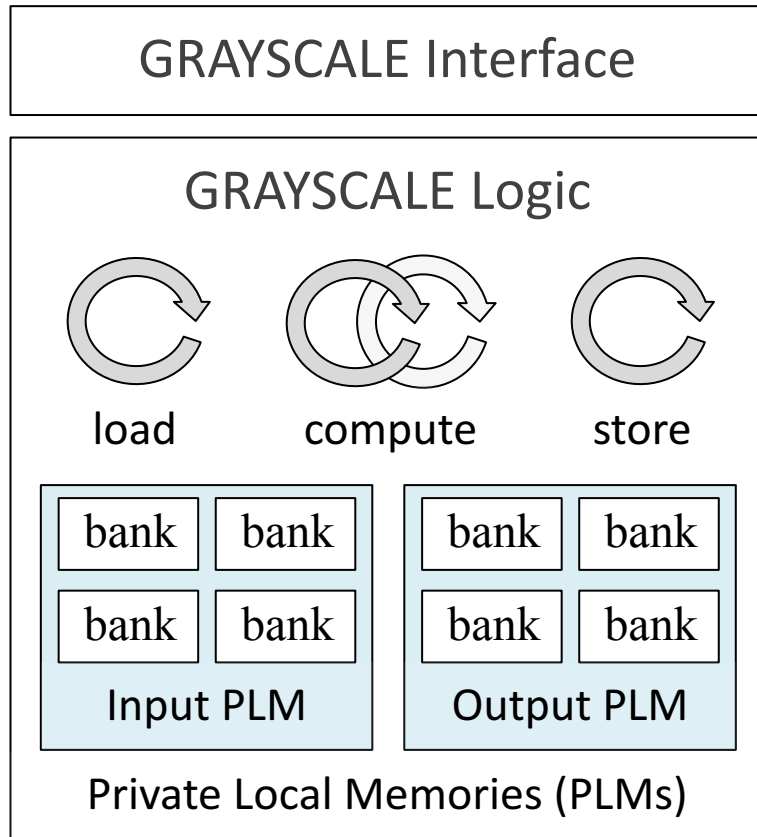
rapid integration
and prototyping



ESP instance for WAMI
(Wide-Area Motion Imagery)

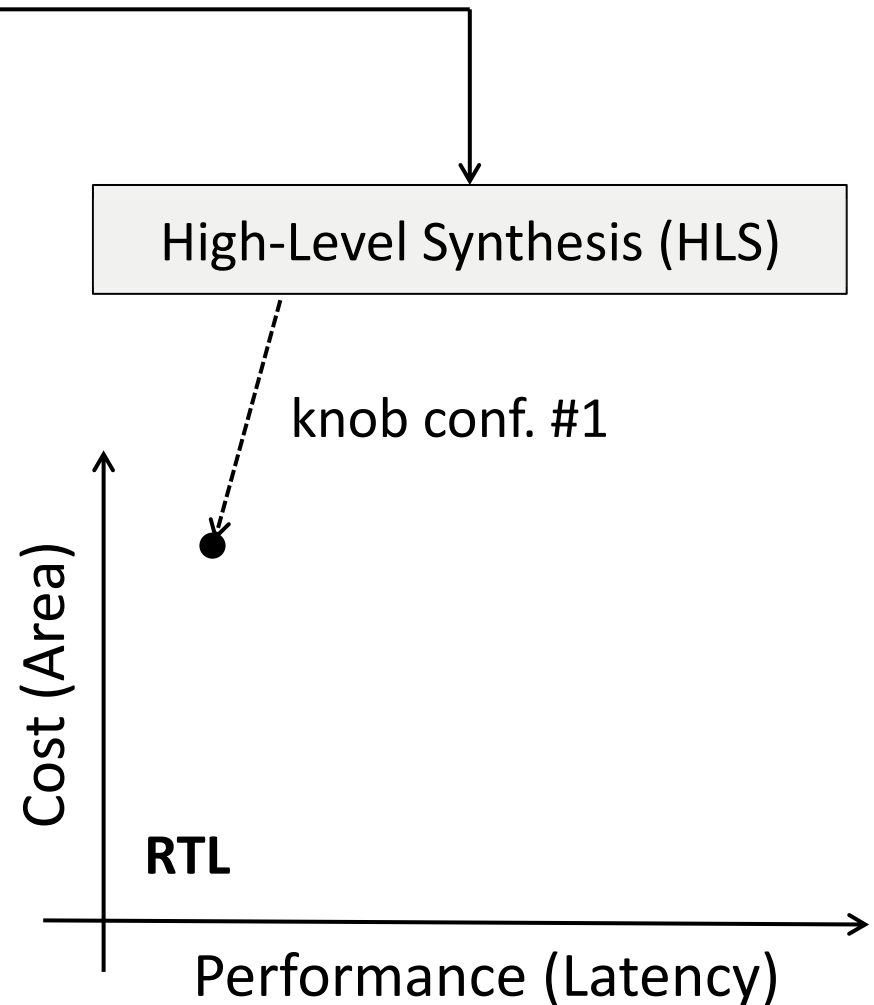
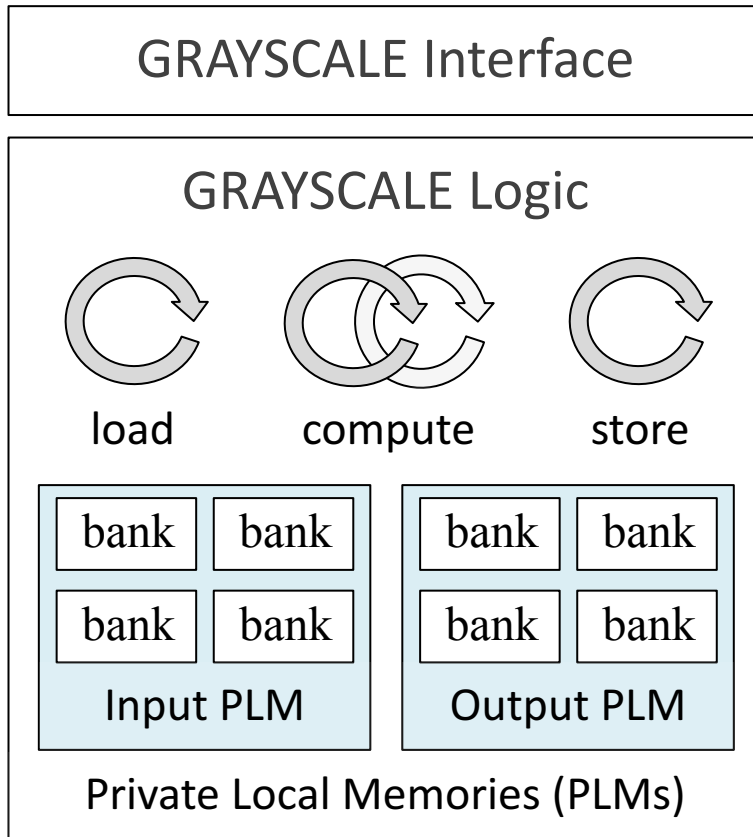
Hardware Accelerators with HLS

SystemC Specification



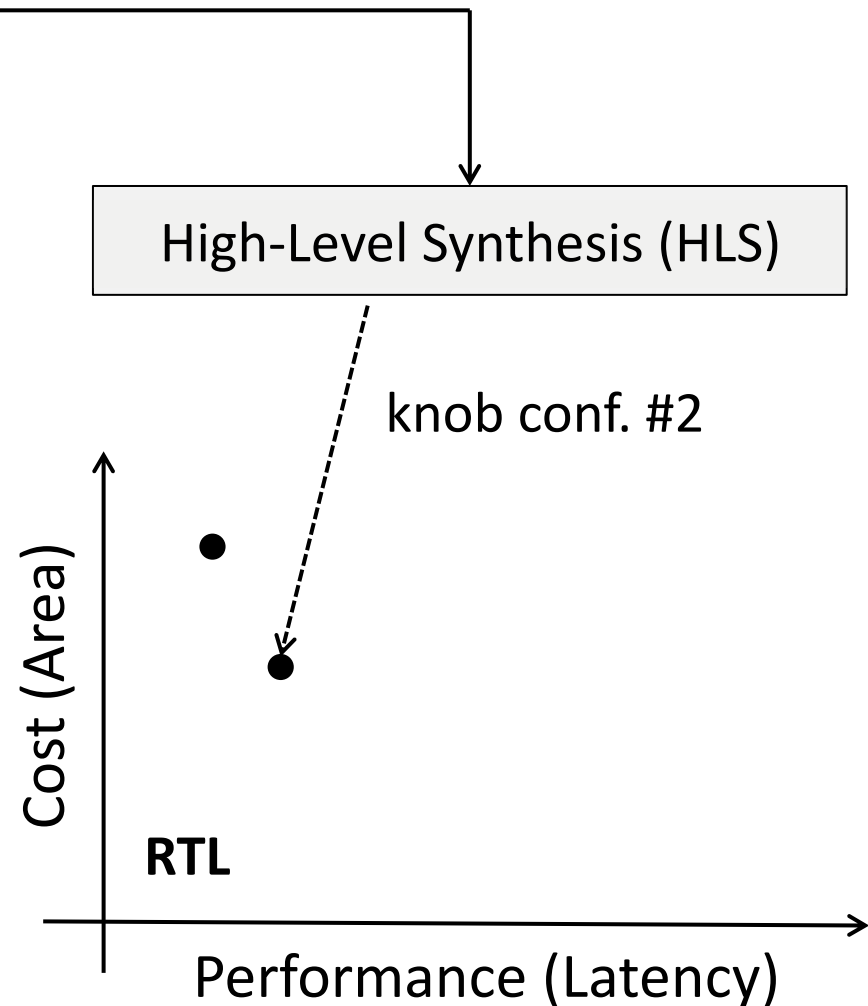
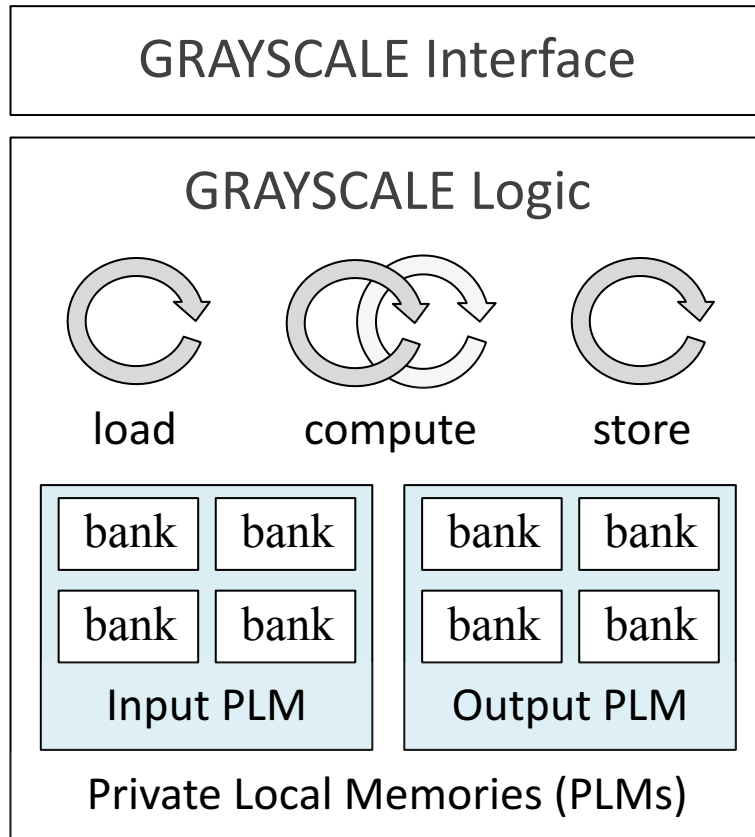
Hardware Accelerators with HLS

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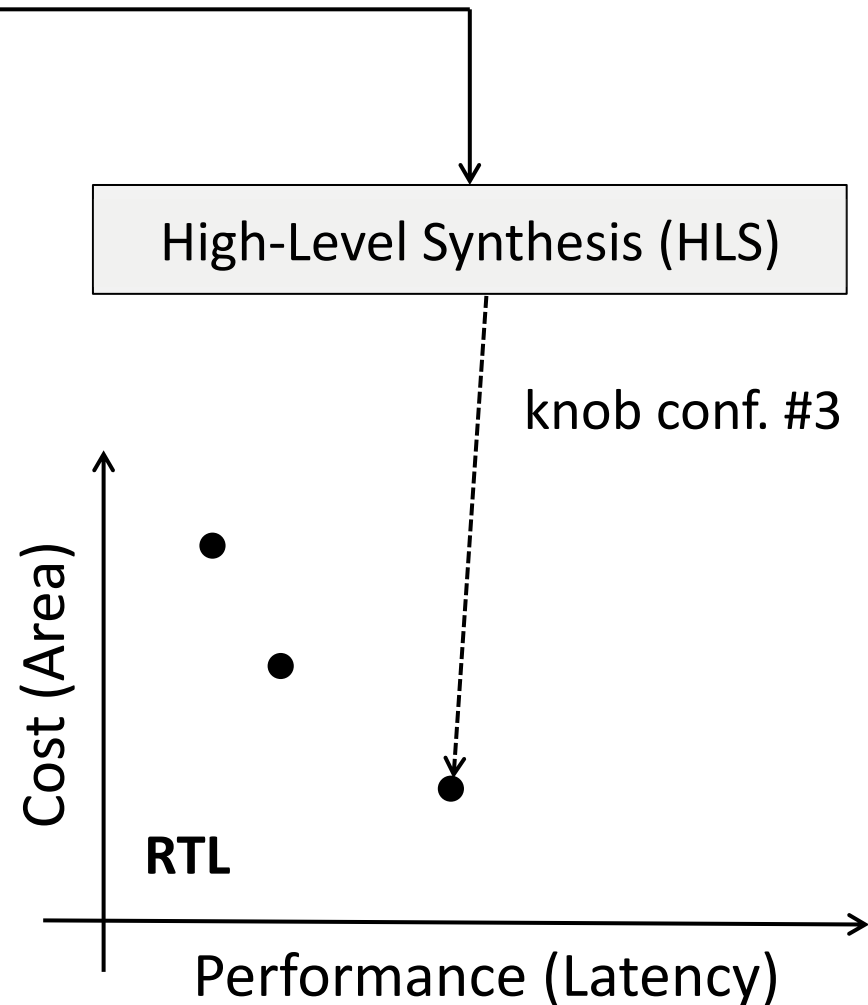
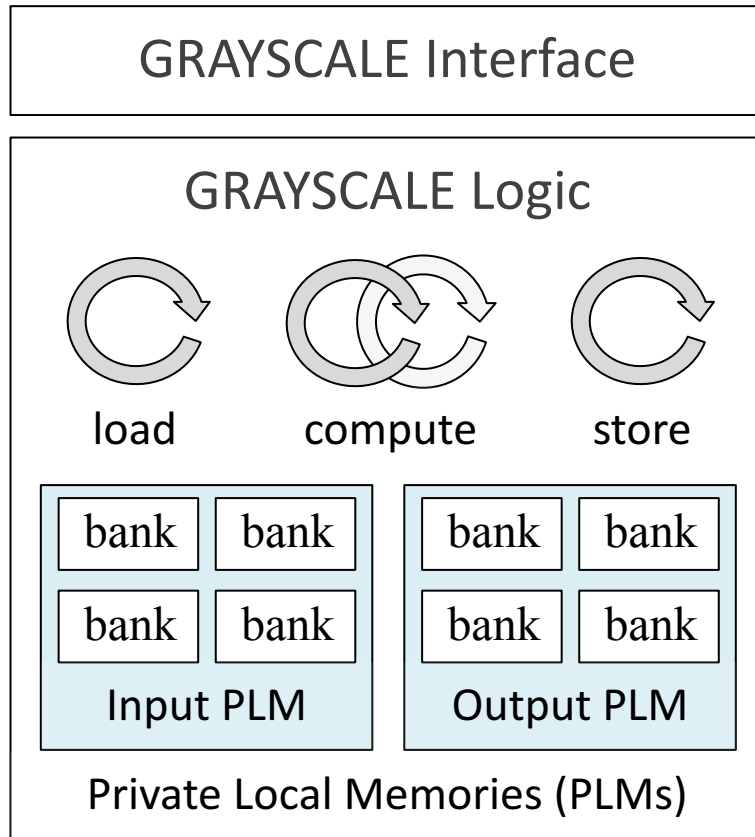
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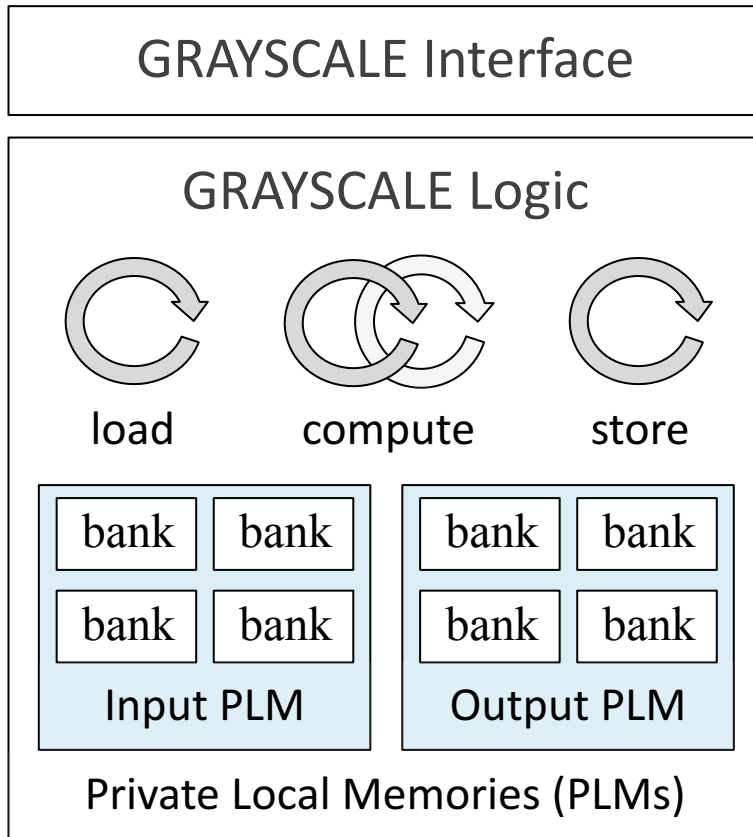
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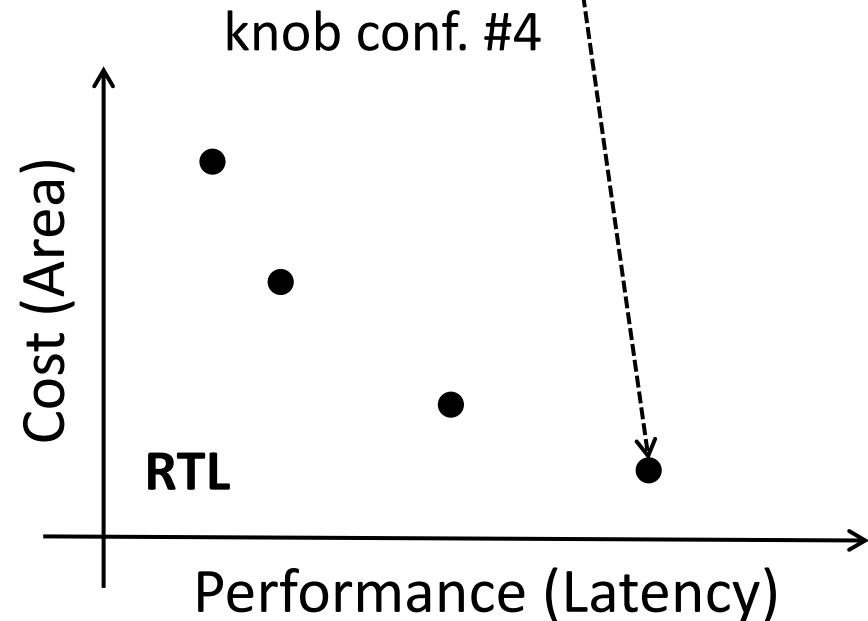


Hardware Accelerators with HLS

SystemC Specification

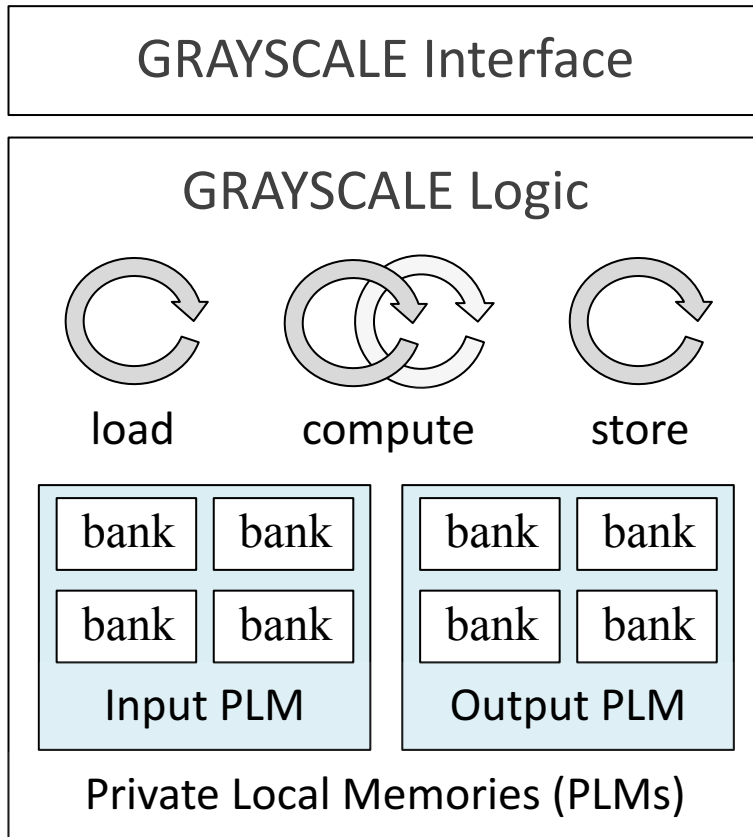


High-Level Synthesis (HLS)

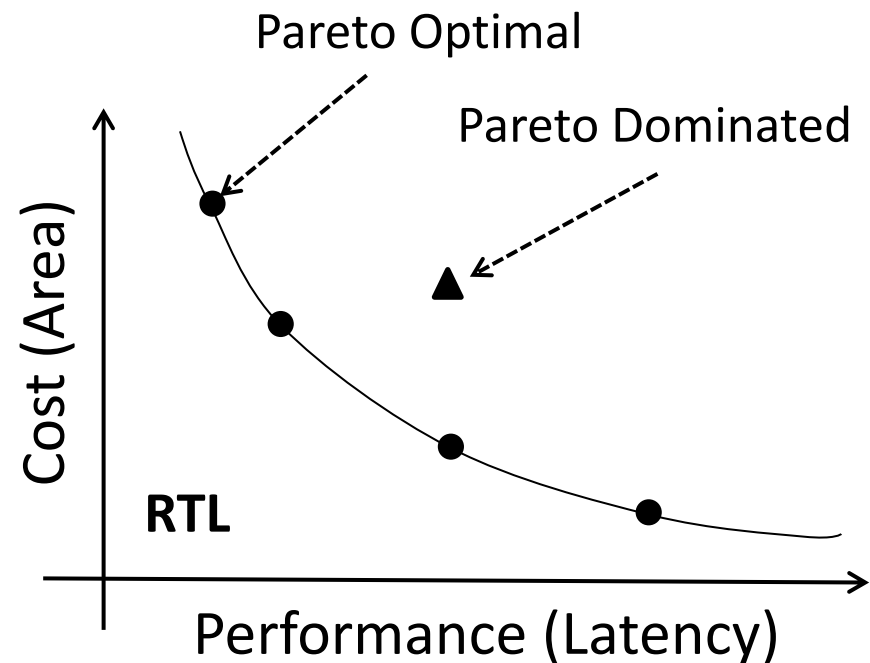


Hardware Accelerators with HLS

SystemC Specification



High-Level Synthesis (HLS)



Standard HLS Knobs

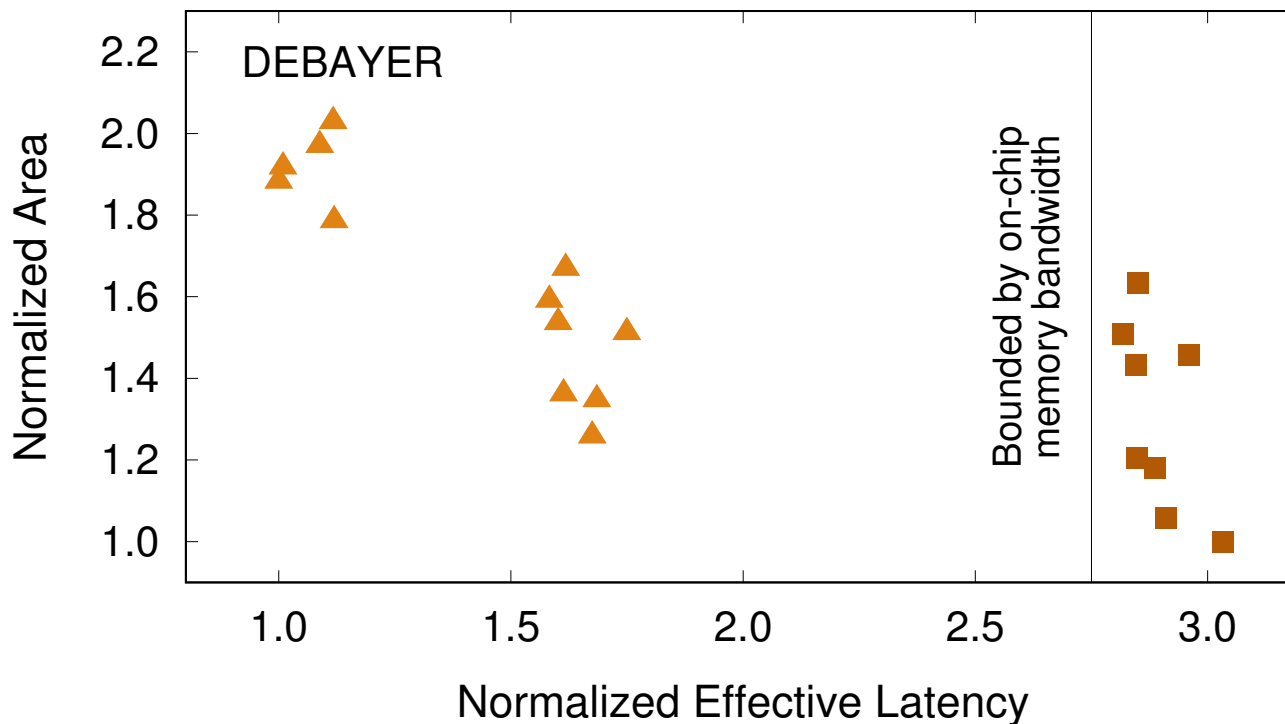
Standard knobs provided by the current HLS tools

| Knob | Settings and Effects |
|--------------------|--|
| Loop manipulations | Unrolls, pipelines or breaks the body of loops |
| Array mappings | Maps arrays to registers or on-chip memories |
| Clock period | Sets the target clock period for synthesis |

- These knobs enable already a rich design-space exploration
 - However, they are not sufficient for exploring accelerators
- ↳ We need other knobs to broaden the exploration

Motivational Example #1

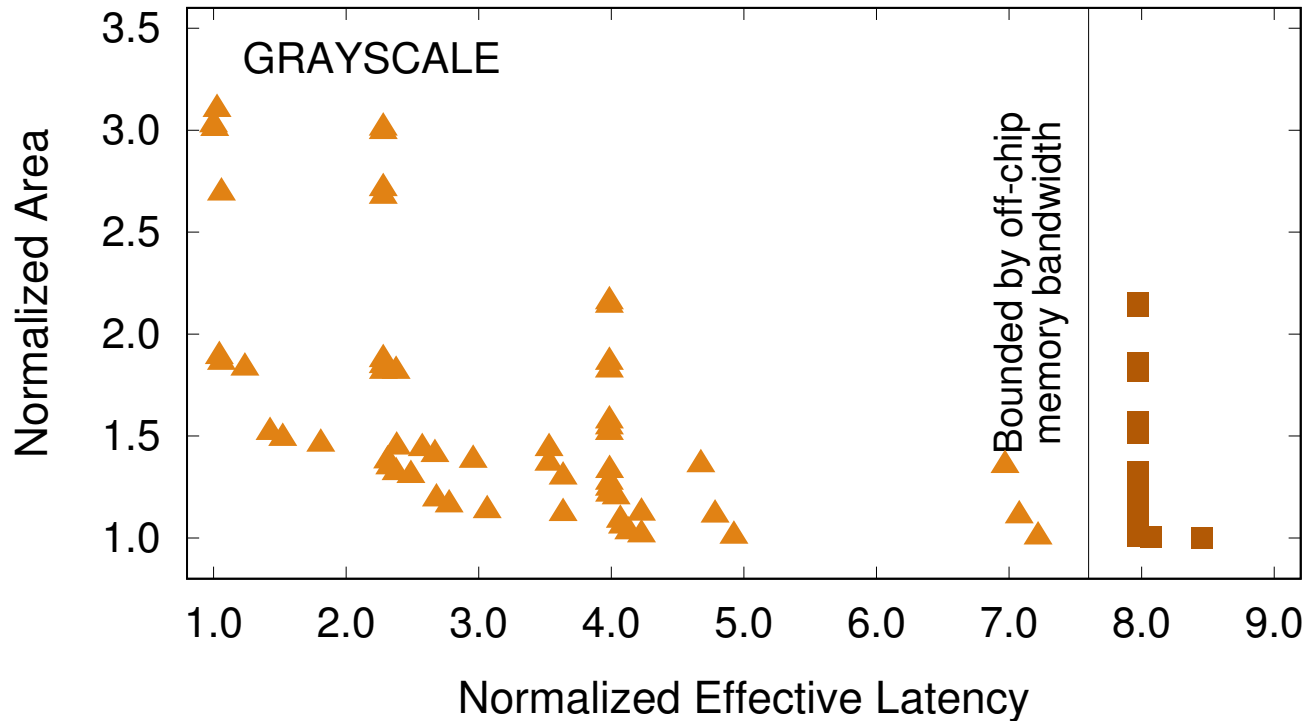
synthesized with the standard knobs ■
synthesized with the proposed knobs ▲



- **Limiting factor**: limited bandwidth to the on-chip memory
- **We need** knobs to tailor the PLM to the accelerator needs

Motivational Example #2

synthesized with the standard knobs ■
synthesized with the proposed knobs ▲



- **Limiting factor:** limited bandwidth to the off-chip memory
- **We need** knobs to operate on the communication interfaces

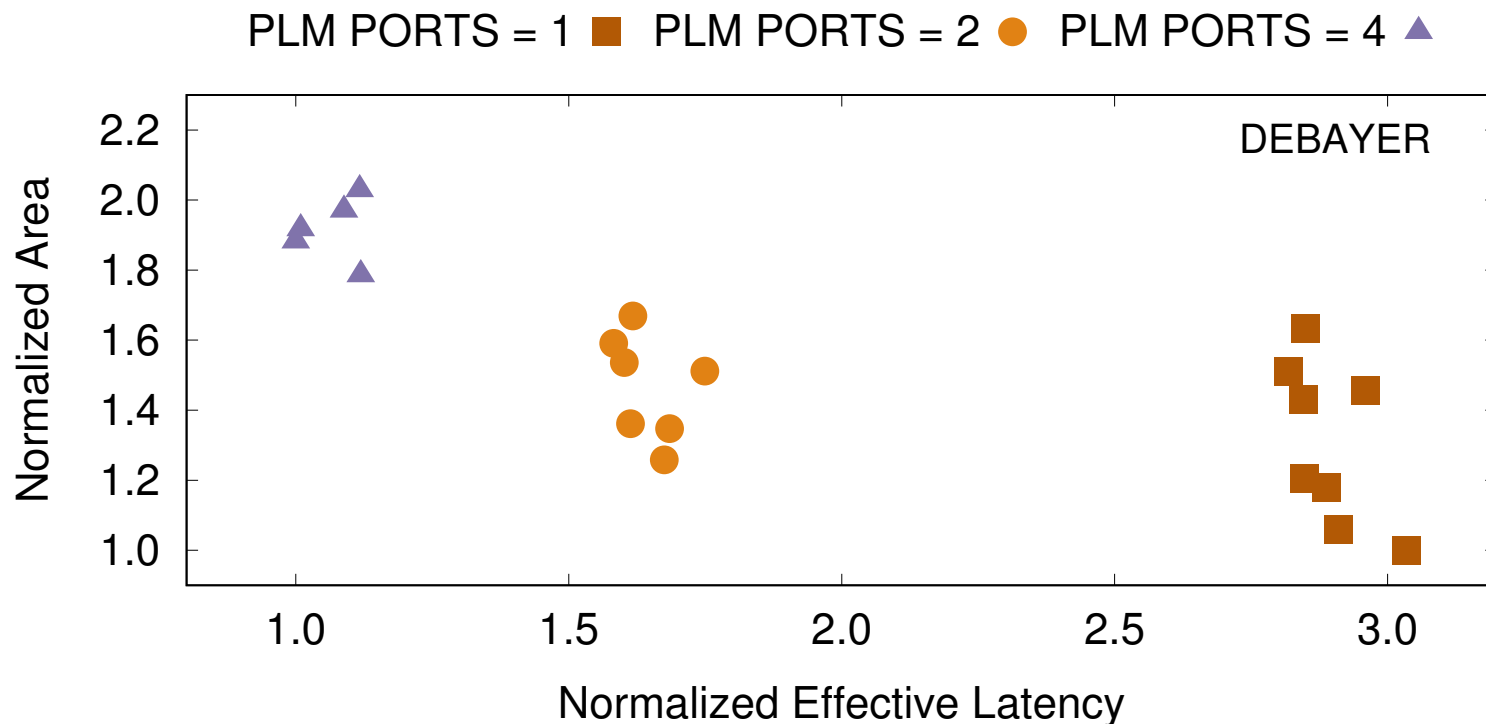
Contributions: Xknobs

eXtended Knobs for High-Level Synthesis

| XKnob | Settings and Effects |
|-----------|---|
| PLM PORTS | Sets the on-chip memory bandwidth |
| DMA WIDTH | Sets the off-chip memory bandwidth |
| DMA CHUNK | Sets the size of the input and output PLM |

Xknob #1: PLM PORTS

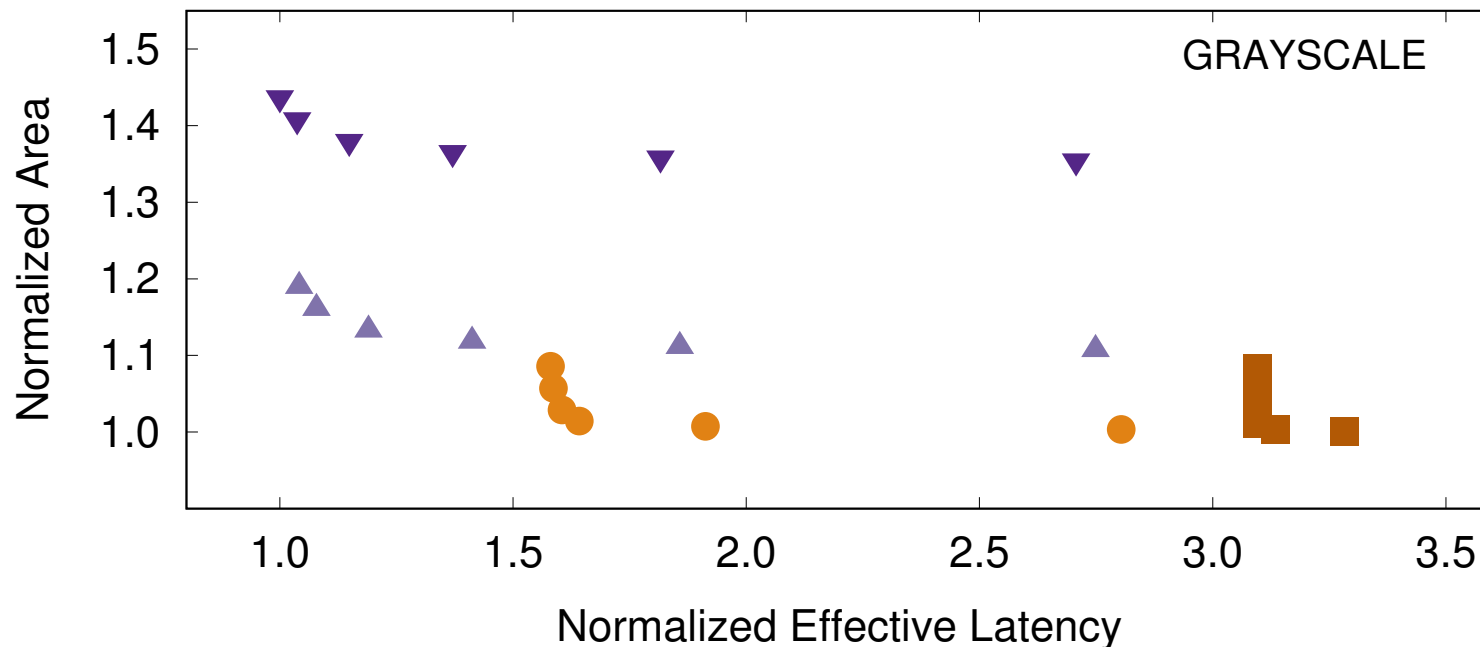
- Sets the number of read/write ports of input/output PLMs
- Higher values of PLM PORTS → more read/write accesses
- Higher values of PLM PORTS → higher area (more banks)



Xknob #2: DMA WIDTH

- Set the size in bits of the DMA communication channels
- Higher values of DMA WIDTH → higher mem. throughput
- Higher values of DMA WIDTH → higher area (more banks)
(higher number of write/read ports of input/output PLMs)

DMA WIDTH = 64 ■ DMA WIDTH = 256 ▲
DMA WIDTH = 128 ● DMA WIDTH = 512 ▼

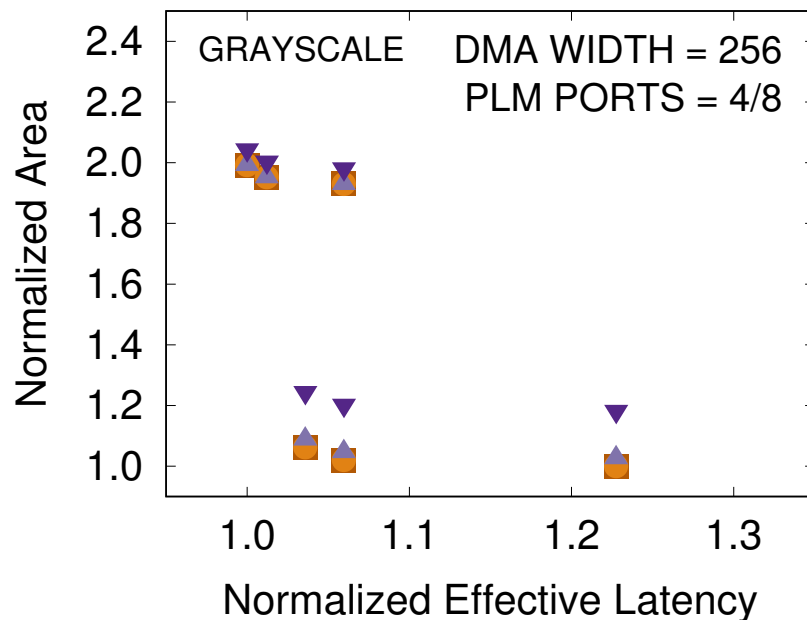


Xknob #3: DMA CHUNK

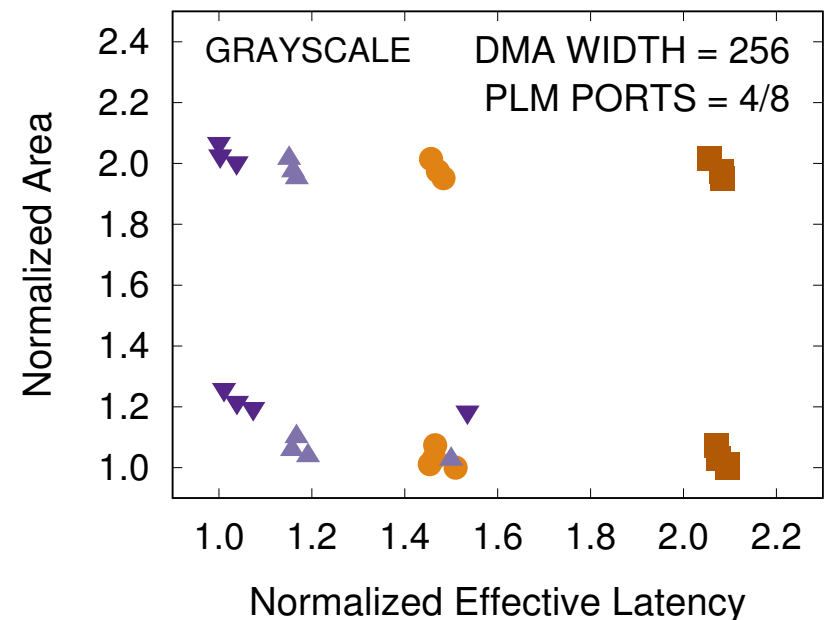
- Set the size of the PLM in multiple of the stored data type
- Higher values of DMA CHUNK → optimized communication
- Higher values of DMA CHUNK → higher area (for the PLM)

DMA CHUNK = 256 ■ DMA CHUNK = 512 ● DMA CHUNK = 1024 ▲ DMA CHUNK = 2048 ▼

without contention



with contention



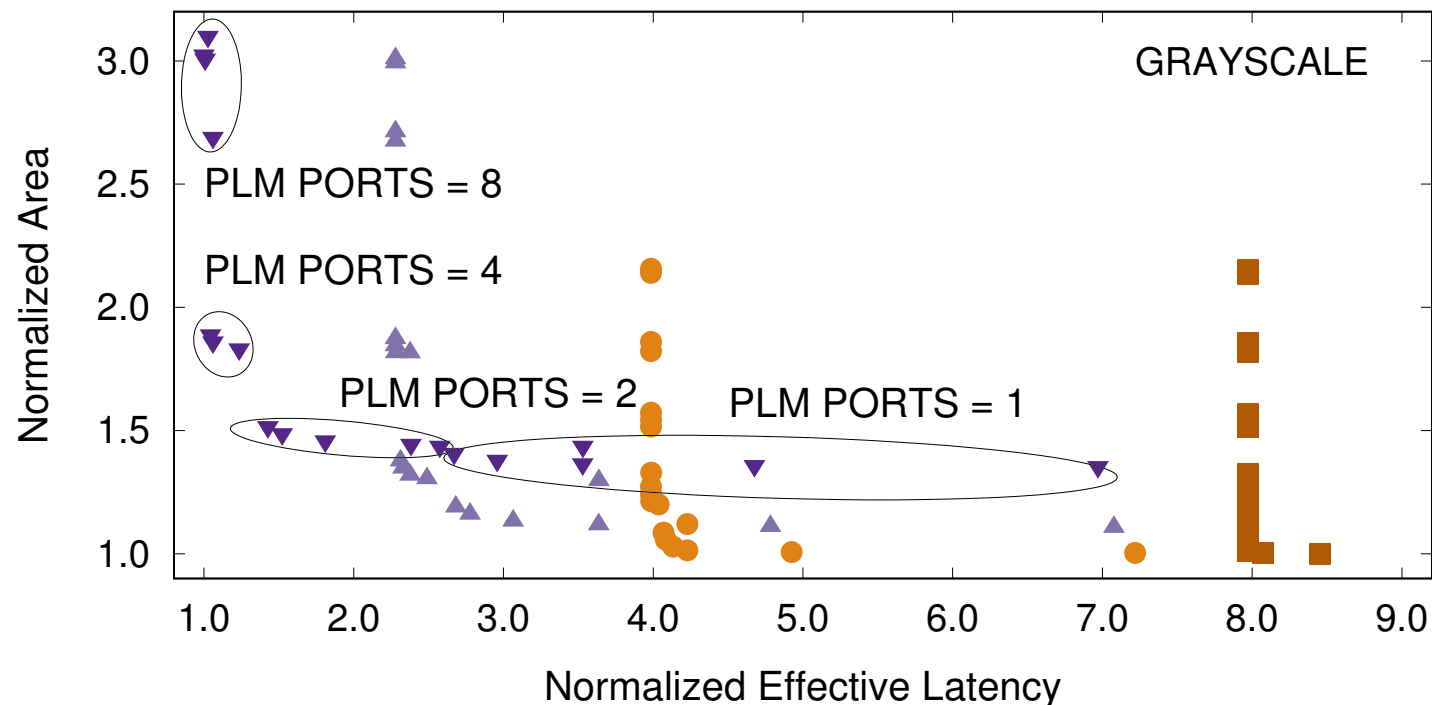
Experimental Results

- We evaluate the combined effects of the **XKnobs** by using:
 - **GRAYSCALE** → accelerator limited by communication
 - **DEBAYER** → accelerator limited by computation
- The other WAMI accelerators behave similarly to either the GRAYSCALE accelerator or the DEBAYER accelerator

Experiment #1

- We consider two **XKnobs**: PLM PORTS and DMA WIDTH

DMA WIDTH = 32 ■ DMA WIDTH = 64 ● DMA WIDTH = 128 ▲ DMA WIDTH = 256 ▼

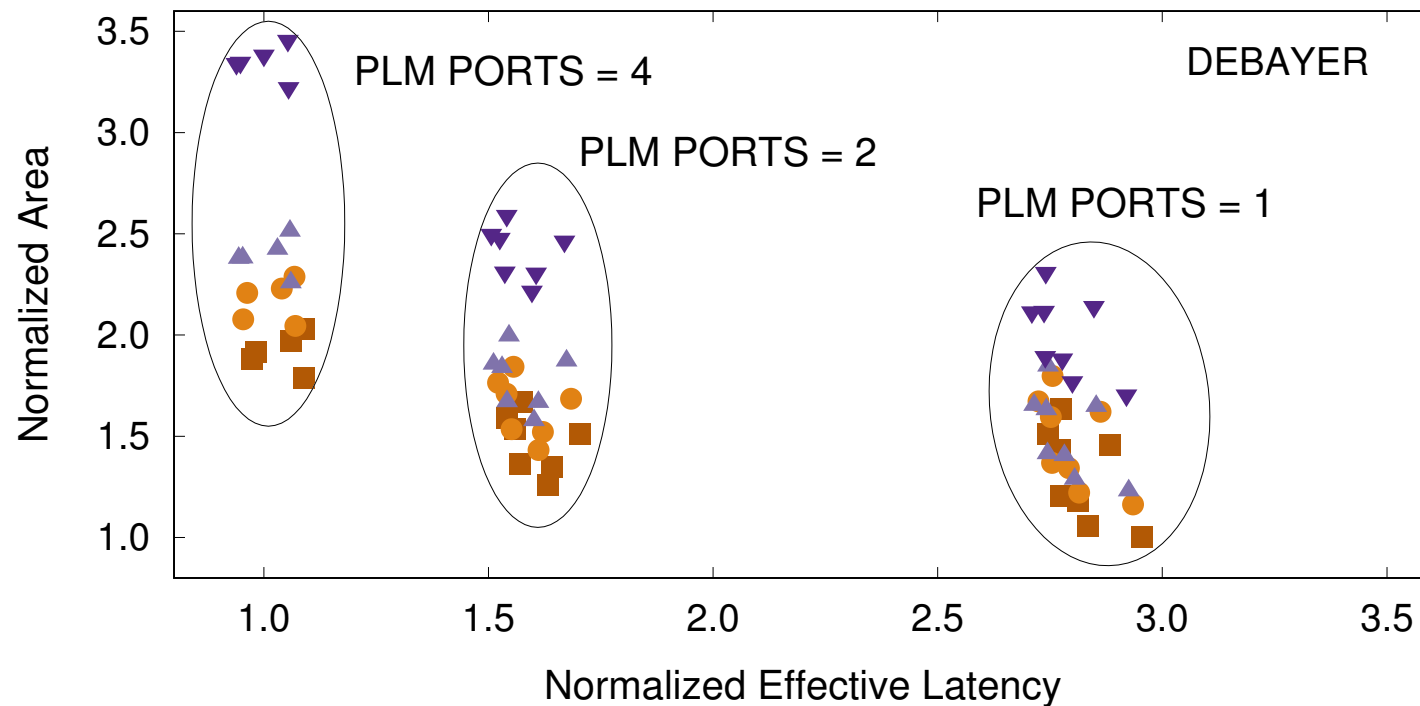


- GRAYSACLE** → accelerator limited by communication

Experiment #1

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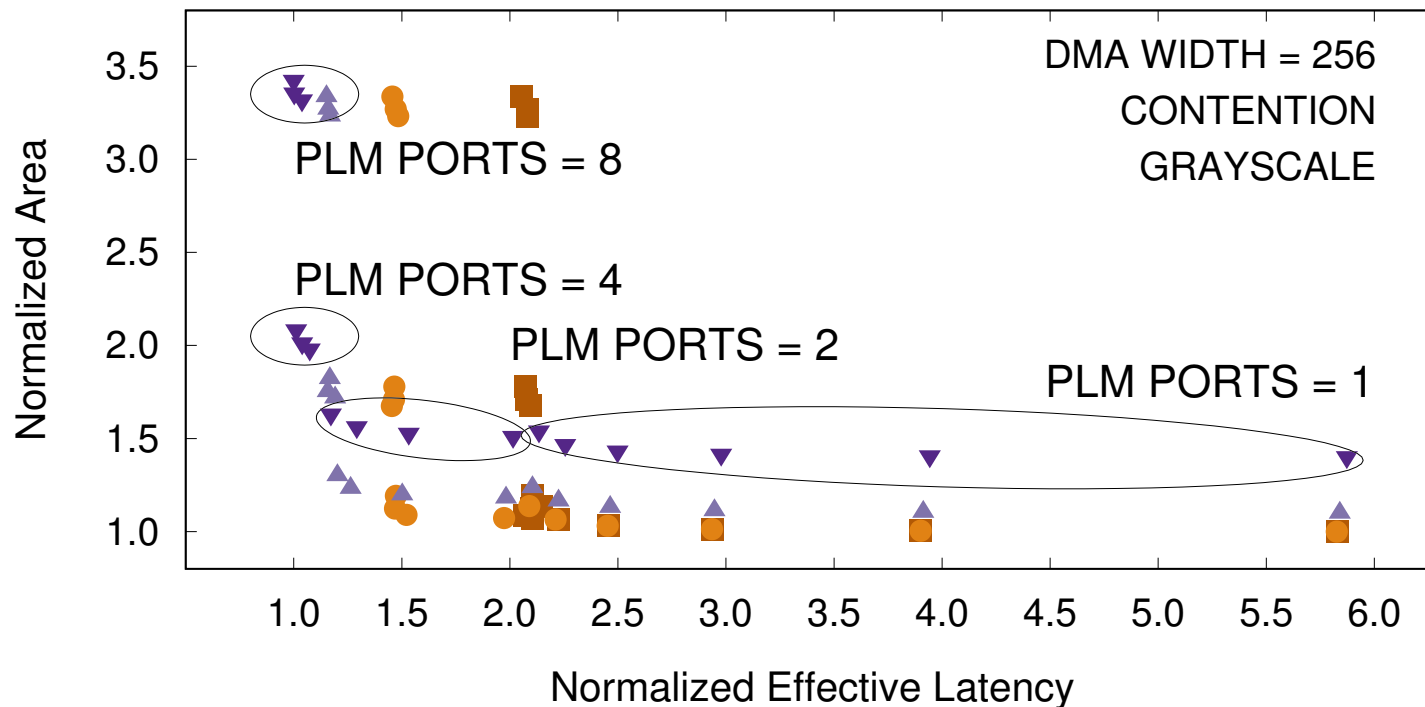


- DEBAYER** → accelerator limited by computation

Experiment #2

- We consider two **XKnobs**: PLM PORTS and DMA CHUNK

DMA CHUNK = 256 ■ DMA CHUNK = 512 ● DMA CHUNK = 1024 ▲ DMA CHUNK = 2048 ▼

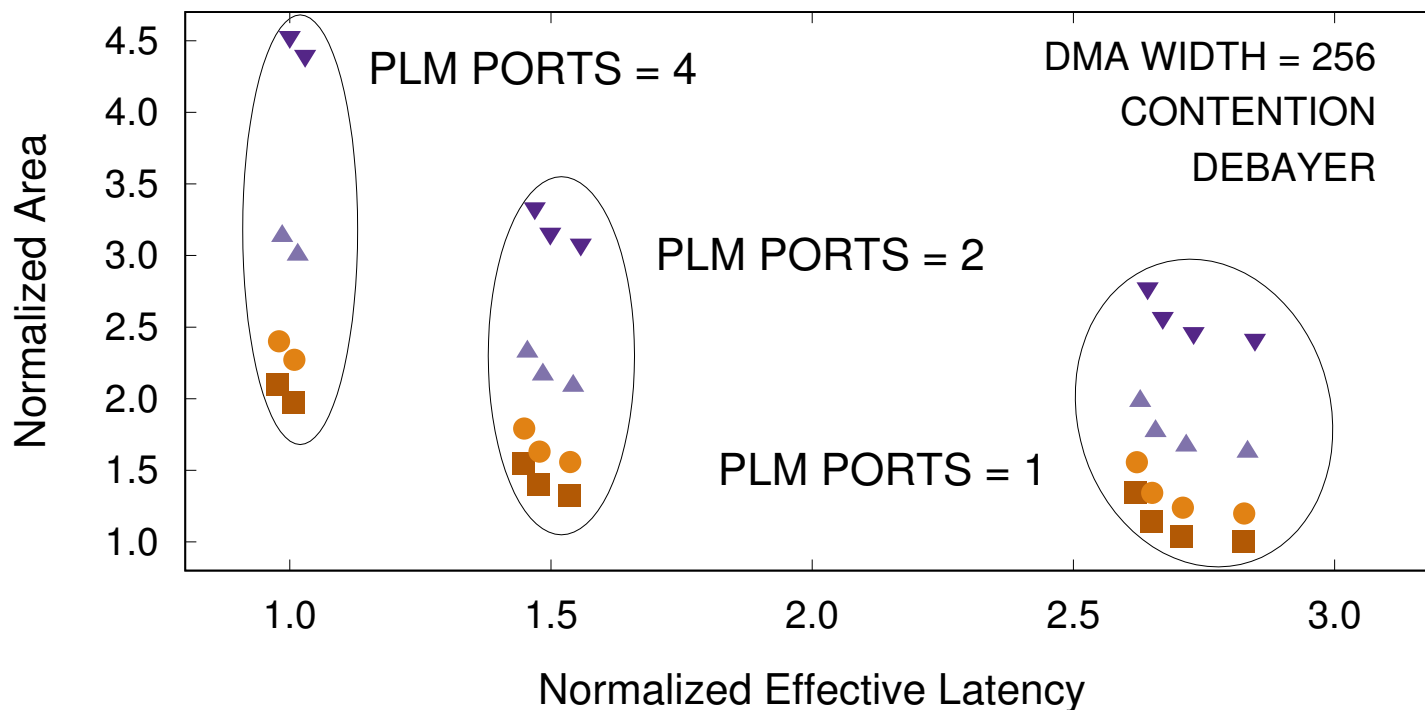


- GRAYSCALE** → accelerator limited by communication

Experiment #2

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DMA CHUNK = 256 ■ DMA CHUNK = 512 ● DMA CHUNK = 1024 ▲ DMA CHUNK = 2048 ▼



- **DEBAYER** → accelerator limited by computation

Concluding Remarks

- We presented the **XKnobs**
 - a set of knobs that aims at extending the standard knobs used in current HLS tools
- For WAMI, the **Xknobs** broaden the design space by up to **8.5x** for performance and **3.5x** for cost
- The **XKnobs** can be integrated in any HLS tools and design-space exploration methodologies to enrich the set of Pareto-optimal implementations of hardware accelerators

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Thank you for the attention!

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Columbia University, NY