Some Professional Highlights: 2008-present

Steven Nowick (7/8/18)

Below is a list of some highlights in the last 10 years, including grants, publications, awards, etc. It is not a complete list -- see CV and research statement for more items and details.

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1. IEEE Fellow (2009)

Circuits and Systems Society (CAS),
"For contributions to asynchronous and mixed-timing integrated circuits and systems"

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2. Chair/Founder, "Computing Systems for Data-Driven Science" center,
Data Science Institute, Columbia University **(2015-present)**

Founded a major new research center at Columbia University, as part of its Data Science Institute, with 40 faculty and senior research members. Originally established as a working group (*"Frontiers in Computing Systems"*), it was approved in May 2018 as a university research center (see story).

The center brings together researchers in (i) *massive-scale computing systems* (hardware, software, databases, emerging paradigms [quantum computing, accelerator-based architectures, asynchronous design, hybrid analog-digital computing]), (ii) *data science*, and (iii) critical and diverse *application areas using large-scale computing, in science, medicine and engineering* (climate/ocean science, medical informatics, computational genomics, astrophysics, large-scale engineering [energy grid, aging infrastructure]). The goal of the center is to foster synergy and collaborations, as well as major research projects and educational initiatives, at the nexus of these three areas.

As part of our activity, organized a regional inaugural symposium (March 2017) with 150 participants, called *"Frontiers in Computing Systems"*, including a keynote by the chief architect of IBM's "Watson" system, and invited talks by leading speakers and panelists from D.E. Shaw Research, NASA Goddard Institute for Space Studies, Simons Foundation (Flatiron Institute) and the National Science Foundation. (See story and agenda.)

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3. Chair/Co-Founder, Columbia Computer Engineering Program (chair, 2008-2013)

Co-founded program (1994), jointly run by CS and EE departments, and served as chair from 2008-2013 (re-elected 2011 for 2nd term). During this period, the BS program grew from 23 to 57 majors, and the MS applications increased from 76 to 285 (Fall admission), with 64 total current MS students enrolled.

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4. Columbia Engineering (SEAS) Alumni Distinguished Faculty Teaching Award (2011)

Best teacher award in Columbia Engineering School (2 per year, out of approximately 170 faculty). Selected by undergraduate students, with consultation of alumni.

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5. Technology Transfer: AMD Corporation (2015-2017)

By invitation from Advanced Micro Devices (AMD), we experimentally migrated our recent high-performance and low-energy asynchronous network-on-chip (NoC) switch into their industrial design flow, and conducted the first direct ("apples-to-apples") experimental comparison between an asynchronous NoC design and a leading industrial synchronous NoC chip in identical advanced technology (14nm FinFET). The asynchronous design was led by our group, in collaboration with the University of Ferrara (Italy), and the migration was led by Nowick's PhD student, Weiwei Jiang. As part of this project, Jiang also developed a new efficient approach for asynchronous virtual channels, with a joint patent filed by AMD. The synchronous chip was manufactured by AMD and is currently used in several commercial products.

Experimental results, on a single network node, show the asynchronous NoC design performed significantly better when compared to the clock-gated synchronous chip – 55% less area with 28% lower latency – along with a 58% reduction in active power and an 88% reduction in idle power.

The experiments were conducted at AMD Research, in collaboration with AMD Fellows Greg Sadowski and Wayne Burleson. *"This was a highly-productive and effective collaboration between Steve Nowick's group and AMD,"* said Sadowski. *"His group's asynchronous network-on-chip has great potential for our future systems, once the automated tool flow is developed."*

This evaluation was published in the 2017 ACM/IEEE Design, Automation and Test in Europe (DATE) Conference.

In new developments, we now provide a complete and automated synthesis CAD tool flow for asynchronous NoC's, using synchronous commercial tools, was published in the 2017 IEEE Async Symposium.

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6. Major Grants

Awarded two competitive medium-scale NSF awards:

"*Power-Adaptive, Event-Driven Data Conversion and Signal Processing Using Asynchronous Digital Techniques.*" Total: $1,062,605, PI: Yannis Tsividis (EE, Columbia), co-PI: Steven Nowick (CS, Columbia). My portion: $500,000 (approx.). [2010-2015]

topic area: continuous-time digital signal processors (CT-DSP's)

"*Design and Tools for Easy-to-Program Massively Parallel On-Chip Systems: Deriving Scalability Through Asynchrony.*" Total: $921,686, PI: Steven Nowick (CS, Columbia), co-PI: Uzi Vishkin (ECE, U. Maryland). My portion: $461,000. [2008-2013]

topic area: asynchronous/GALS networks-on-chip (NoC's) for high-performance chip multiprocessors

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7. Smaller Grants *(selected)*

Awarded two competitive small-scale NSF awards:

"*An Asynchronous Network-on-Chip Methodology for Cost-Effective and Fault-Tolerant Heterogeneous SoC Architectures.*" Total: $420,000, PI: Steven Nowick (CS, Columbia). [2015-2018]

"*Designing Low-Latency and Robust Interconnection Networks with Fine-Grain Dynamic Adaptivity Using Asynchronous Techniques.*" Total: $450,000, PI: Steven Nowick. [2012-2016]

topic area: asynchronous/GALS networks-on-chip (NoC's)

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8. Professional Society Activities

(i) *Selection Committee Chair (2012-2013),* ***ACM/SIGDA "Outstanding PhD Dissertation in EDA Award"***

(ii) *Jury Member (2017),* ***ACM "India Doctoral Dissertation Award"***

(iii) *Selection Committee Member (2014-2015),* ***ACM/IEEE "A. Richard Newton Technical Impact Award in Electronic Design Automation"***

(iv) *Member (2012),* ***IEEE Fellows Evaluation Committee (Computer Society).***

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9. Government Agency Activities

(i) *Invited Participant (March 2015),* ***NSF Workshop on Ultra-Low Latency Wireless Networks***

Invited to a national study group, sponsored by NSF, with fewer than 40 participants, on the future of wireless technology to achieve extreme low-latency communication, targeting both macro-level and micro-level (i.e. on-chip) networks. I participated in writing a white paper documenting the outcomes of the workshop, that is expected to be used by NSF for defining future funding initiatives and research directions (see http://inlab.lab.asu.edu/nsf/#).

(ii) *Invited Participant (August 2014),* ***NSF/DARPA/DOE/NASA Workshop on System-on-Chip Design for High-Performance Computing ("SoC for HPC")***

Invited to national study group with only 32 total participants (government, academia, industry), including only 10 invited academics, on the future of designing cost-effective high-performance computing systems for both Big Data and consumer applications. The focus was on adapting system-on-chip (SoC) design techniques and tool flows to develop cost-effective future-generation many-core parallel computers. I presented my work on asynchronous and GALS networks-on-chip.

The workshop was organized by a multi-agency team from NSF, DOE, DARPA, NASA, and Sandia and Lawrence Berkeley Laboratories (see https://sites.google.com/a/lbl.gov/socforhpc/).

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10. Conference Activities

(i) *Topic Area Co-Chair (2015):* **ACM/IEEE DATE Conference,** *Program Committee,* "Network on Chip" area

(ii) *Selection Committee Member (2014):* **William J. McCalla Best Paper Award: ACM/IEEE ICCAD Conference**

(iii) *Subcommittee Chair (2011-2013):* **ACM/IEEE DAC Conference,** *Program Committee,* "High-Level and Logic Synthesis, Circuit-Level Optimization, and FPGA" area

(iv) *Topic Area Chair (2009-10)/Co-Chair (2008):* **ACM/IEEE DATE Conference,** *Program Committee,* "Logic and Technology-Dependent Synthesis for Deep-Submicron Circuits" area

(v) *Selection Committee Member (2010)*: **Best Paper Award: ACM/IEEE DAC Conference**

Other: PC Member for 7 conferences/workshops: DAC, DATE, NOCS, Async, IWLS, INA-OCMC, FMGALS

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11. Journal Activities

(i) *Associate Editor (2010-present),* **ACM Journal on Emerging Technologies in Computing Systems** (three 3-year terms)

(ii) *Associate Editor (2015-present),* **IEEE Design and Test Magazine**

(iii) *Associate Editor (2015-16, 2001-07),* **IEEE Transactions on VLSI Systems** (four 2-year terms)

(iv) *Associate Editor (2003-11),* **IEEE Transactions on Computer-Aided Design** (four 2-year terms)

(v) *Guest Co-Editor,* **ACM Journal on Emerging Technologies in Computing Systems**, *special issue on asynchrony in system design,* vol. 7:4, December 2011.

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12. Best Paper Awards

(i) ***Best Paper Award (logic & circuit design track)*** *(2012):* **IEEE ICCD Conference**
C. Vezyrtzis, Y. Tsividis and S.M. Nowick, "*Designing Pipelined Delay Lines with Dynamically-Adaptive Granularity for Low-Energy Applications*."

(ii) ***Best Paper Finalist*** *(2017):* **ACM Network-on-Chip (NOCs) Symposium**
K. Bhardwaj and S.M. Nowick, "*Achieving Lightweight Multicast in Asynchronous NoCs Using a Continuous-Time Multi-Way Read Buffer."*

(iii) ***Best Paper Finalist*** *(2015):* **IEEE Async Symposium**
G. Miorandi, D. Bertozzi and S.M. Nowick, "*Increasing Impartiality and Robustness in High-Performance N-Way Asynchronous Arbiters."*

(iv) ***Best Paper Finalist*** *(2013):* **ACM/IEEE DATE Conference**
A. Ghiribaldi, D. Bertozzi and S.M. Nowick, "*A Transition-Signaling Bundled Data NoC Switch Architecture for Cost-Effective GALS Multicore Systems.*"

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13. Research/Educational Outreach: Overview Articles on State-of-the-Field

With co-author Montek Singh (my former PhD students), I authored two highly visible articles on the state of the field in asynchronous design. The contribution of this educational outreach, to the larger research community, is to provide a unique and up-to-date snapshot, history, and technical overview, of asynchronous design.

The first article, in two parts in IEEE Design & Test Magazine (May/June 2015), including 114 references, is the only asynchronous overview article in the last 15 years that broadly covers modern advances in asynchronous computer architecture, networks-on-chip, neuromorphic computing, testing and design-for-testability, CAD tool flows, and diverse emerging application areas (handling extreme environments, energy harvesting, ultra-low-energy systems, continuous-time DSP's, use with new technology [flexible electronics, quantum cellular automata]).

This two-part paper was on the 'top-download' list of IEEE Design & Test Magazine for nearly two years.

The second article, in IEEE Design & Test Magazine (September/October 2015), is the only existing overview paper surveying and providing technical foundations on high-performance asynchronous pipelines. Since these pipelines have been used in leading designs (Intel/Fulcrum's Ethernet switch chips, Achronix's FPGA's, etc.), this overview provides a unique contribution to capturing the history and leading examples in this important area.

S.M. Nowick and M. Singh, "Asynchronous Design - Part 1: Overview and Recent Advances," IEEE Design & Test of Computers, vol. 32(3), pp. 5-18, 2015.
S.M. Nowick and M. Singh, "Asynchronous Design - Part 2: Systems and Methodologies," IEEE Design & Test of Computers, vol. 32(3), pp. 19-28, 2015.

S.M. Nowick and M. Singh, "High-Performance Asynchronous Pipelines: an Overview," IEEE Design and Test of Computers, vol. 28(5), pp. 8-22, 2011.

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14. Invited Talks

23 invited talks to academia, industry and keynotes, from 2009-2018: AMD Research (*twice*), IBM T.J. Watson, Intel Labs, NASA Goddard Space Flight Center, D.E. Shaw Research, ACM SLIP-15 Workshop, NSF/DARPA/DOE/NASA "SoC for HPC" Workshop (see #9 above), CMU, Stanford, EPFL (*twice*), Universita di Bologna, Cornell/Cornell Tech, Georgia Tech, Duke, CEA-LETI, University of Massachusetts (Amherst), University of Toronto, Texas A&M (*twice*), Portland State, University of Texas (Austin).

These include **the keynote presentation** at the 17th ACM/IEEE System Level Interconnection Prediction (SLIP) Workshop (2015), and an invited talk to the **Computer Engineering Eminent Scholar Seminar series** at Texas A&M University (2013).
