Practical Memory Safety

Mohamed Tarek Ibn Ziad

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Guest Lecture at CU Boulder - October 31st, 2022

- Research Scientist @ NVIDIA
 - Member of the Architecture Research Group (ARG).

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 - Member of the Computer Architecture and Security Technologies Lab (CASTL)
 - Hardware-Software Co-design for Practical Memory Safety
 - Supervisor: Simha Sethumadhavan

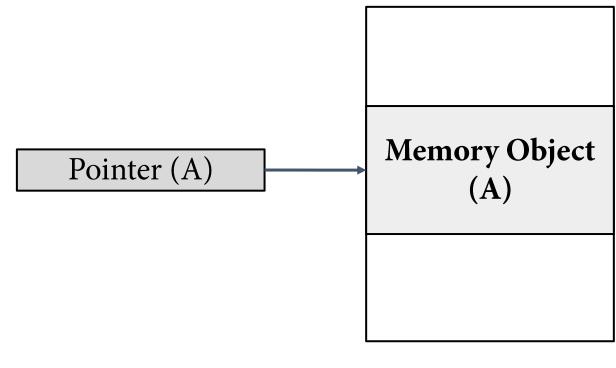
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Today's Talk!

A program property that guarantees memory objects

can only be accessed:



Memory

A program property that guarantees **memory objects** can only be accessed:

• Between their intended bounds,

Pointer (A)

Memory Object
(A)

Memory

A program property that guarantees **memory objects** can only be accessed:

· Between their intended bounds,

• During their lifetime, and

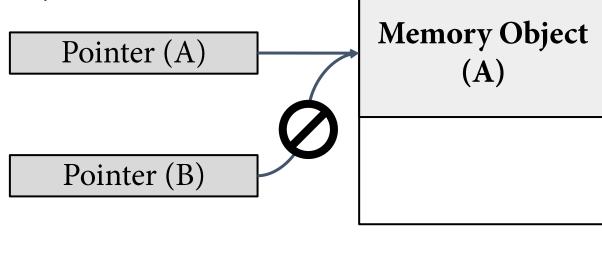
Pointer (A)

Memory Object
(A)

Memory

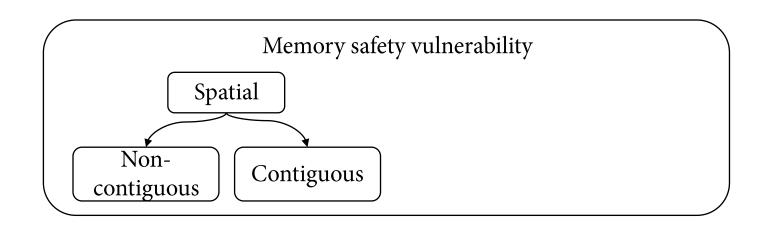
A program property that guarantees **memory objects** can only be accessed:

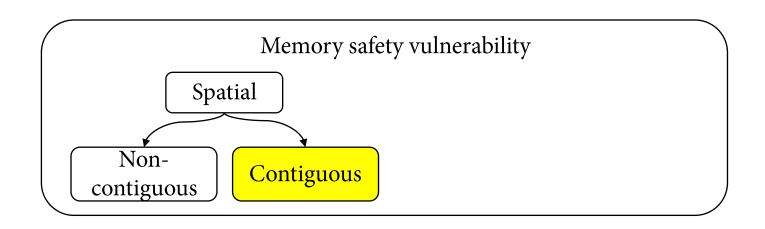
- · Between their intended bounds,
- During their lifetime, and
- Given their original (or compatible) type.

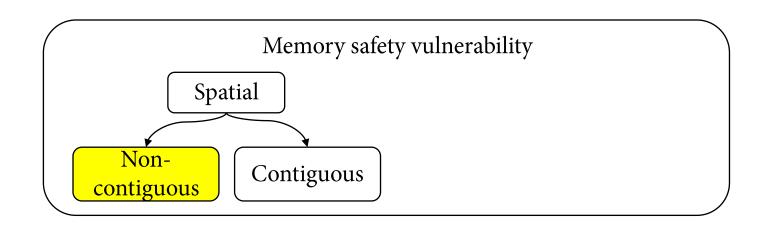


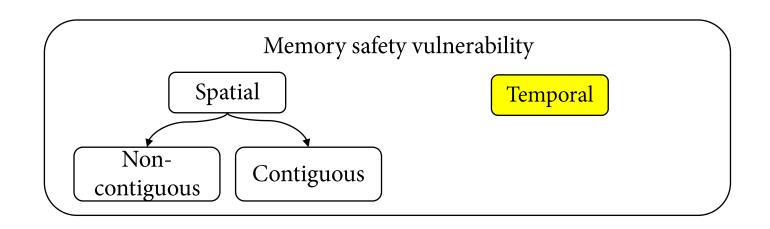
Memory safety vulnerability

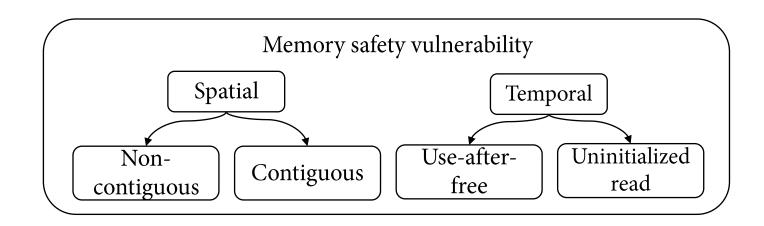
Spatial

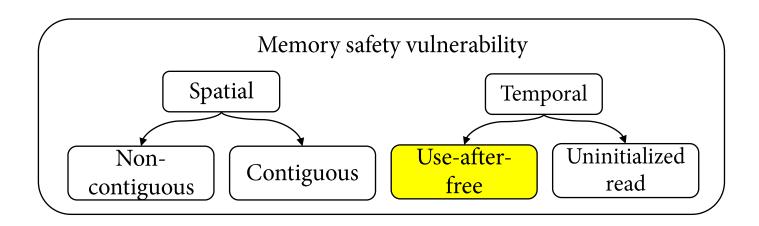


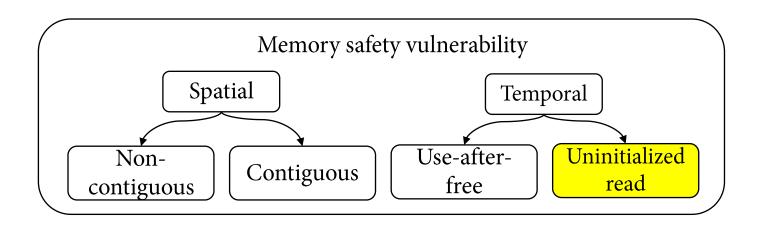


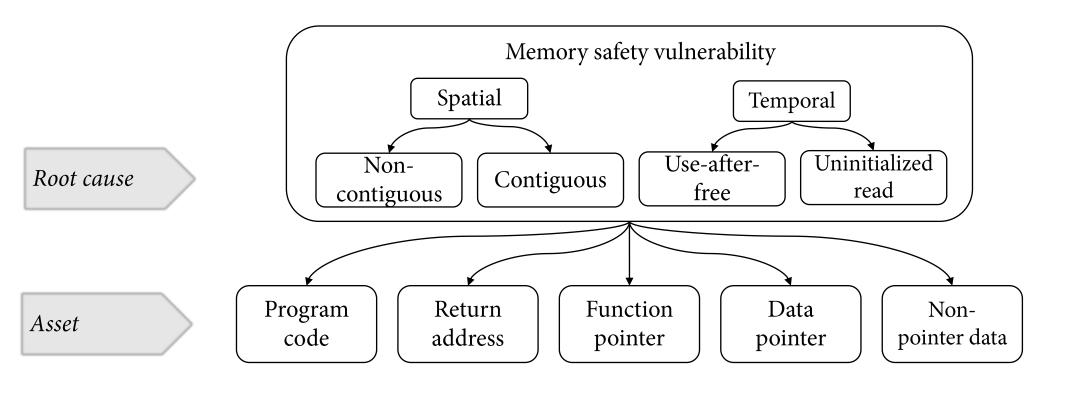


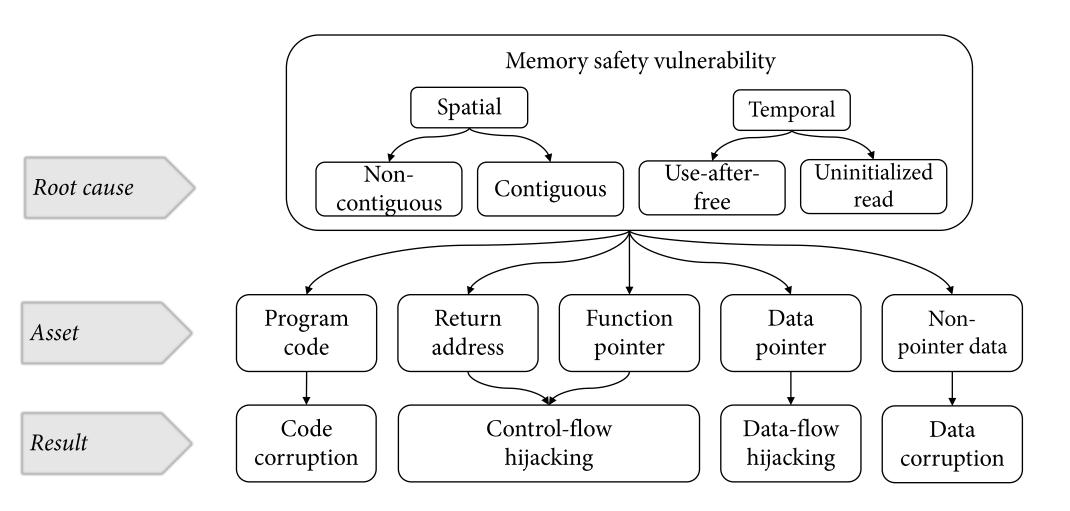


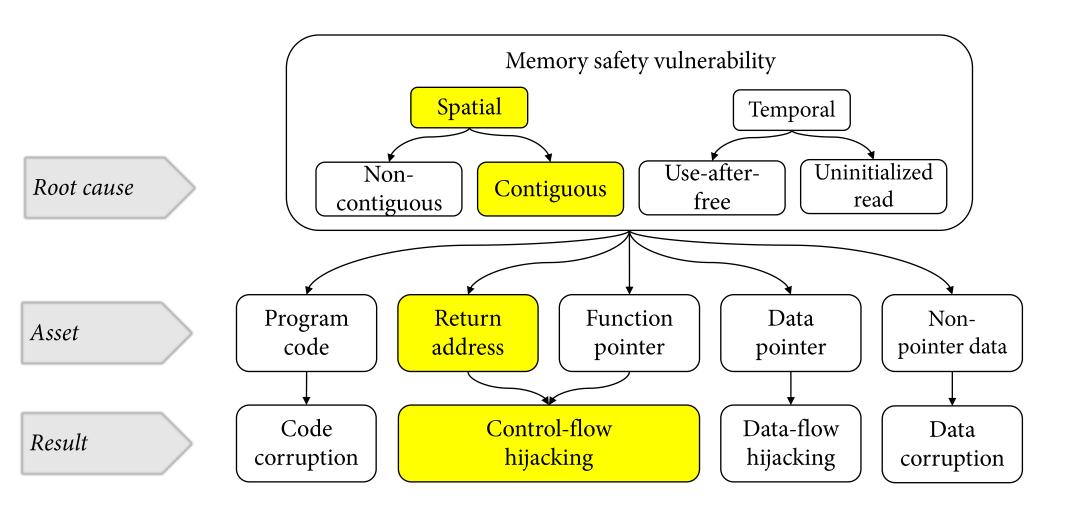


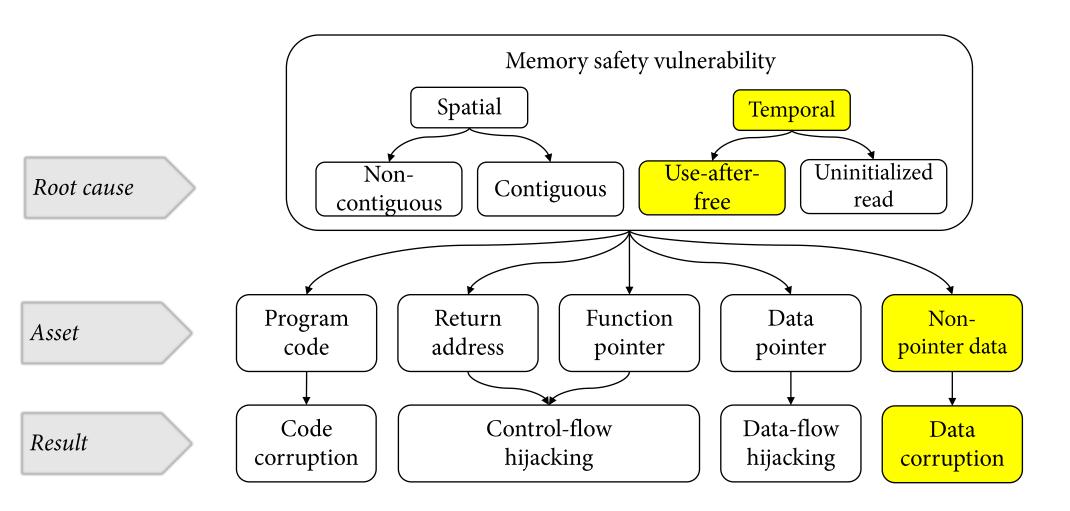












Why is memory safety a concern?



-

Computing Sep 6

Apple says China's Uighur Muslims were targeted in the recent iPhone hacking campaign

The tech giant gave a rare statement that bristled at Google's analysis of the novel hacking operation.

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EDITOR'S PICK | 42,742 views | Nov 21, 2018, 07:00am

Exclusive: Saudi Dissidents Hit With Stealth iPhone Spyware Before Khashoggi's Murder

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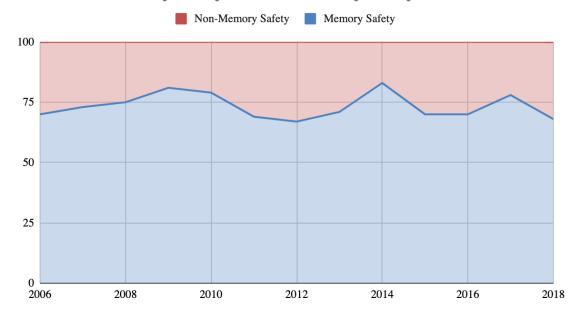
The New Hork Times

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WhatsApp Rushes to Fix Security Flaw Exposed in Hacking of Lawyer's Phone Exclusive: Saudi Dissidents Hit With Stealth iPhone Spyware Before Khashoggi's Murder

Prevalence of Memory Safety Vulns

Memory safety vs. Non-memory safety CVEs



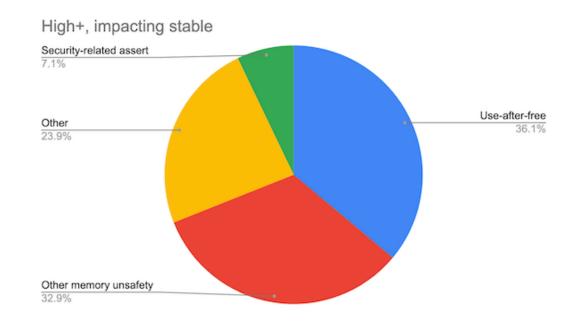
Microsoft Product CVEs between 2006-2018

Prevalence of Memory Safety Vulns

Memory safety vs. Non-memory safety CVEs



Microsoft Product CVEs between 2006-2018



Chromium high severity security bugs between 2015-2020

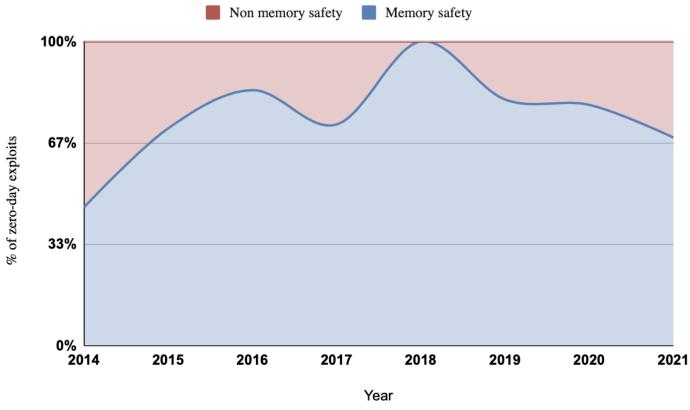


ATTACKERS

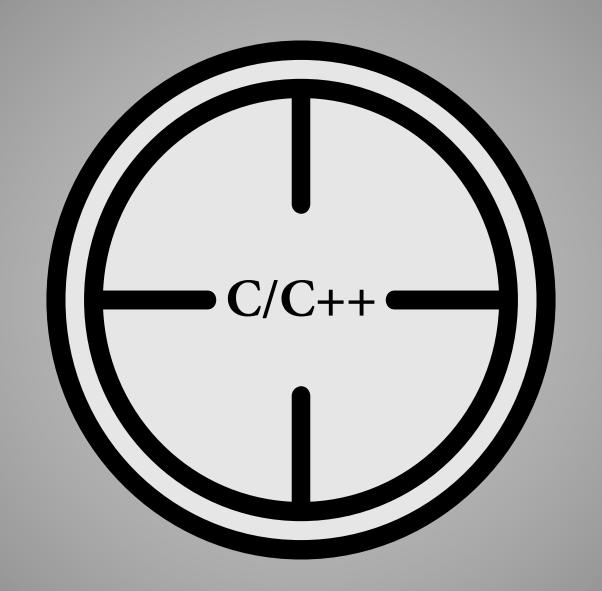


MEMORY SAFETY

Attackers prefer Memory Safety Vulns



% of Zero-day "in the wild" exploits from 2014-2021





















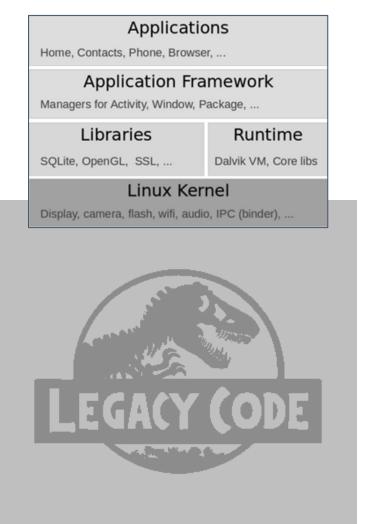
Applications Home, Contacts, Phone, Browser, ... Application Framework Managers for Activity, Window, Package, ... Libraries SQLite, OpenGL, SSL, ... Runtime Dalvik VM, Core libs Linux Kernel Display, camera, flash, wifi, audio, IPC (binder), ...

C/C++ is here to stay!







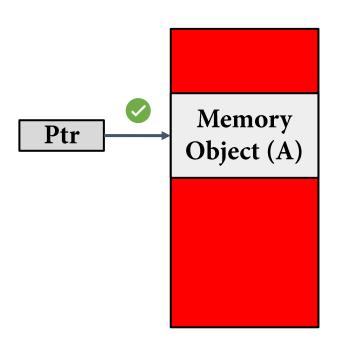


Memory Blocklisting

Memory Permitlisting

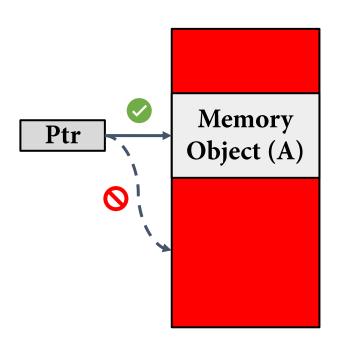
Memory Blocklisting

Memory Permitlisting



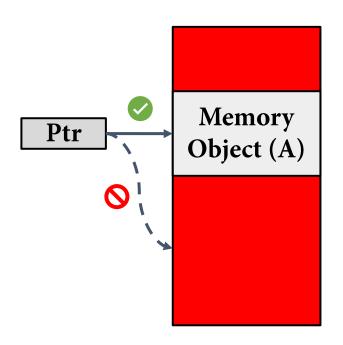
Memory Blocklisting

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Memory Blocklisting

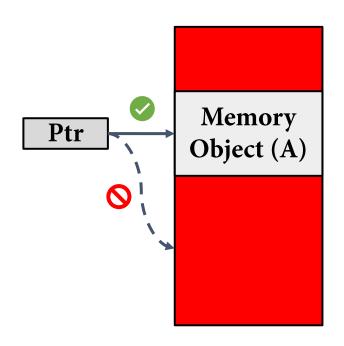
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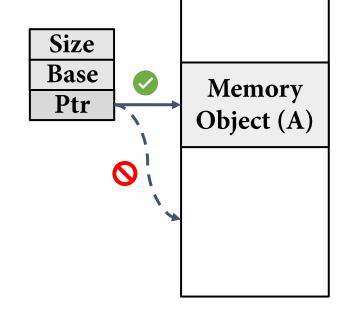


e.g., Google's Address Sanitizer

Memory Blocklisting

Memory Permitlisting

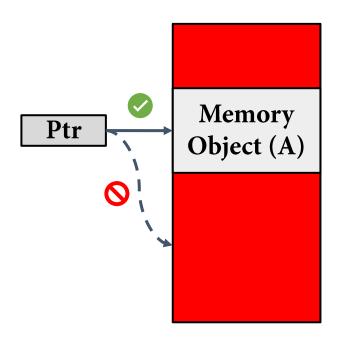




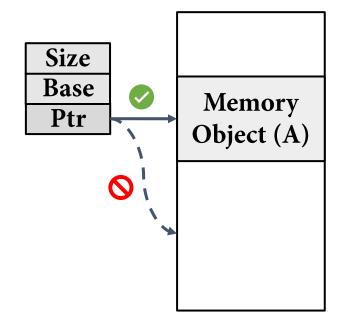
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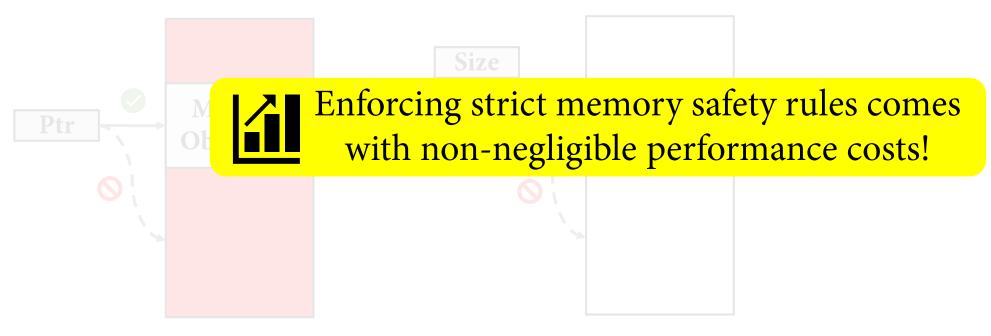


e.g., Intel's MPX and CHERI

Memory Blocklisting

Memory Permitlisting

Exploit Mitigation

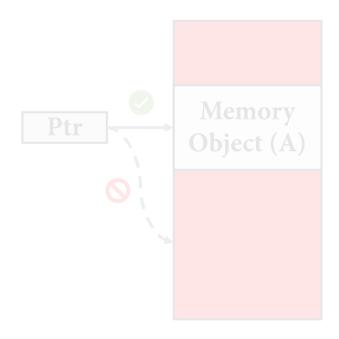


e.g., Google's Address Sanitizer

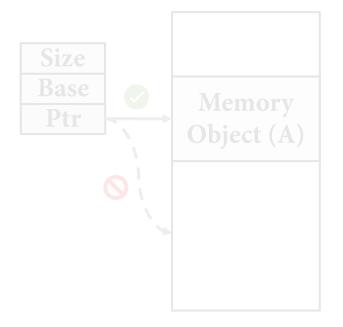
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Memory Blocklisting

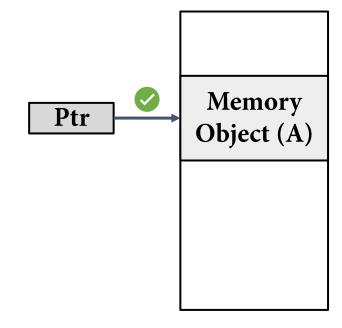
Memory Permitlisting



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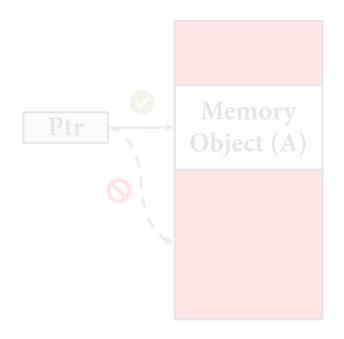


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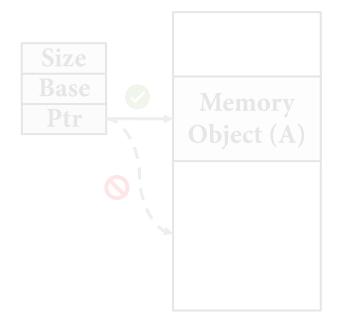


Memory Blocklisting

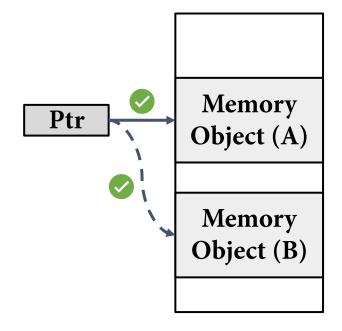
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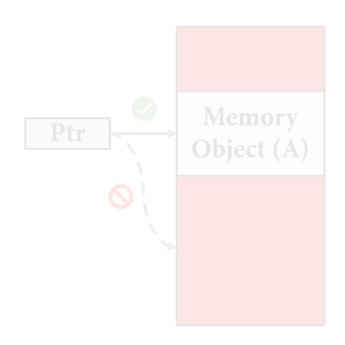


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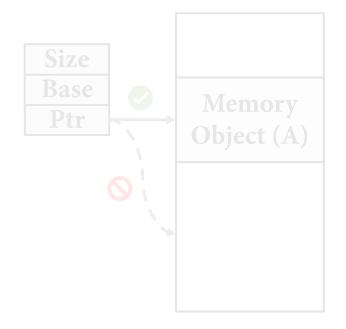


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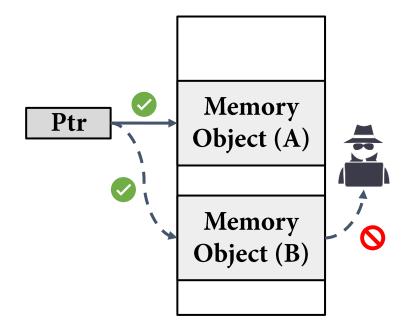
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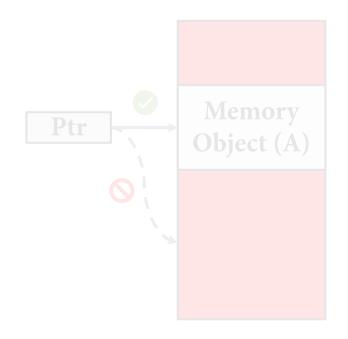


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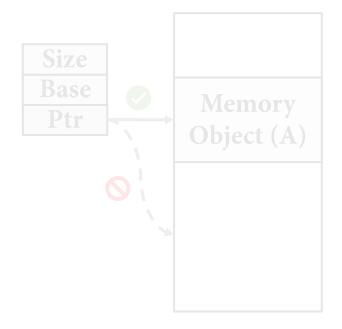


Memory Blocklisting

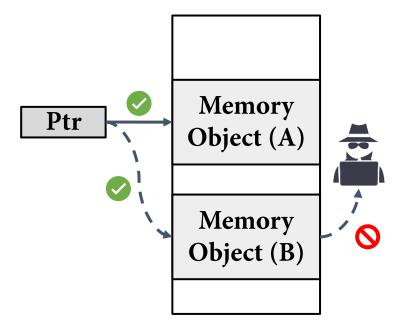
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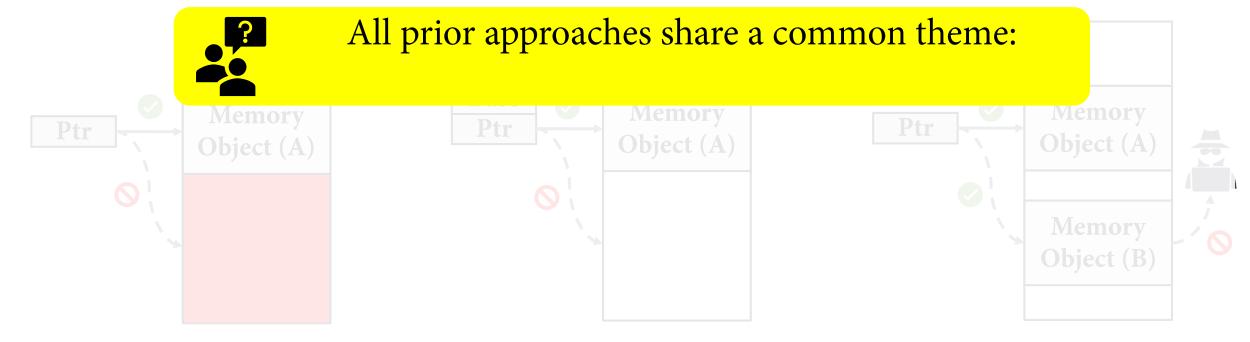
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e.g., ARM's PAC

Memory Blocklisting

Memory Permitlisting



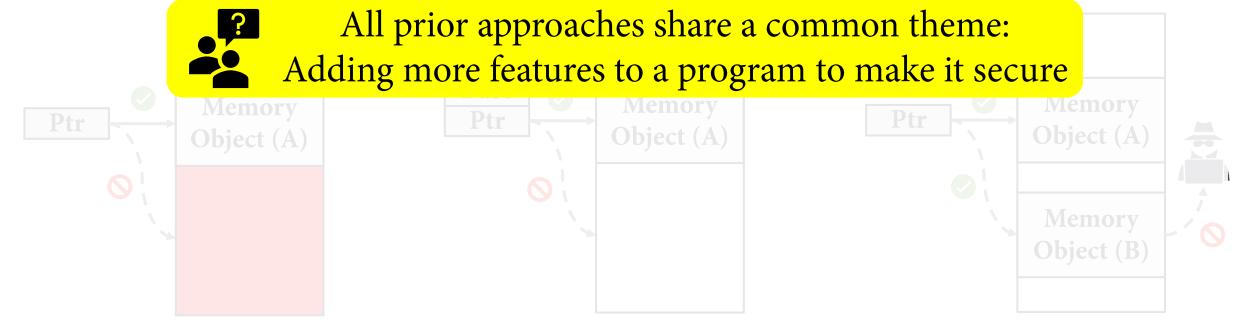
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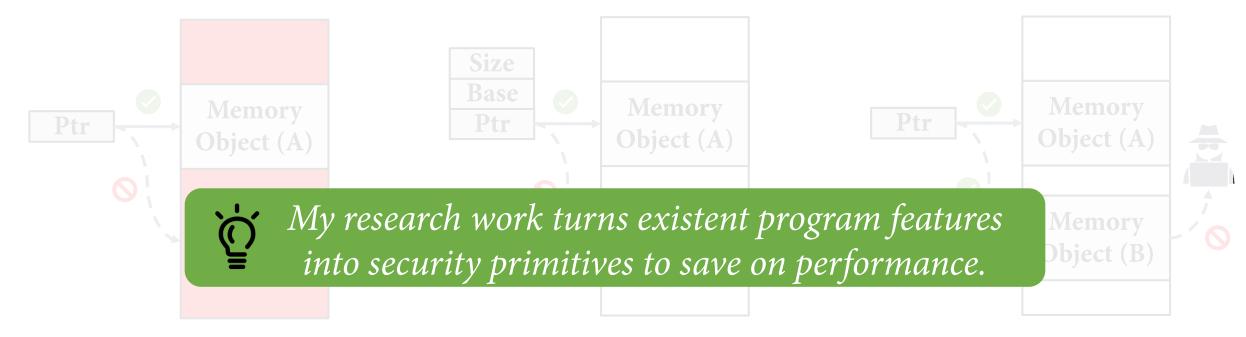
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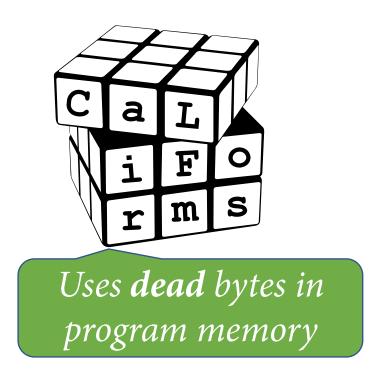
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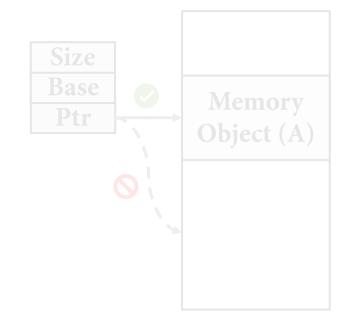
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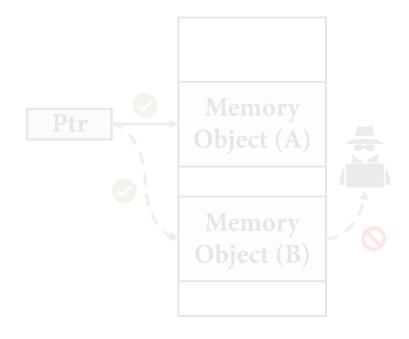


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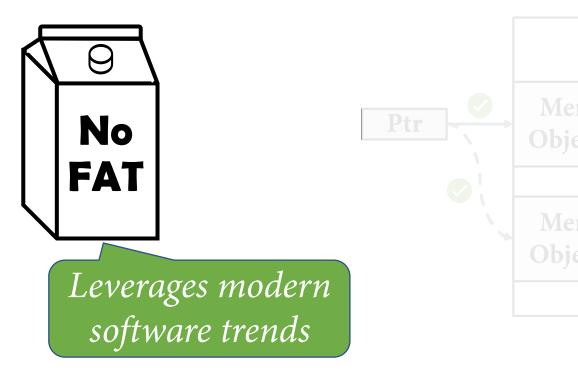


Memory Blocklisting







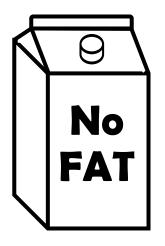


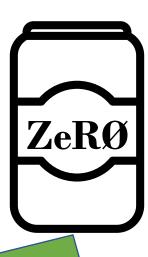
Memory Blocklisting

Memory Permitlisting

Exploit Mitigation







Mitigates all known exploits with **zero** runtime overheads.

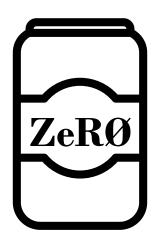
Memory Blocklisting

Memory Permitlisting

Exploit Mitigation







[MICRO 2019]

[ISCA 2021]

[ISCA 2021]

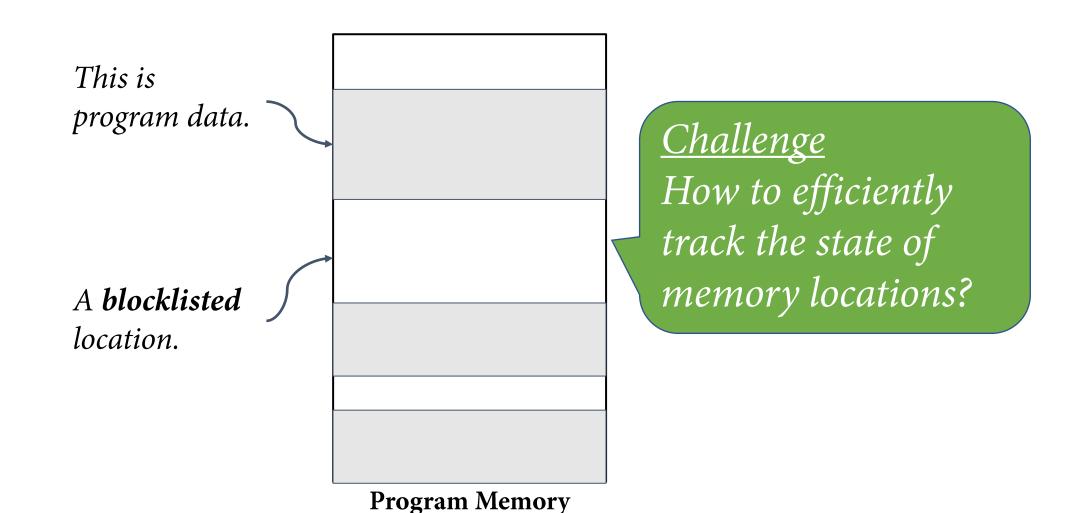


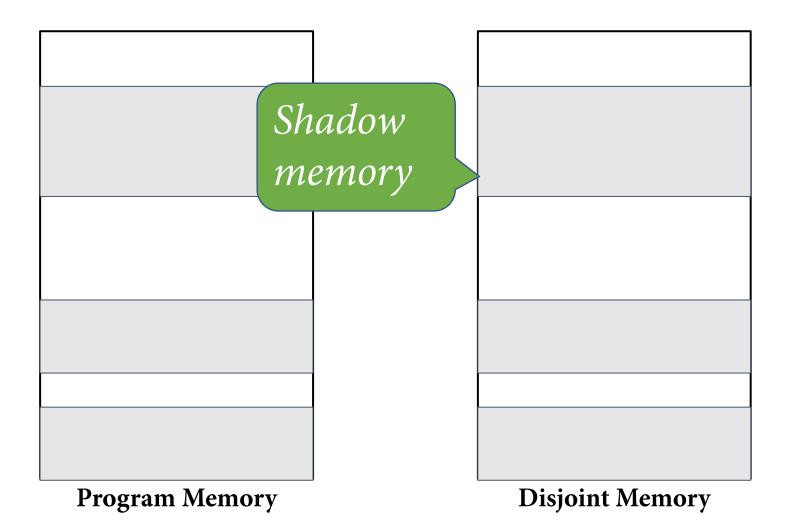
Cache Line Formats

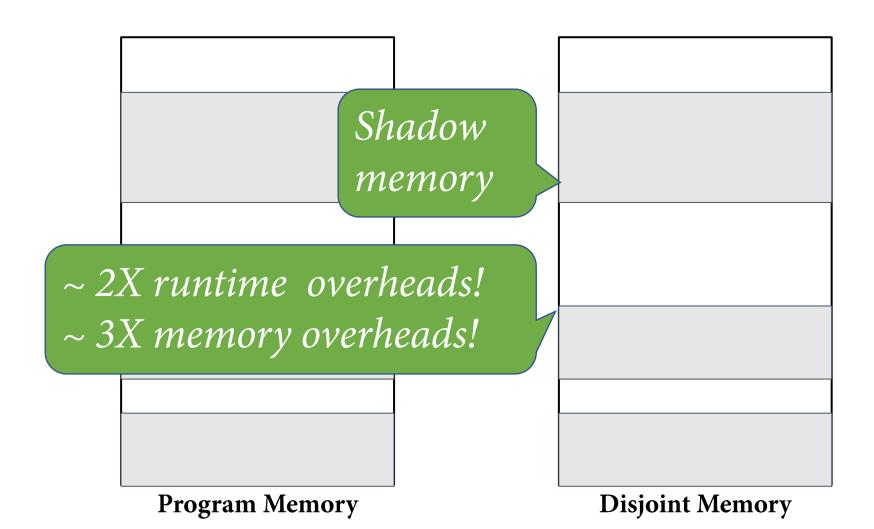
Hiroshi Sasaki, Miguel A. Arroyo, **Mohamed Tarek Ibn Ziad**, Koustubha Bhat, Kanad Sinha, and Simha Sethumadhavan, Practical byte-granular memory blacklisting using Califorms.

[MICRO 2019] [IEEE Micro Top Picks Honorable Mention]

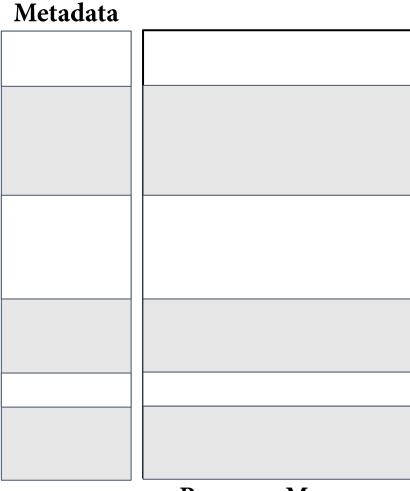




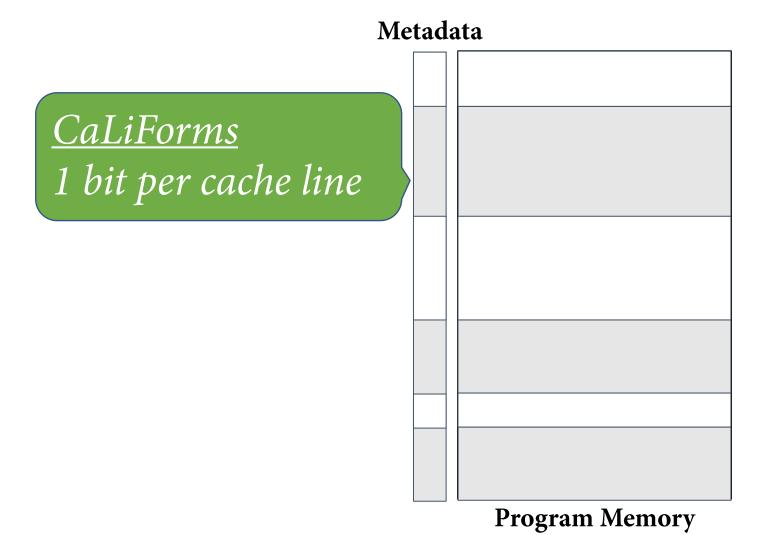


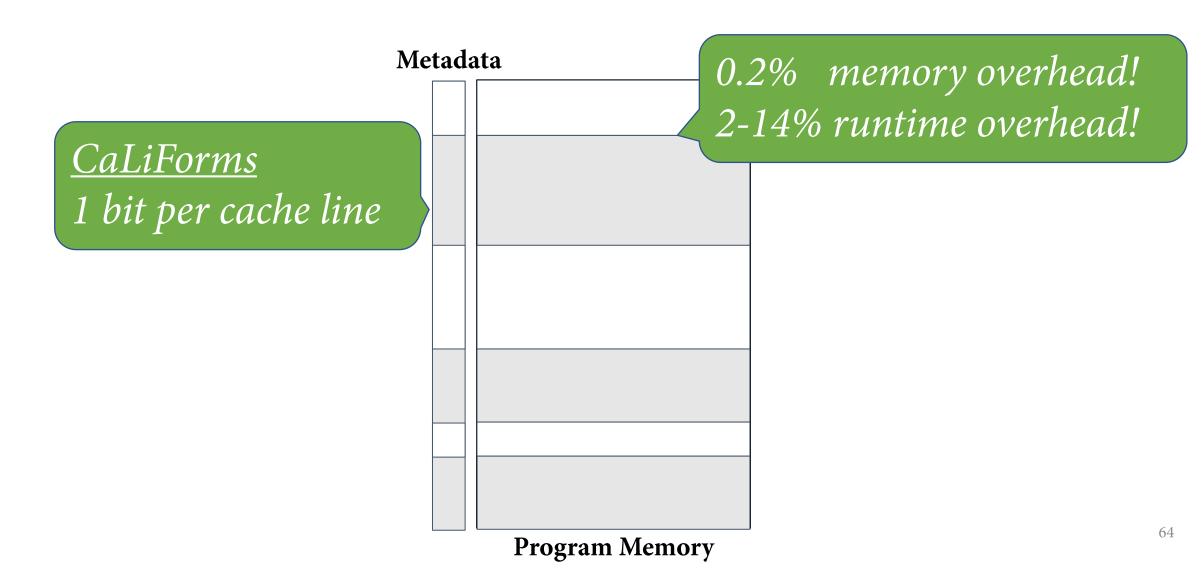


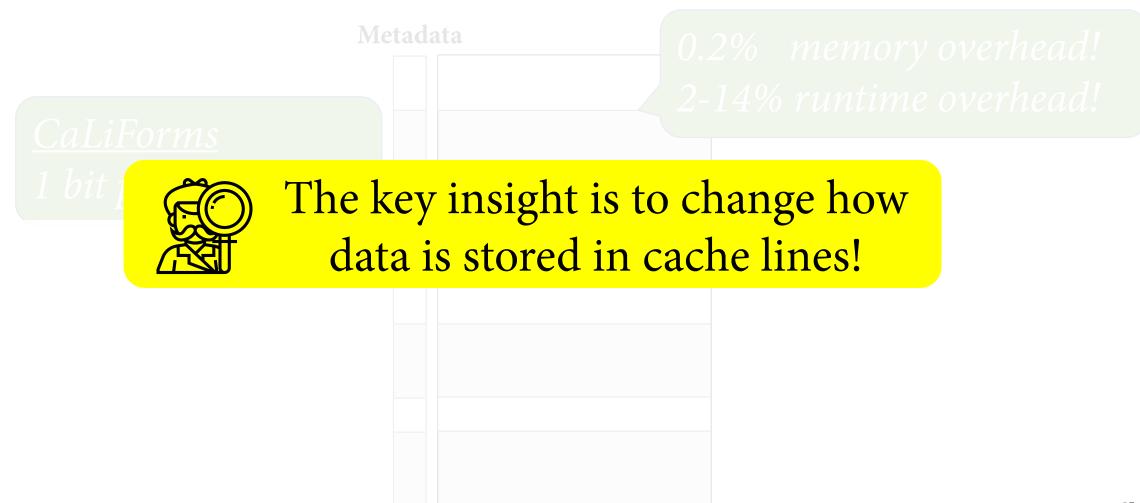
Memory Tagging n bits per cache line

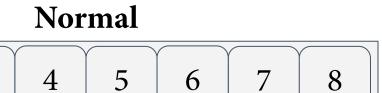


Metadata Memory Tagging n bits per cache line Limited entropy! **Program Memory**

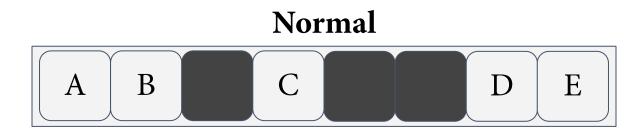




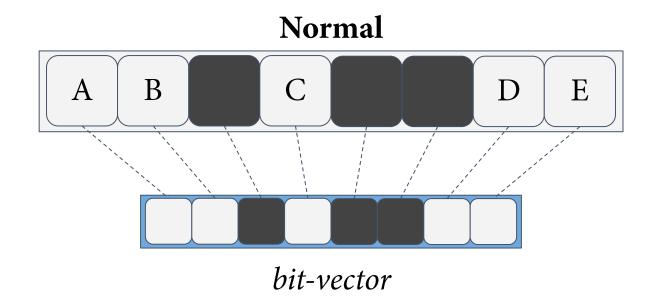




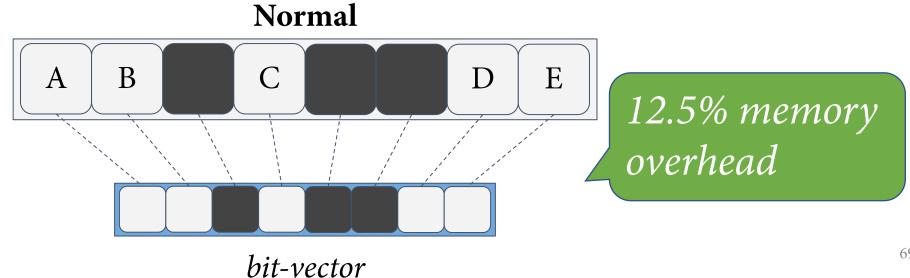






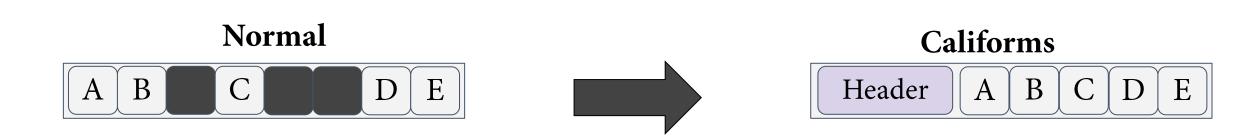






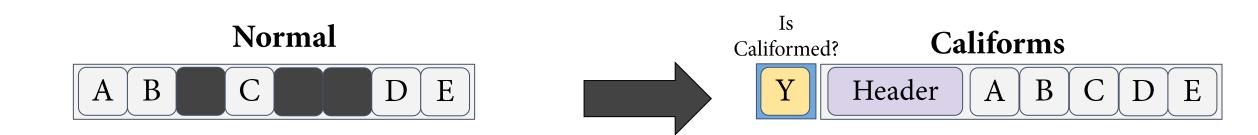
Our Metadata: Encoded within unused data.

Blocklisted Location

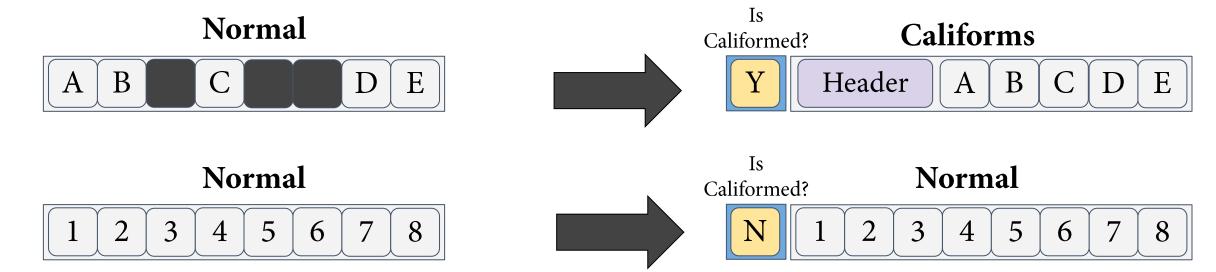


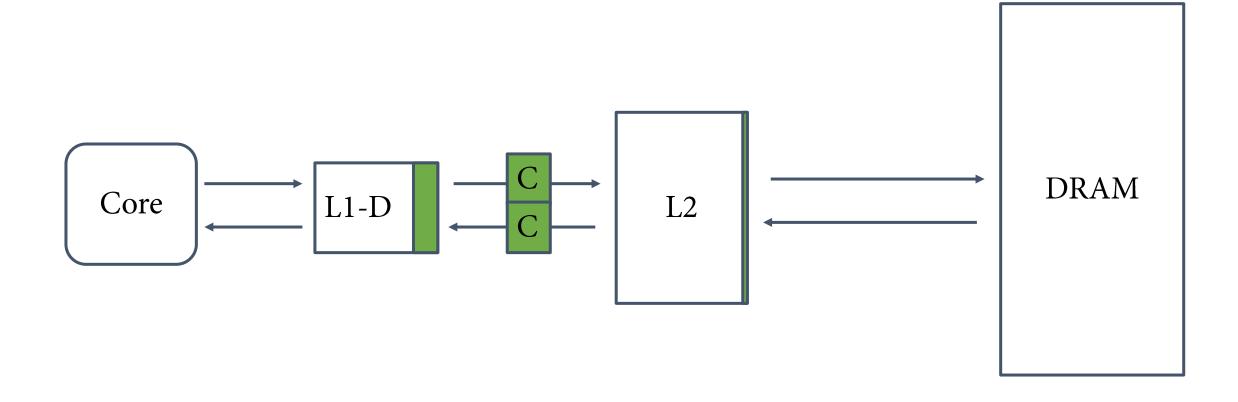
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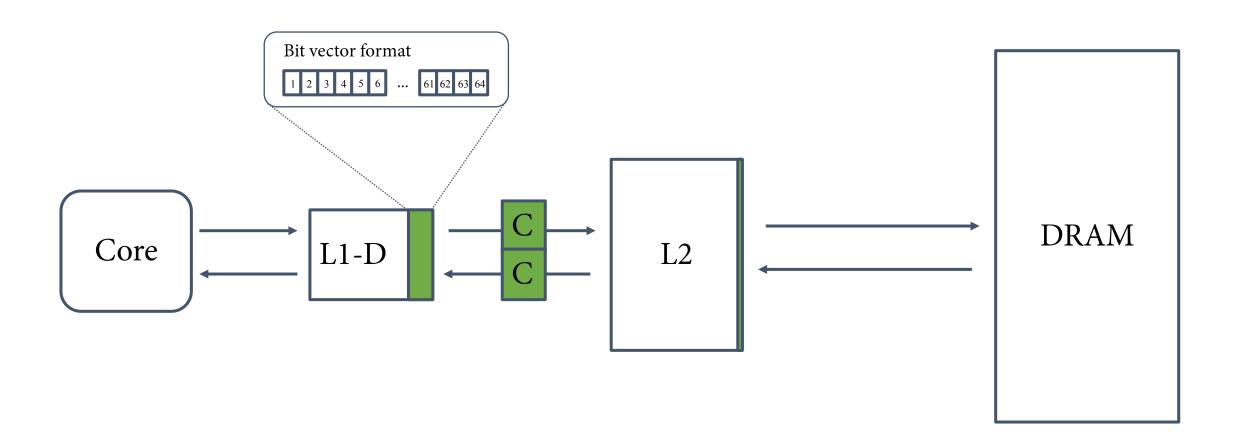
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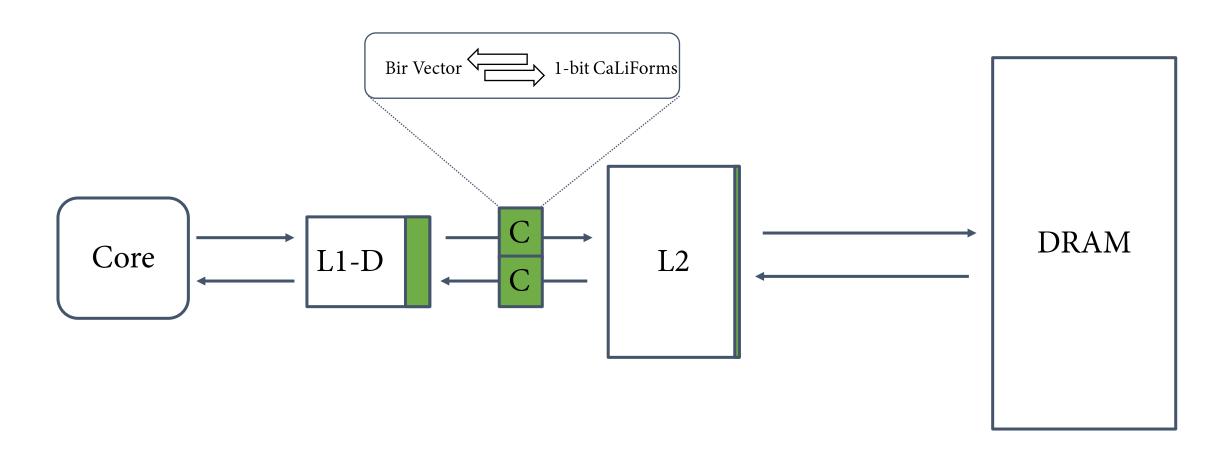


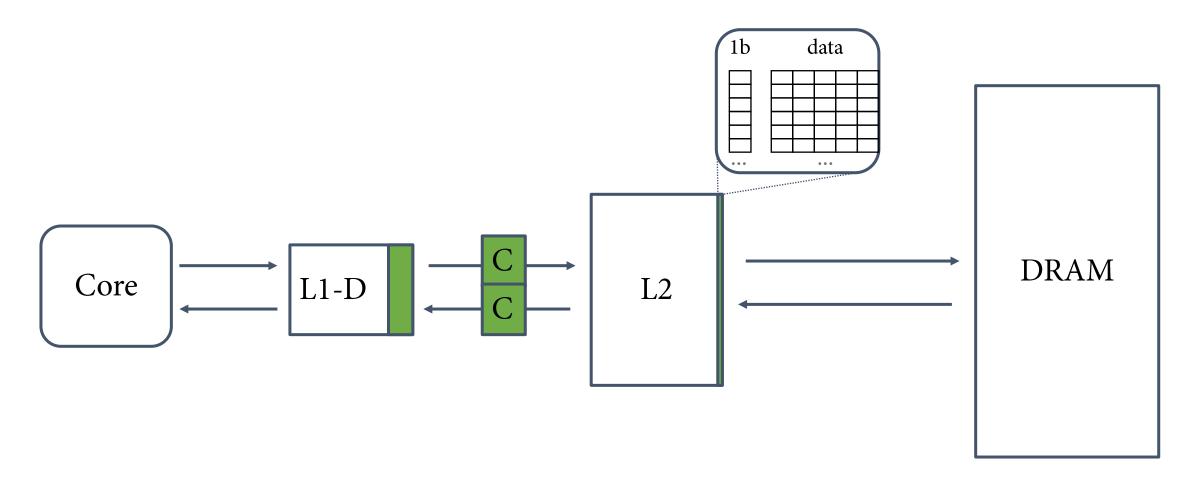


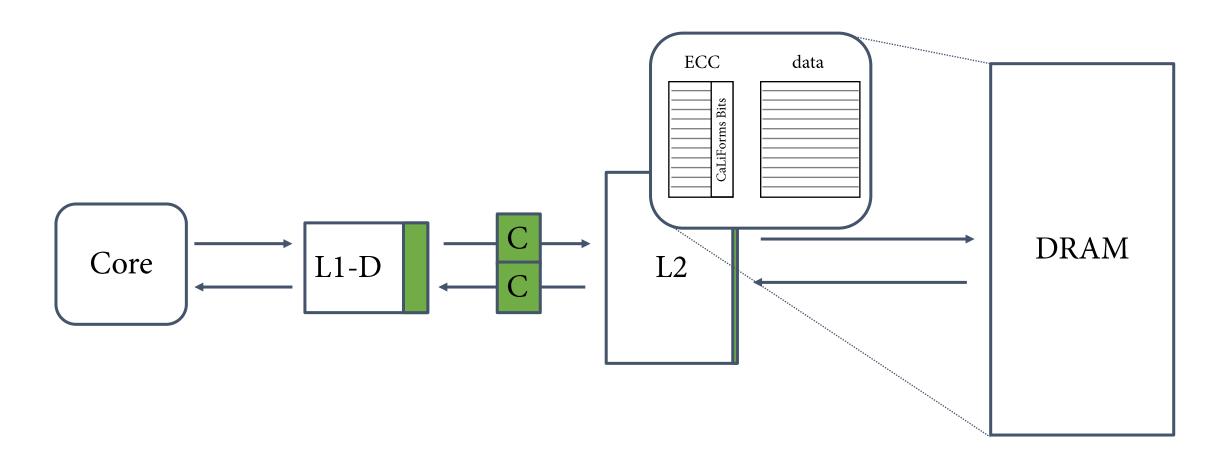


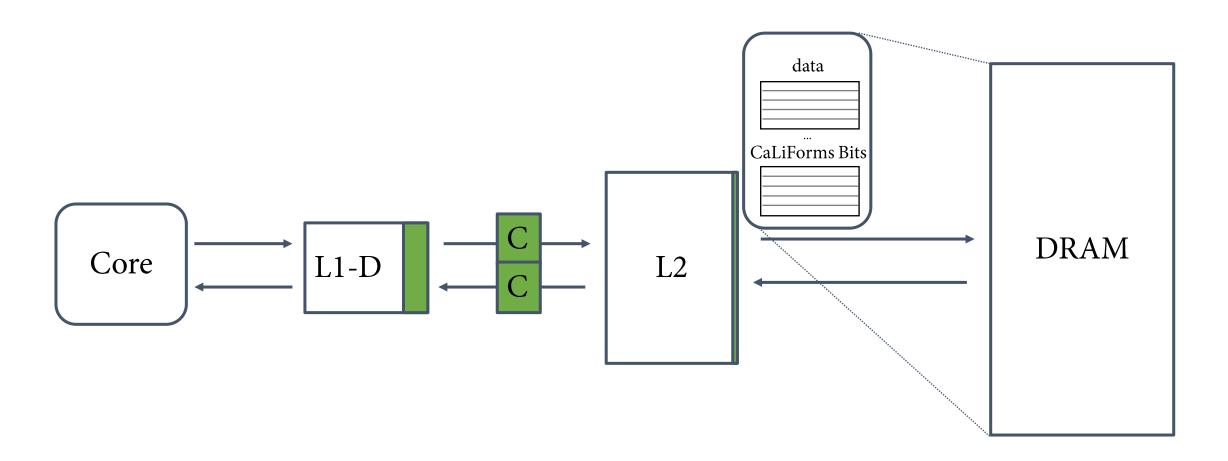




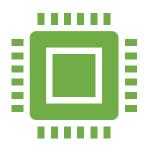








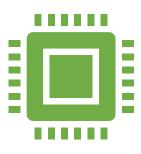
CaLiForms Performance Overheads



Hardware Modifications

Our measurements show no impact on the cache access latency.

CaLiForms Performance Overheads



Hardware Modifications

Our measurements show no impact on the cache access latency.

Software Modifications

• We evaluate three different insertion policies using Clang/LLVM.

CaLiForms Insertion Polices

```
struct
A_opportunistic {
  char c;
  char tripwire[3];
  int i;
  char buf[64];
  void (*fp)();
}
```

(1) Opportunistic

CaLiForms Insertion Polices

```
struct A_full {
struct
                                char tripwire[2];
A_opportunistic {
  char c;
                                char c;
  char tripwire[3];
                                char tripwire[1];
  int i;
                                int i;
                                char tripwire[3];
  char buf[64];
  void (*fp)();
                                char buf[64];
                                char tripwire[2];
                                void (*fp)();
                                char tripwire[1];
```

(1) Opportunistic

(2) Full

CaLiForms Insertion Polices

```
struct
A_opportunistic {
  char c;
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```

(1) Opportunistic

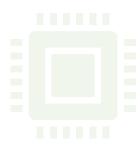
```
struct A_full {
  char tripwire[2];
  char c;
  char tripwire[1];
 int i;
  char tripwire[3];
  char buf[64];
 char tripwire[2];
 void (*fp)();
 char tripwire[1];
```

(2) Full

```
struct A_intelligent
{
  char c;
  int i;
  char tripwire[3];
  char buf[64];
  char tripwire[2];
  void (*fp)();
  char tripwire[3];
}
```

(3) Intelligent

CaLiForms Performance Overheads



Hardware Modifications

Our measurements show no impact on the cache access latency.

Software Modifications

• We evaluate three different insertion policies using Clang/LLVM.

CaLiForms Performance Overheads



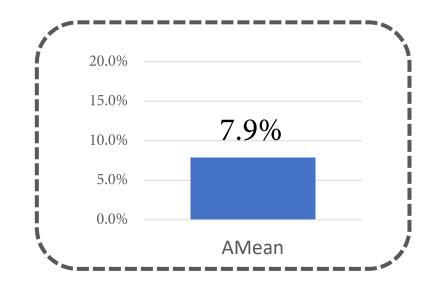
Hardware Modifications

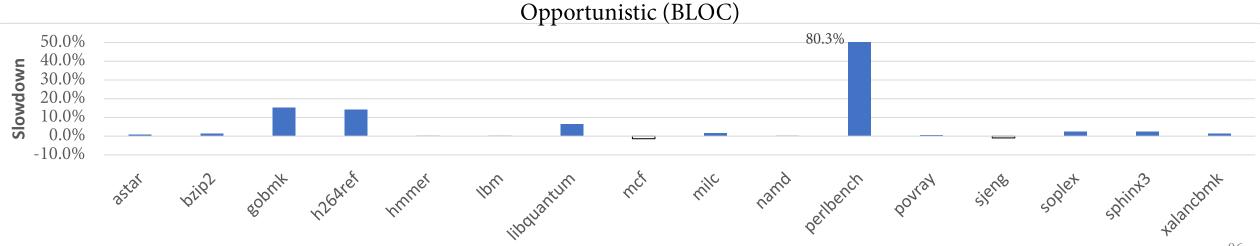
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Software Modifications

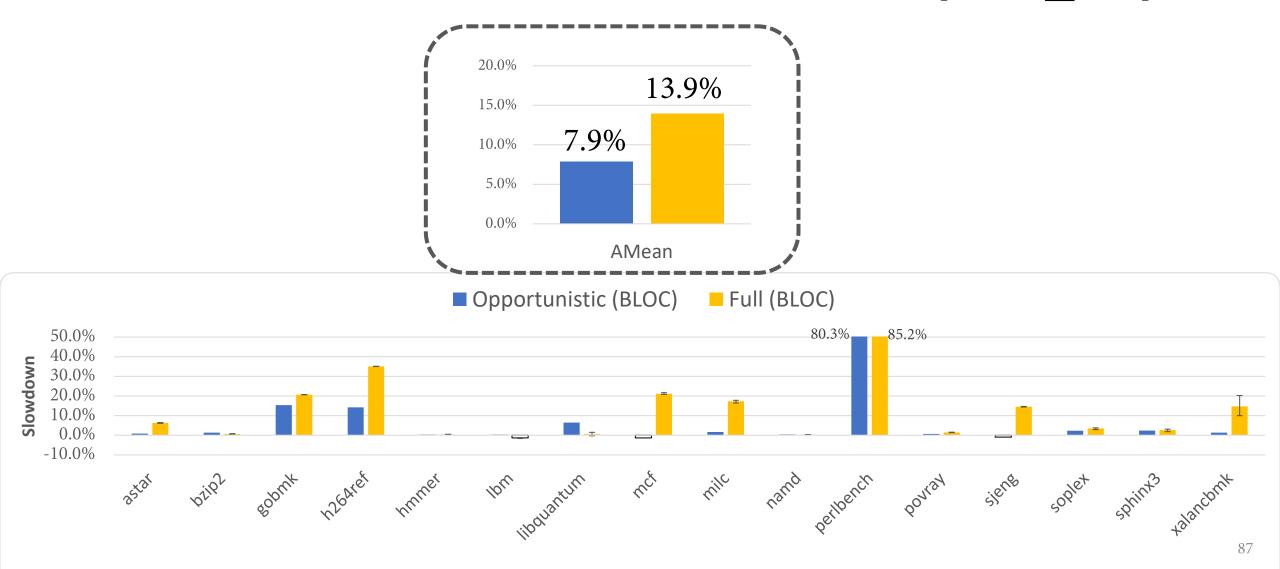
- We evaluate three different insertion policies using Clang/LLVM.
- We emulate the overheads of BLOC instructions that are used during malloc/free to mark the blocklisted locations per cacheline.

CaLiForms Performance Results (x86_64)

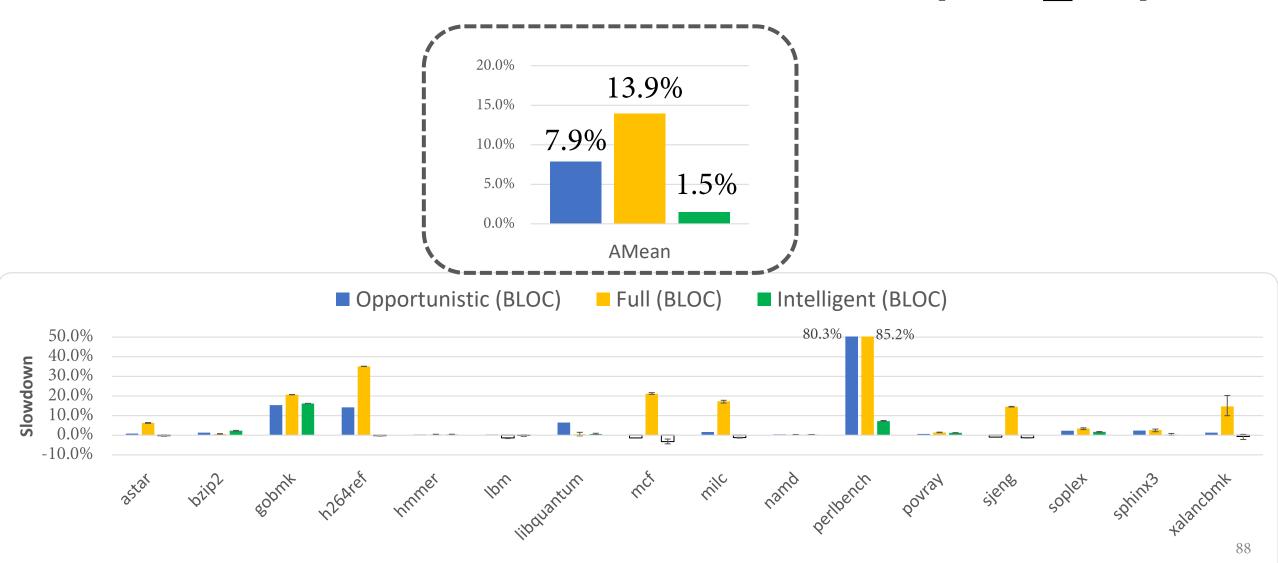




CaLiForms Performance Results (x86_64)



CaLiForms Performance Results (x86_64)



CaLiForms Performance Overheads

```
struct
A_opportunistic {
  char c;
  char tripwire[3];
  int i;
  char buf[64];
  void (*fp)();
}
```

```
char tripwire[2];
char c;

The intelligent policy
provides the best
performance-security
tradeoff.
```

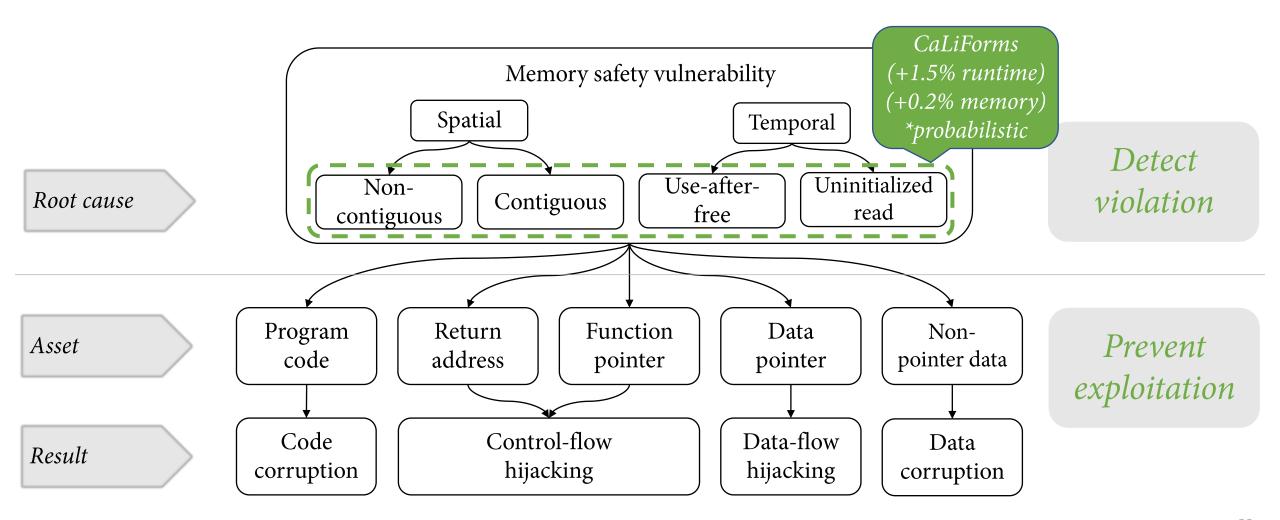
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}
```

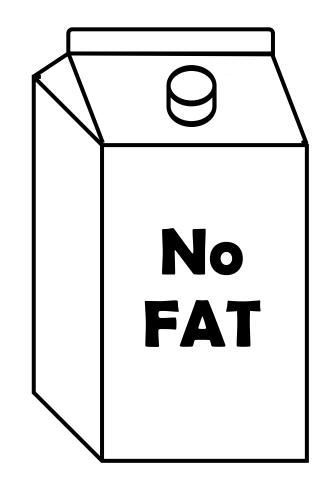
(1) Opportunistic

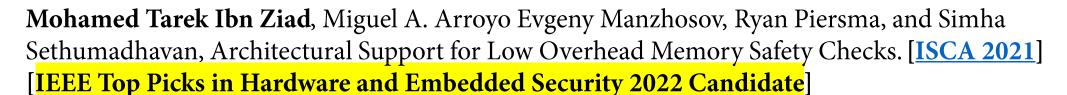
(2) Full

(3) Intelligent

Memory Attacks Taxonomy











Current software trends can be used to enhance systems security



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Increasing adoption of binning allocators



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Increasing adoption of binning allocators

- Maintains memory locality.
- Implicit lookup of allocation information.



Current software trends can be used to enhance systems security



Increasing adoption of binning allocators



- Maintains memory locality.
- Implicit lookup of allocation information.









```
40. int main() {
41.    char* ptr = malloc(12);
42.    ...
50. }
```

Virtual Memory

```
40. int main() {
41. char* ptr = malloc(12);
42. ...
50. }
```

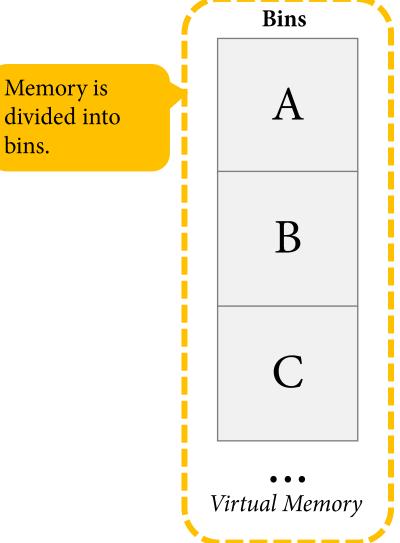


```
40. int main() {
41. char* ptr = malloc(12);
42. ...
50. }

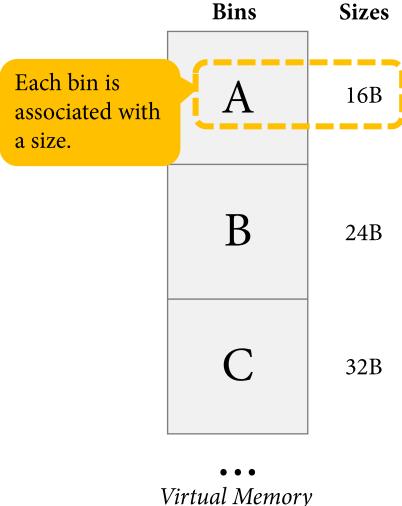
Memory is requested by the allocator.
```

Virtual Memory

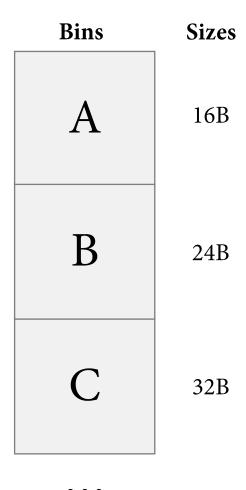
```
40. int main() {
41. char* ptr = malloc(12);
42. ...
50. }
```



```
int main() {
     char* ptr = malloc(12);
41.
42.
       • • •
50.
```

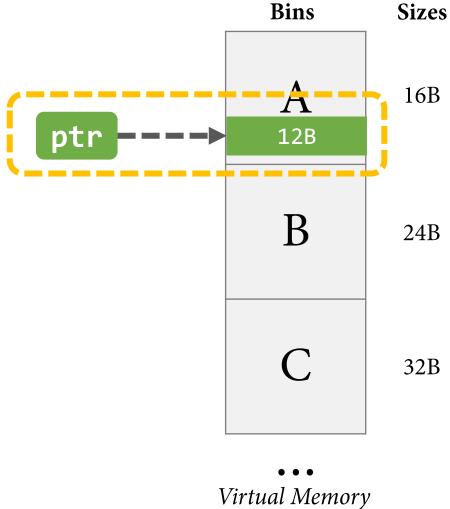


```
40. int main() {
41. char* ptr = 12B
42. ...
50. }
```

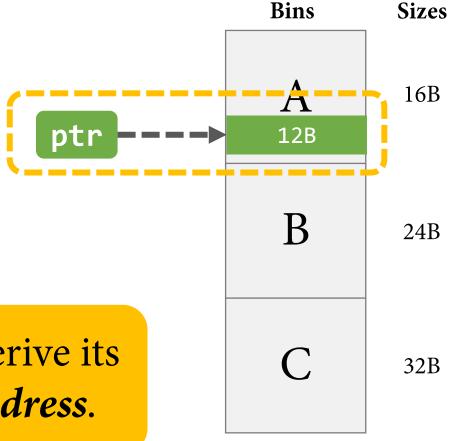


Virtual Memory

```
int main() {
     char* ptr = malloc(12);
41.
42.
       • • •
50.
```



```
40. int main() {
41. char* ptr = malloc(12);
42. ...
50. }
```

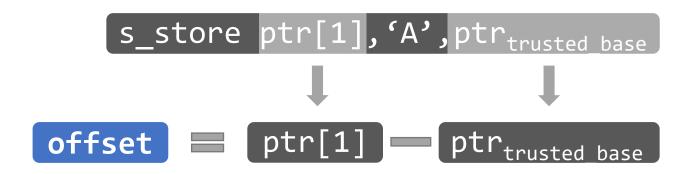


Given **any** pointer, we can derive its **allocation size** and **base address**.

Virtual Memory

```
40. int main() {
41.    char* ptr = malloc(12);
42.    ptr[1] = 'A';
43.    ...
50. }
```

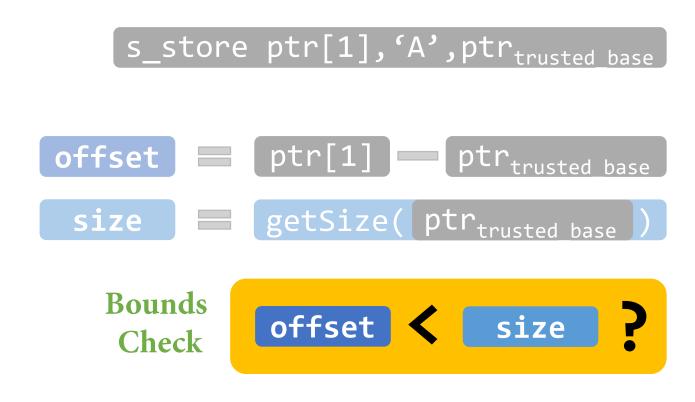
s_store ptr[1], A, ptr_{trusted base}



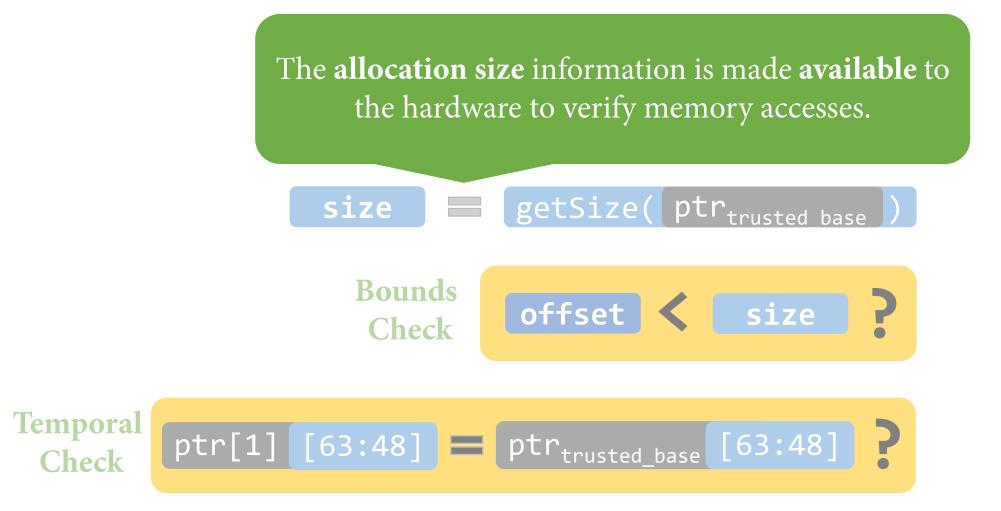
```
s_store ptr[1], 'A', ptr<sub>trusted_base</sub>

offset = ptr[1] = ptr<sub>trusted_base</sub>

size = getSize( ptr<sub>trusted_base</sub> )
```



```
s store ptr[1], 'A', ptr<sub>trusted base</sub>
                                ptr[1] = ptr<sub>trusted base</sub>
                     offset
                                    getSize( ptr<sub>trusted base</sub>
                         Bounds
                                     offset < size
                          Check
Temporal
           ptr[1] [63:48] = ptr<sub>trusted base</sub> [63:48]
  Check
```



Let's pass the pointer to another context (e.g., foo).

```
40. int main() {
41. char* ptr = malloc(12); ptr<sub>trusted base</sub>
42. ptr[1] = 'A'; s_store ptr[1], 'A', ptr<sub>trusted base</sub>
43. ...
49. foo(ptr);
50.
51. void Foo (char*)xptr){
52.
xptr[7] = 'B';
54. ...
60.
```

```
40. int main() {
41. char* ptr = malloc(12); ptr<sub>trusted base</sub>
42. ptr[1] = 'A'; s_store ptr[1], 'A', ptr<sub>trusted base</sub>
43. ...
49. foo(ptr);
50. }
51. void Foo (char* xptr){
52.
s_store xptr[7] = 'B'; \Rightarrow s_store xptr[7], 'B', xptr<sub>trusted base</sub>
54. ...
60.
```

```
40. int main() {
41. char* ptr = malloc(12); ptr<sub>trusted base</sub>
42. ptr[1] = 'A'; s_store ptr[1], 'A', ptr<sub>trusted base</sub>
43. ...
49. foo(ptr);
50.
51. void Foo (char* xptr){
52.
                           s store xptr[7], B, xptr<sub>trusted base</sub>
xptr[7] = 'B';
54.
                                                How do we get this?
60.
```

```
40. int main() {
41. char* ptr = malloc(12); ptr<sub>trusted base</sub>
42. ptr[1] = 'A'; s_store ptr[1], 'A', ptr<sub>trusted base</sub>
43. ...
49. foo(ptr);
50.
51. void Foo (char* xptr){
                             xptr<sub>trusted base</sub> ← compBase(xptr[7])
52.
xptr[7] = 'B';
                            s_store xptr[7], B, xptr<sub>trusted base</sub>
54.
60.
```

 $\left\{ \text{xptr}_{\text{trusted base}} \leftarrow \text{compBase}(\text{xptr}[7]) \right\}$

$$\left[xptr_{trusted\ base} \leftarrow compBase(xptr[7]) \right]$$

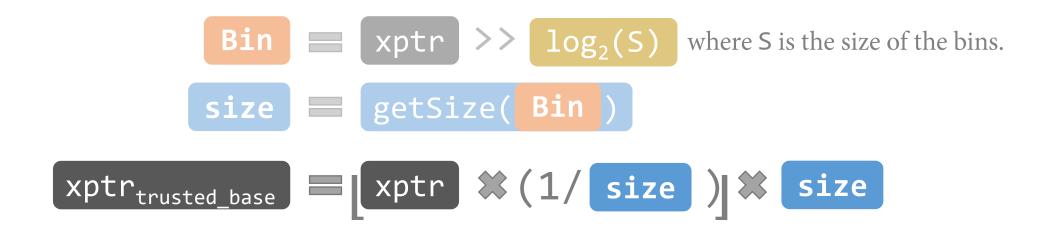


```
xptr<sub>trusted base</sub> ← compBase(xptr[7])
```

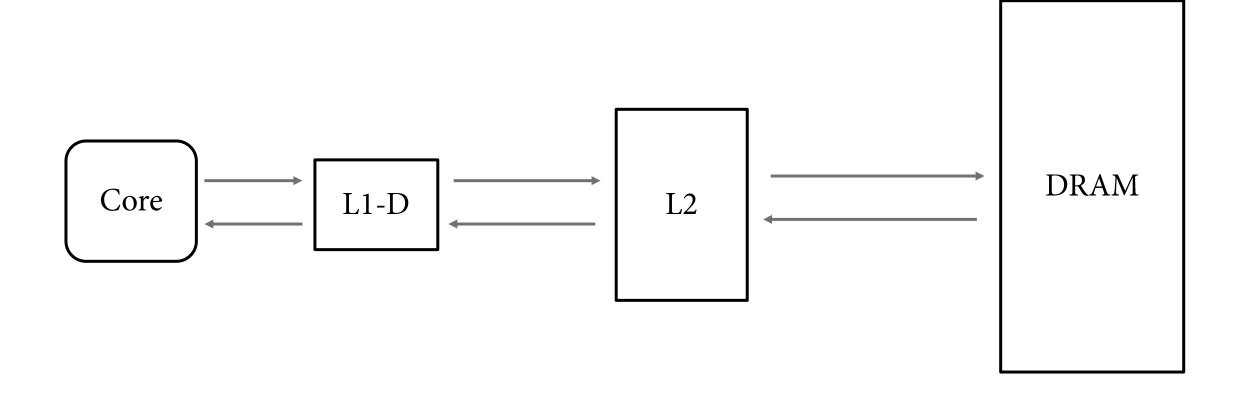
```
Bin = xptr >> log<sub>2</sub>(S) where S is the size of the bins.

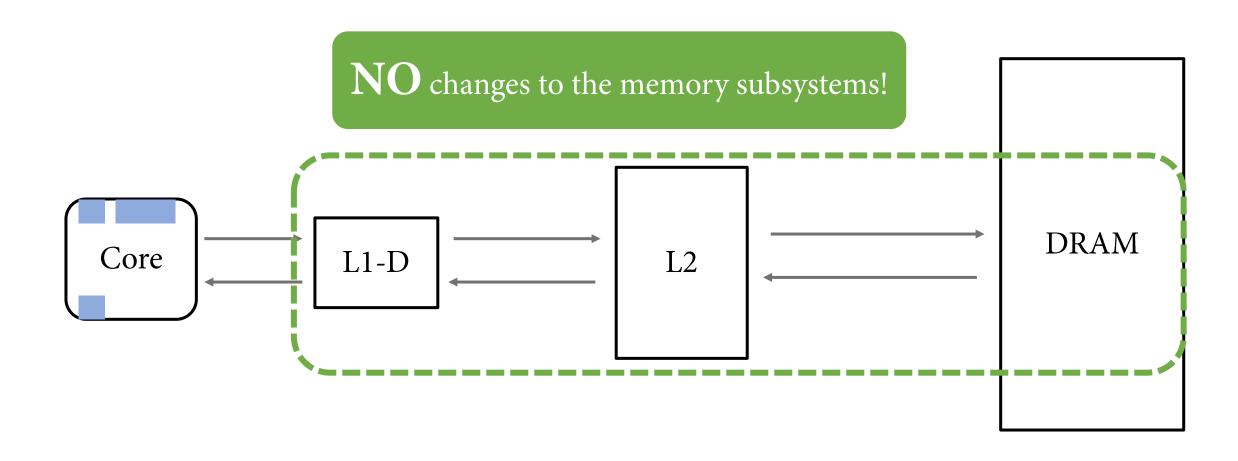
size = getSize(Bin)
```

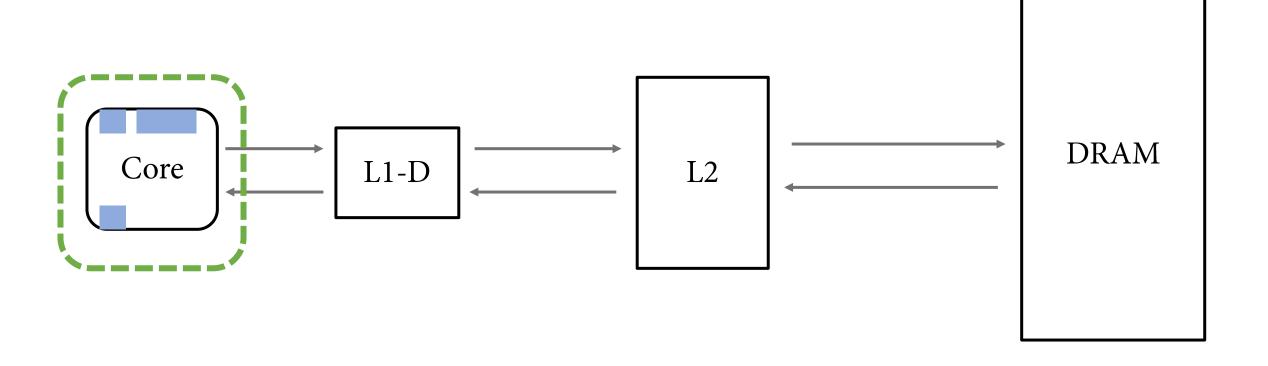
 $\left[xptr_{trusted\ base} \leftarrow compBase(xptr[7]) \right]$

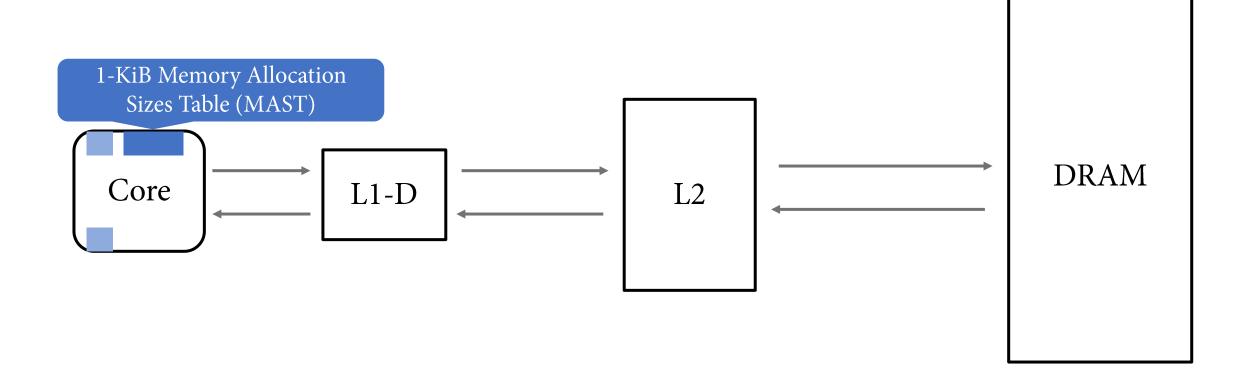


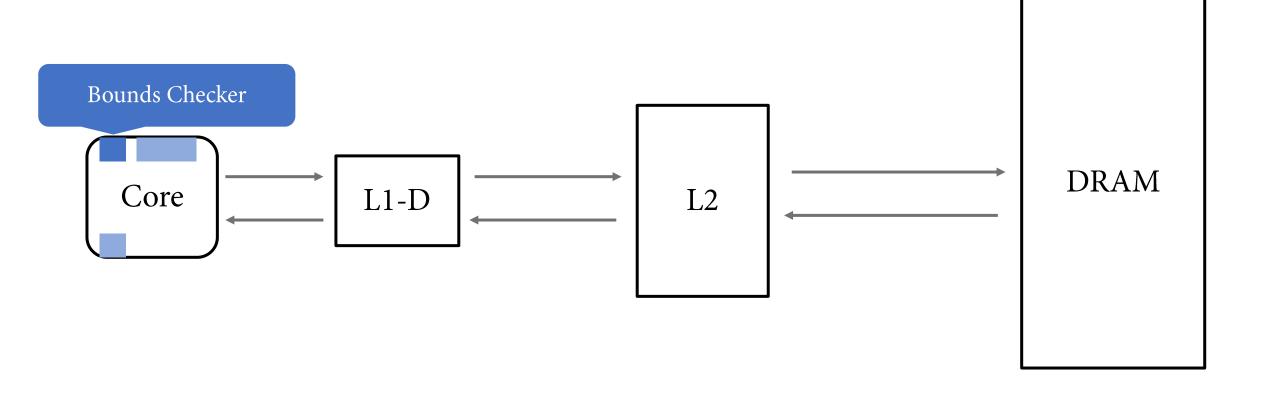
Base pointer is **implicitly** derived!

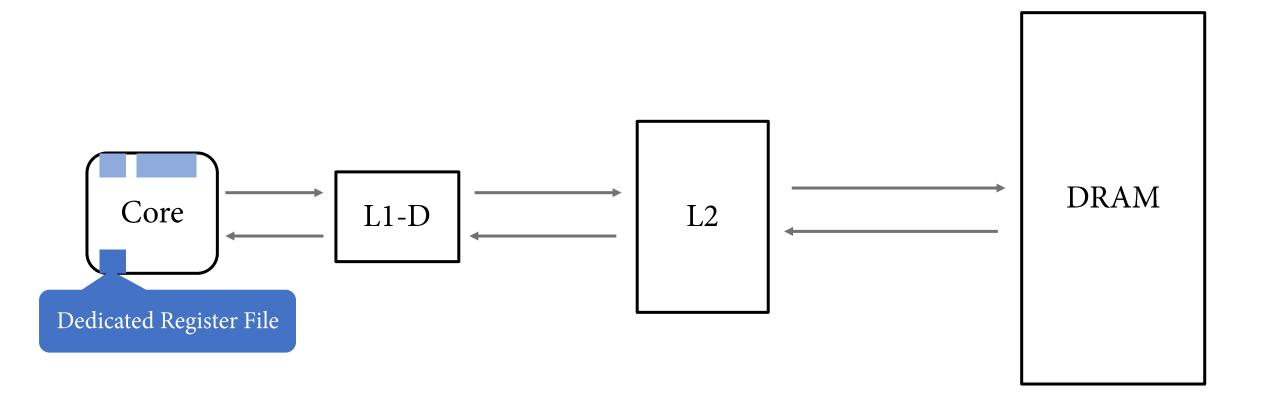


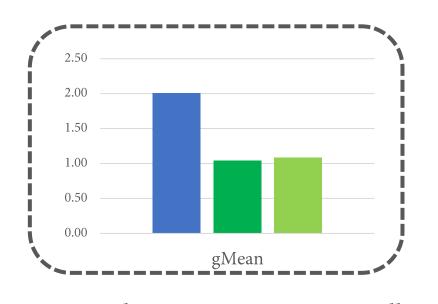




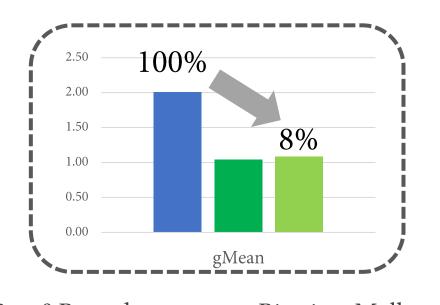


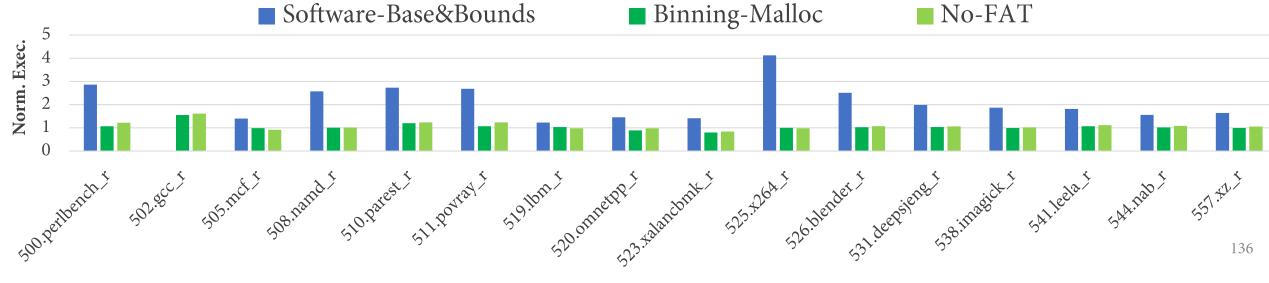


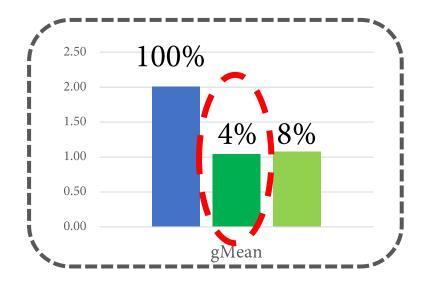






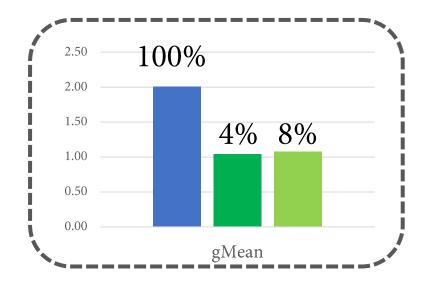






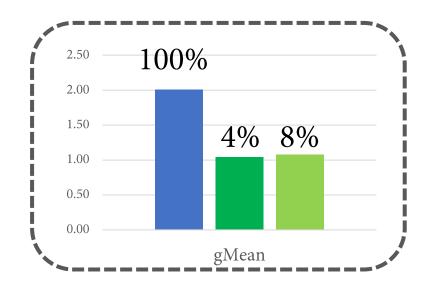
Most of No-FAT's overheads are attributed to:

• The binning memory allocator, and



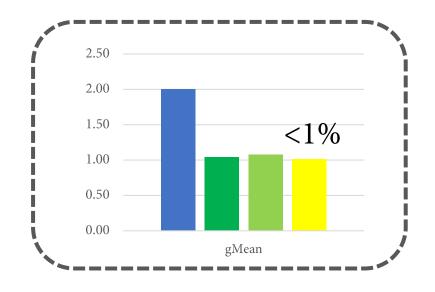
Most of No-FAT's overheads are attributed to:

- The binning memory allocator, and
- The back-to-back MULs during base address computation



Most of No-FAT's overheads are eliminated with:

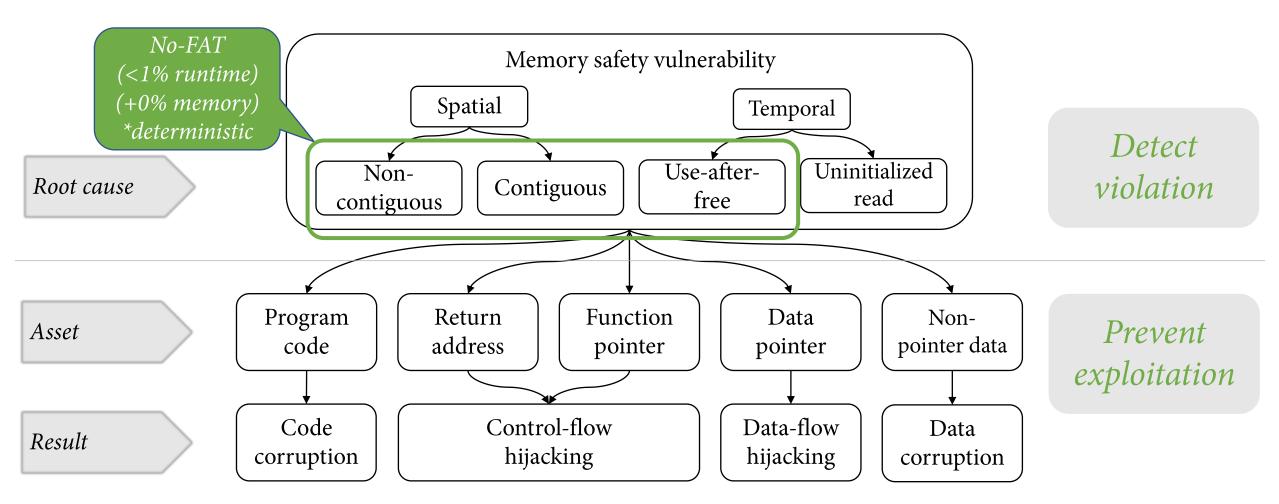
• A performant binning memory allocator (e.g., MiMalloc), and



Most of No-FAT's overheads are eliminated with:

- A performant binning memory allocator (e.g., MiMalloc), and
- A base address cache for derived pointers.

Memory Attacks Taxonomy



My solutions for C/C++ memory (un)safety

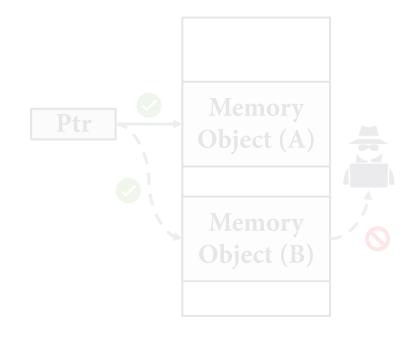
Memory Blocklisting

Memory Permitlisting

Exploit Mitigation







[MICRO 2019]

[ISCA 2021]

Comparison with prior work

Comparison with prior work

Metadata

Memory Tagging

N bits per pointer & allocation

Concerns

Spatial & temporal safety limited by tag width

Metadata

Spatial & temporal safety limited by tag width

Memory Tagging

N bits per allocation

N bits per pointer & allocation

Susceptible to non-adjacent overflows

Concerns

Tripwires

Memory TaggingN bits per pointer & allocationSpatial & temporal safety limited by tag widthTripwiresN bits per allocationSusceptible to non-adjacent overflowsCaLiForms1 bit per cache lineProvides probabilistic guarantees

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1 bit per cache line

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Explicit Base & Bounds

N bits per pointer or allocation

Breaks compatibility with the rest of the system (eg. unprotected libraries).

	Metadata	Concerns
Memory Tagging	N bits per pointer & allocation	Spatial & temporal safety limited by tag width
Tripwires	N bits per allocation	Susceptible to non-adjacent overflows
CaLiForms	1 bit per cache line	Provides probabilistic guarantees
Explicit Base & Bounds	N bits per pointer or allocation	Breaks compatibility with the rest of the system (eg. unprotected libraries).
No-FAT	Fixed (1K) bits per process	Requires binning allocator

My solutions for C/C++ memory (un)safety

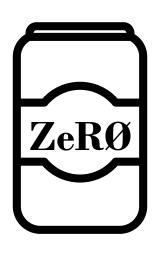
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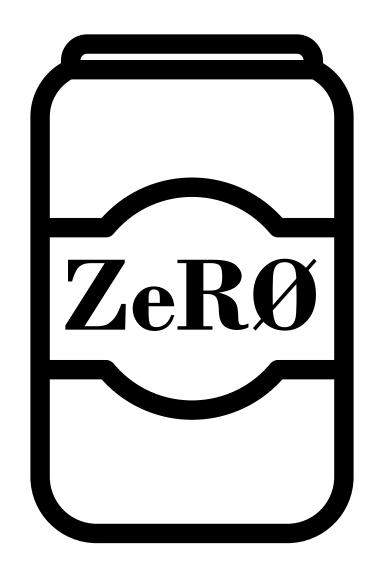


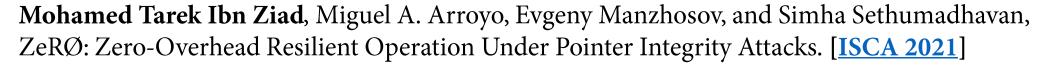


[MICRO 2019]

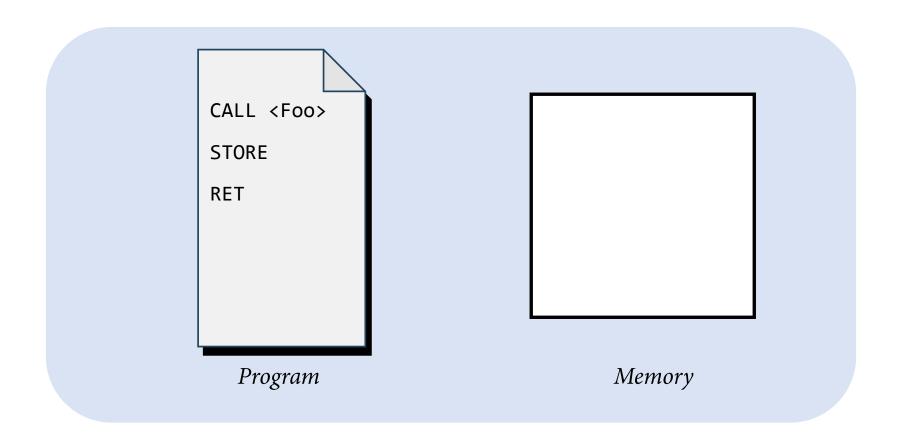
[ISCA 2021]

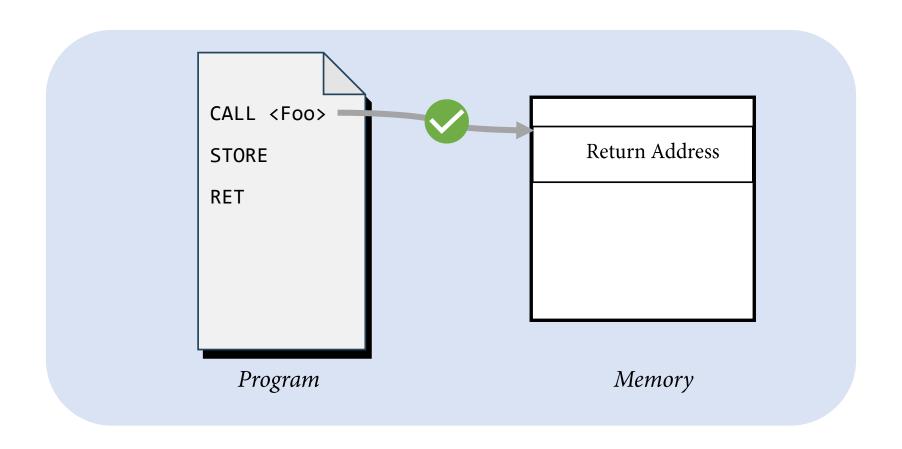
[ISCA 2021]

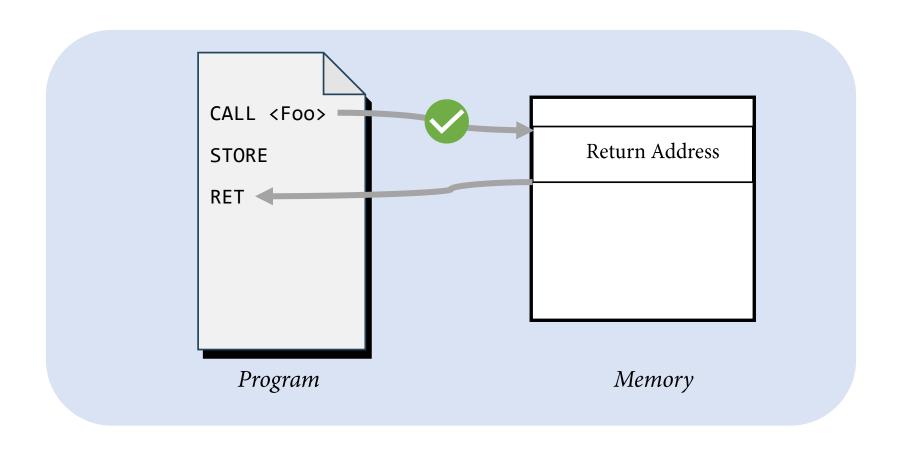


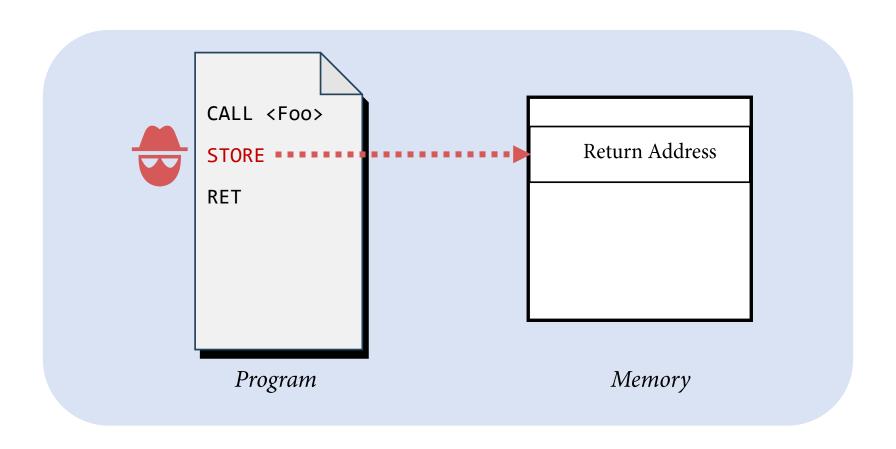


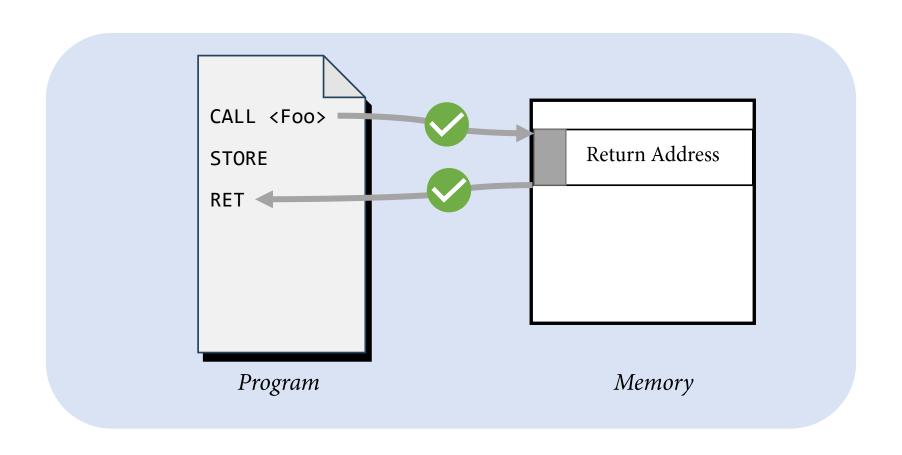


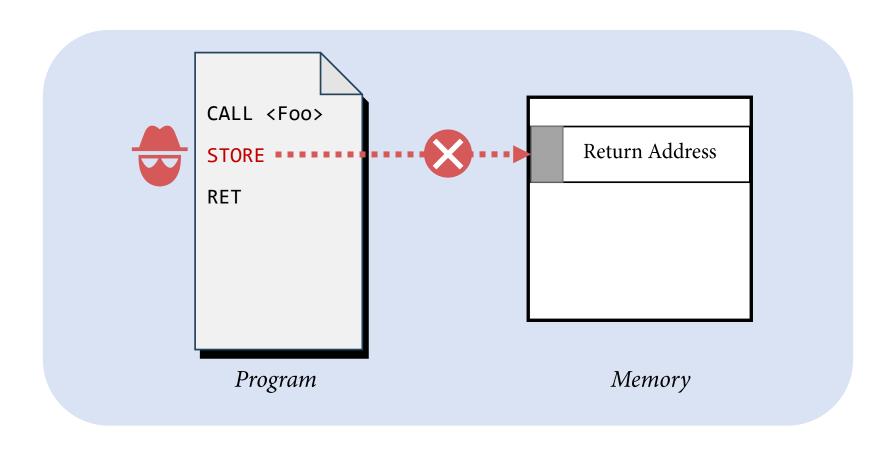


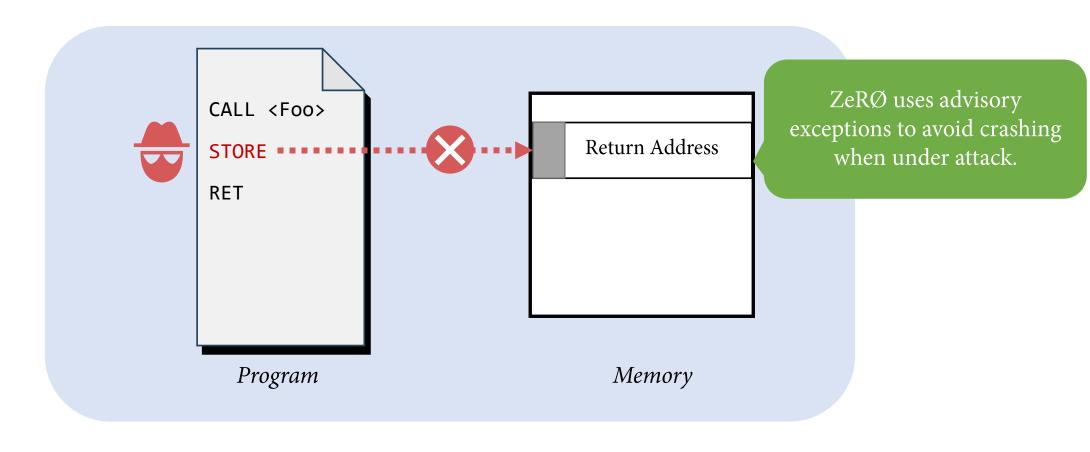




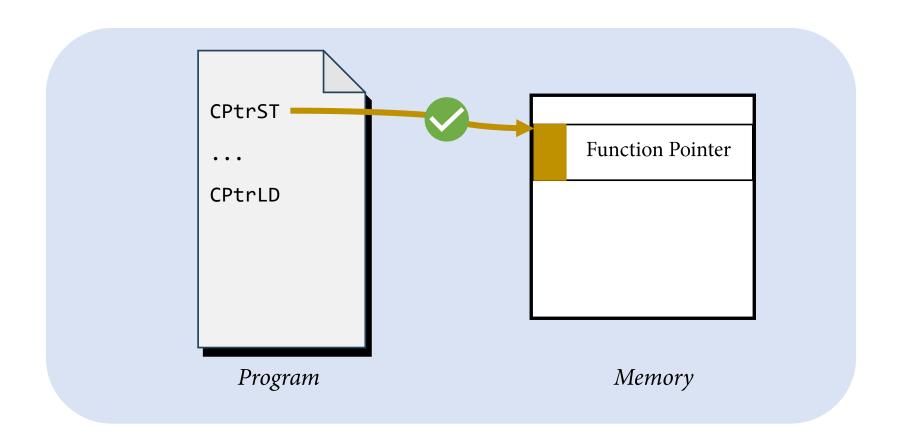




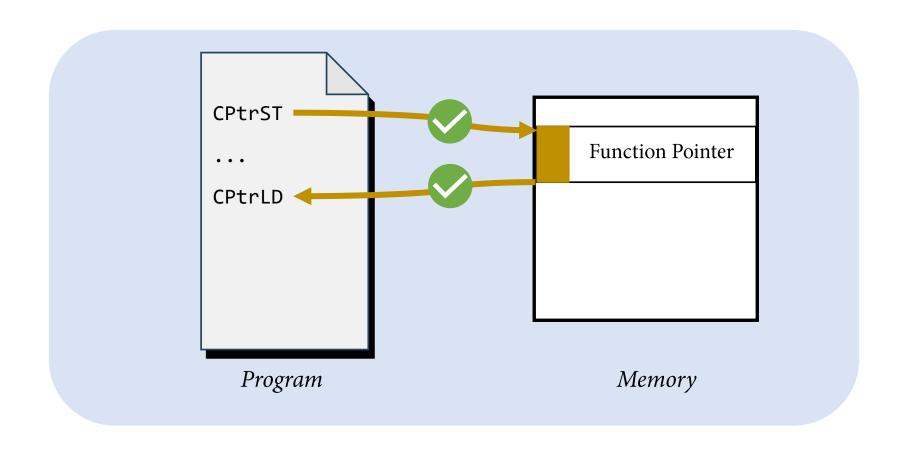




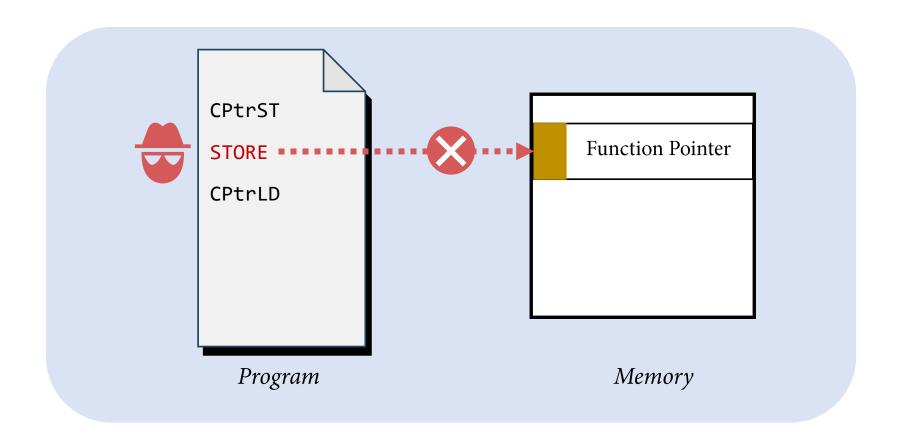
Code Pointer Integrity with ZeRØ



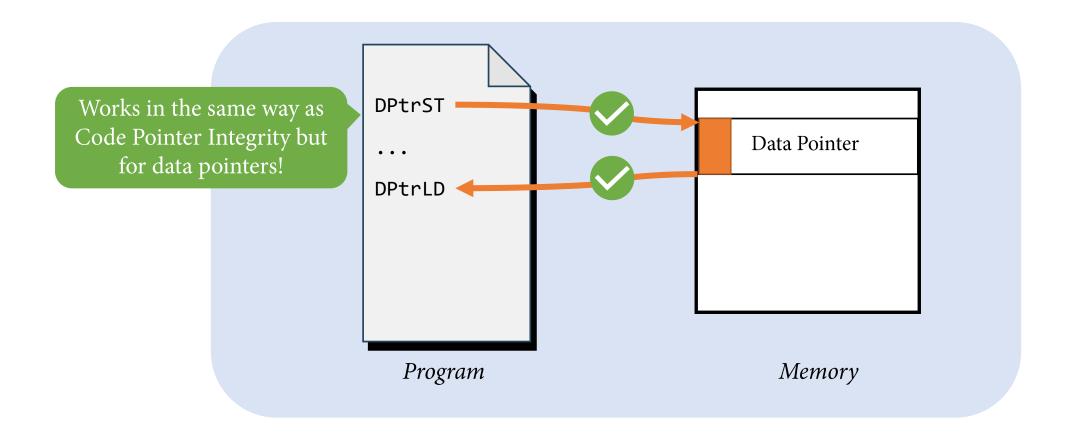
Code Pointer Integrity with ZeRØ



Code Pointer Integrity with ZeRØ



Data Pointer Integrity with ZeRØ





Efficiently Tracking Metadata

In ZeRØ, we encode metadata within unused pointer bits.

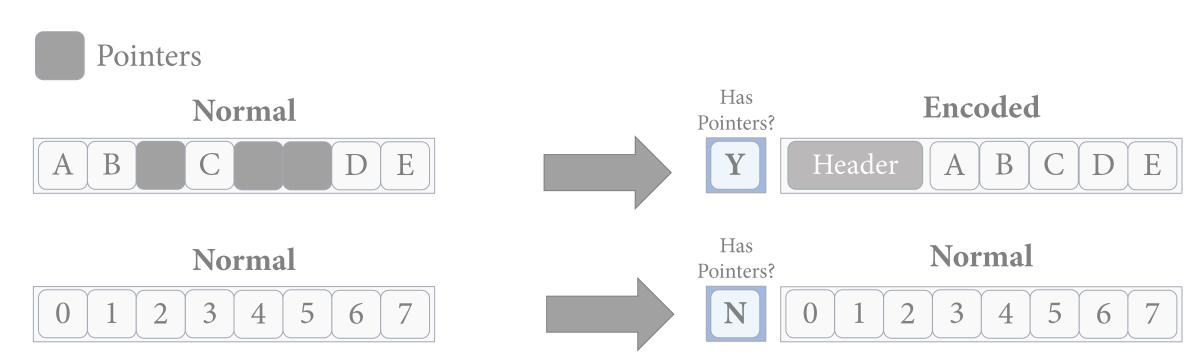


64-bit Pointer

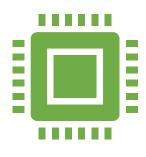
Efficiently Tracking Metadata



We use a novel variant of CaLiForms



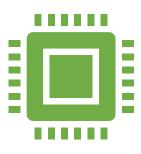
ZeRØ Performance Overheads



Hardware Modifications

Our measurements show no impact on the cache access latency.

ZeRØ Performance Overheads



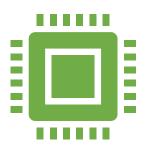
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Software Modifications

• Our special load/stores do not change the binary size.

ZeRØ Performance Overheads

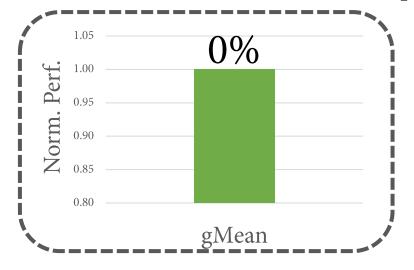


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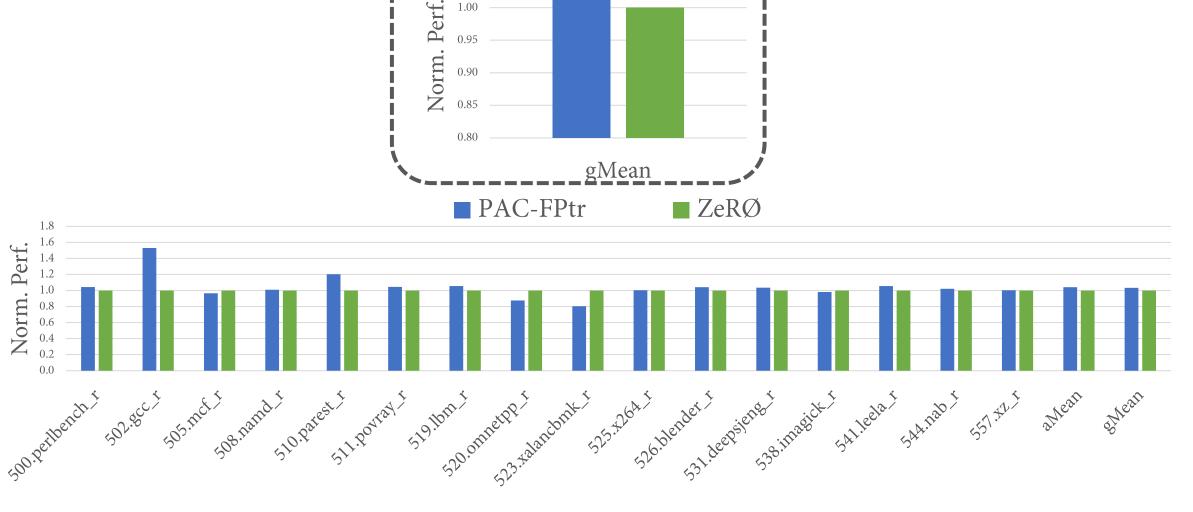
Software Modifications

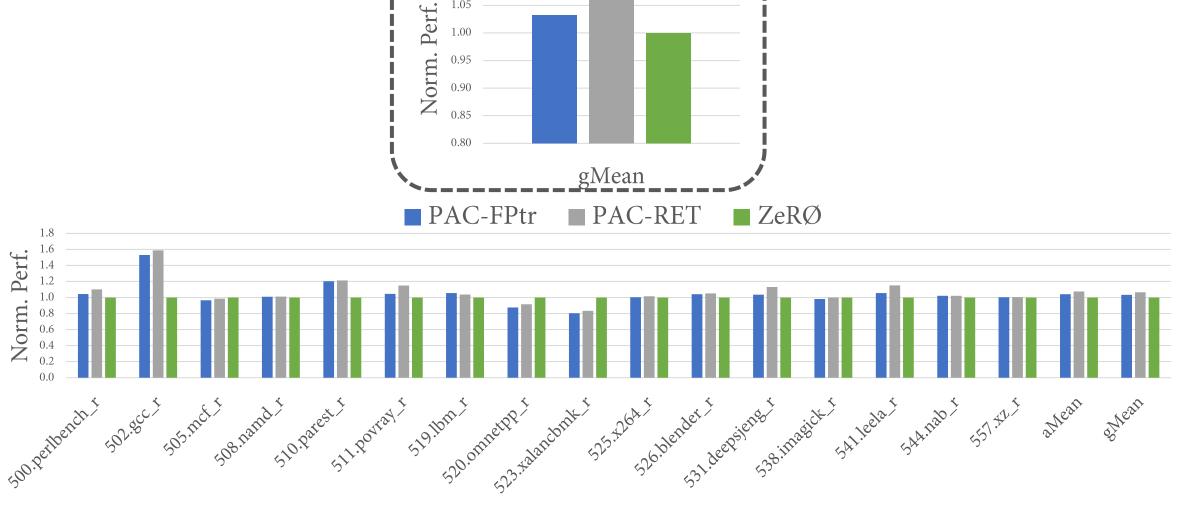
- Our special load/stores do not change the binary size.
- The ClearMeta instructions are only called on memory deletion.

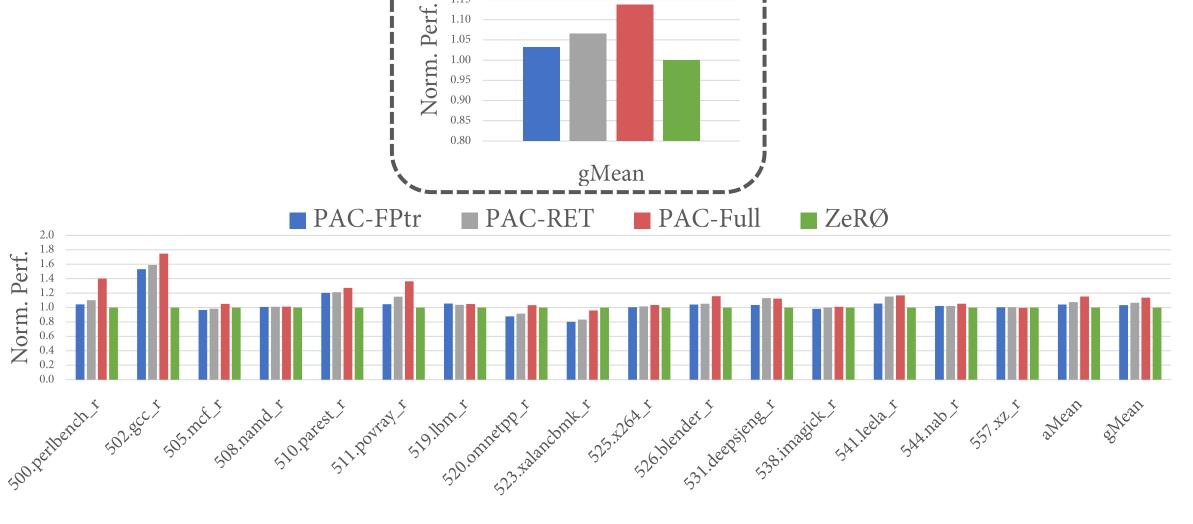


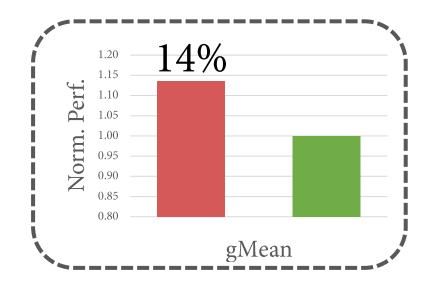


3%



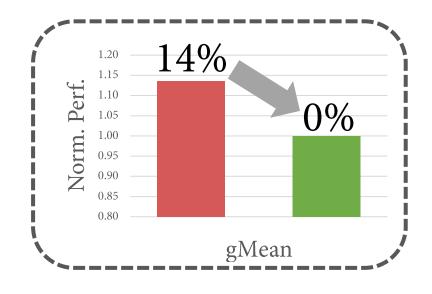






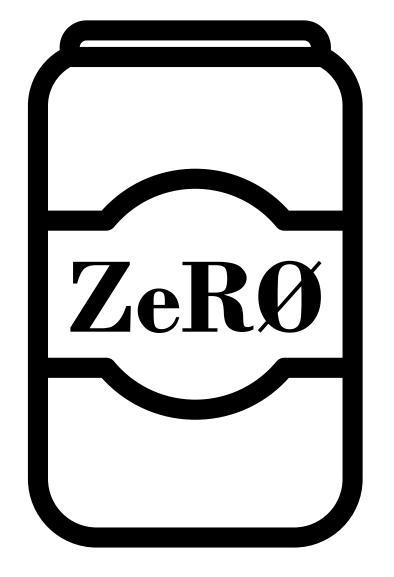
PAC's overheads are attributed to the extra QARMA encryption invocations upon pointer:

- loads/stores
- usages



ZeRØ reduces the average runtime overheads of pointer integrity from 14% to 0%!

An efficient pointer integrity mechanism



An ideal candidate for end-user deployment.

- **✓** Easy to Implement
- **✓** No Runtime Overheads
- **✓** Provides Strong Security

A drop-in replacement for ARM's PAC

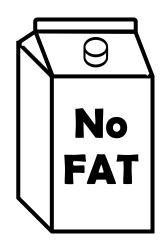
My solutions for C/C++ memory (un)safety

Memory Blocklisting









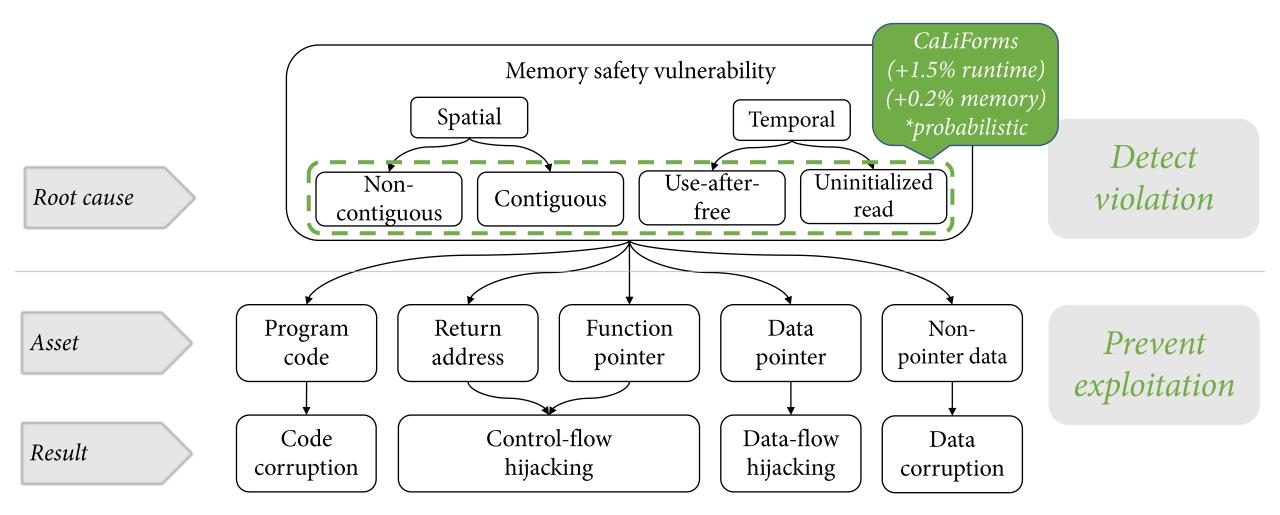


[MICRO 2019]

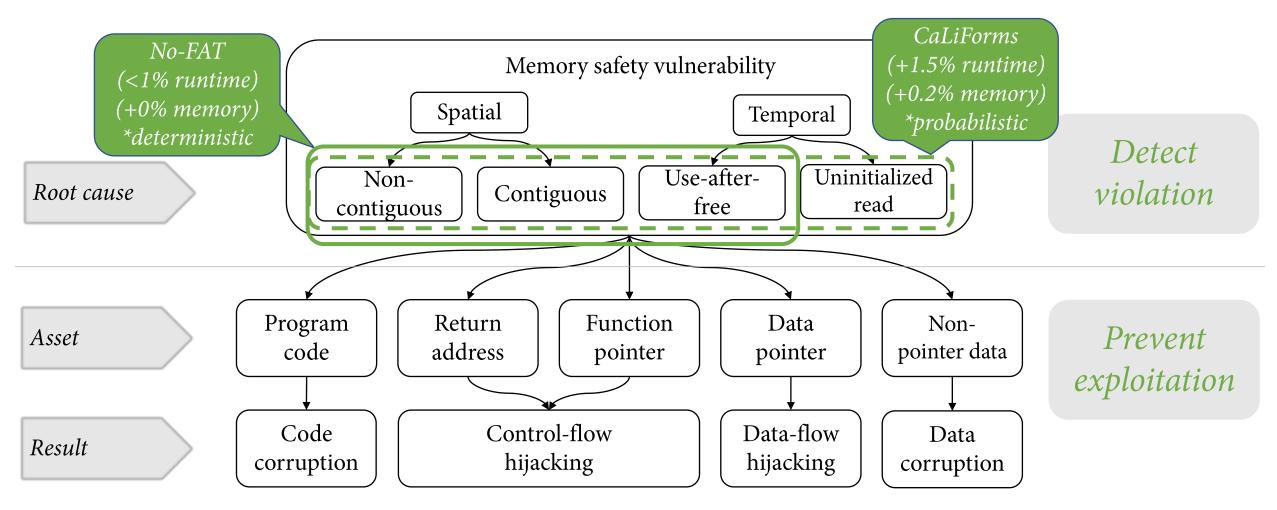
[ISCA 2021]

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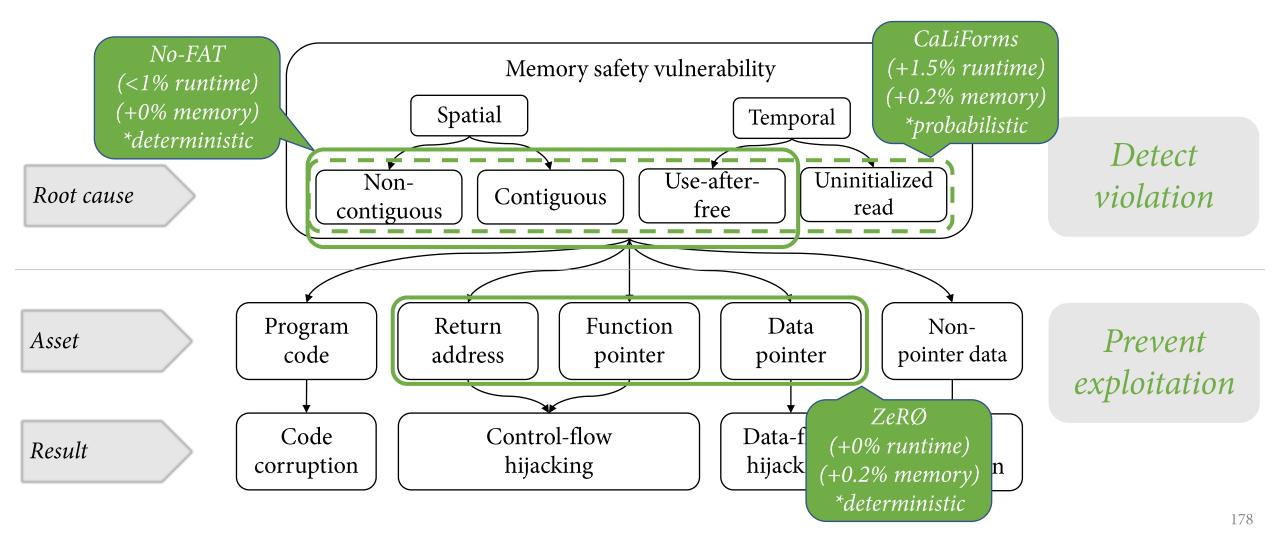
Memory Attacks Taxonomy



Memory Attacks Taxonomy



Memory Attacks Taxonomy



Acknowledgement



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Columbia University



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Columbia University



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Brown University



Kanad Sinha
Columbia University



Koustubha Bhat Vrije Universiteit Amsterdam



Ryan Piersma
Columbia University



Hiroshi Sasaki
Tokyo Institute of Technology

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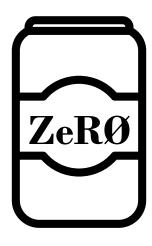
Exploit Mitigation



[MICRO 2019]



[ISCA 2021]



[ISCA 2021]

Thank You!