Luca Carloni

Curriculum Vitae

April 4, 2023

Professor and Chair of Computer Science

Department of Computer Science
Columbia University
1214 Amsterdam Avenue - Mail Code 0401
New York, NY 10027

Web: `http://www.cs.columbia.edu/~luca`
E-mail: `luca@cs.columbia.edu`
Phone: (212) 939-7043

FIELDS OF SPECIALIZATION

- Heterogeneous computing.
- System-on-chip platforms with emphasis on system-level design, intellectual property reuse, network-on-chip, high-level synthesis, and open-source hardware.
- Computer-aided design of integrated circuits and systems.
- Design methodologies and tools for embedded systems and embedded software.

ACADEMIC TRAINING

- **Ph.D. in Electrical Engineering and Computer Sciences** 2004
  University of California at Berkeley
  Major: Computer-Aided Design of Electronic Systems
  Minors: Integrated Circuits; Entrepreneurship
  Dissertation Title: *Latency-Insensitive Design*
  Advisor: Prof. Alberto L. Sangiovanni-Vincentelli
- **M.S. in Engineering** 1997
  University of California at Berkeley
  Dissertation Title: *Negative Thinking in Search Problems*
  Advisors: Prof. Alberto L. Sangiovanni-Vincentelli and Prof. Robert K. Brayton
- **B.S. Laurea *Summa Cum Laude* in Electrical Engineering** 1995
  ***Alma Mater Studiorum* University of Bologna, Italy**
  Dissertation Title: *Logic Synthesis for Low-Power Integrated Circuits*
  Advisor: Prof. Roberto Guerrieri

PROFESSIONAL POSITIONS HELD

- **Professor and Department Chair of Computer Science**, Columbia Univ.
  July 2021 - onwards
- **Professor of Computer Science**, Columbia Univ.
  July 2017 - June 2021
- **Associate Professor of Computer Science with Tenure**, Columbia Univ.
  Mar 2011 - June 2016
- **Associate Professor of Computer Science without Tenure**, Columbia Univ.
  Jan 2009 - Mar 2011
- **Assistant Professor of Computer Science**, Columbia Univ. Jul 2004 - Dec 2008

AWARDS AND HONORS

- Best paper award, *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)* 2020
- Columbia Provost Leadership Fellow 2019-21
- Qualcomm Faculty Award 2018
- Columbia *SEAS Interdisciplinary Research Seed (SIRS)* awards 2018
- Columbia *Research Initiatives in Science and Engineering (RISE)* award 2018
- Qualcomm Faculty Award 2017
- IEEE Fellow 2017
- National Academy of Engineering (NAE) EU-US *Frontiers of Engineering* symposium (60 engineers were selected worldwide) 2013
- Best paper award, *IEEE International Conference on Cloud Computing Technology and Science (CloudCom)* 2012
- Best paper award, *Conf. on Design, Automation and Test in Europe (DATE)* 2012
- IEEE Council on Electronic Design Automation (CEDA) *Early Career Award* 2012
- National Academy of Engineering (NAE) 17th annual U.S. *Frontiers of Engineering* symposium (85 engineers were selected nationwide) 2011
- Office of Naval Research (ONR) *Young Investigator Award* 2010
- Alfred P. Sloan Foundation *Research Fellow* 2008

- Best paper award, *High-Performance Embedded Computing (HPEC)* Workshop 2007
- NSF *Faculty Early Career Development (CAREER) Award* 2006
- "A Methodology for Correct-By-Construction Latency-Insensitive Design" was selected as one of the 42 papers from over 2,200 presented at the Intl. Conf. on Computer-Aided Design between 1983 and 2002 to be included in *"The Best of ICCAD - 20 Years of Excellence in Computer-Aided Design"* 2003
- UC Berkeley *Demetri Angelakos Memorial Achievement Award* in recognition of altruistic attitude towards fellow graduate students 2002

GRADUATE AND POST-GRADUATE ADVISING

- **Ph.D. Students Graduated**

1. Luca Piccolboni,
   Multi-Functional Interfaces for Accelerators
   Ph.D. in Computer Science, Columbia University 2022
   currently with Microsoft, New York, NY.
2. Jihye Kwon
   Machine Learning for AI-Augmented Design Space Exploration of Computer Systems
   Ph.D. in Computer Science, Columbia University 2022
   currently with Cadence Design Systems, San Jose, CA.
3. Davide Giri
   Agile Design of Many-Accelerator System-on-Chip Architectures
   Ph.D. in Computer Science, Columbia University 2022
   posthumously awarded.
4. Emilio Garcia Cota
   Scalable Emulation of Heterogeneous Systems
   Ph.D. in Computer Science, Columbia University 2019
   currently with Google, Inc., New York, NY.
5. Paolo Mantovani
   Scalable System-on-Chip Design
   Ph.D. in Computer Science, Columbia University 2018
   currently with Google Inc., New York, NY.
6. Young Jin Yoon
   Design and Optimization of Networks-on-Chip for Heterogeneous Systems-on-Chip
   Ph.D. in Computer Science, Columbia University 2017
   currently with Intel Corp., Hillsboro, OR.
7. YoungHoon Jung
   Design and Optimization of Mobile Cloud Computing Systems with Networked Virtual Platforms
   Ph.D. in Computer Science, Columbia University 2015
   currently with with XL8 Inc., San Jose, CA.
8. Hung-Yi Liu
   Supervised Design-Space Exploration
   Ph.D. in Computer Science, Columbia University 2015
   currently with Motivo, Inc. Chapel Hill, NC.
9. Marcin Szczodrak
   Multitasking on Wireless Sensor Networks
   Ph.D. in Computer Science, Columbia University 2015
   currently with Google Inc., Mountain View, CA.

10. Richard Neill
    Heterogeneous Cloud Systems Based on Broadband Embedded Computing
    Ph.D. in Computer Science, Columbia University 2013
    currently with Zodiac Interactive, New York, NY.
11. Rebecca Collins
    Data-Driven Programming Abstractions and Optimization for Multi-Core Platforms
    Ph.D. in Computer Science, Columbia University 2011
    currently with Google, Inc., New York, NY.
12. Cheng-Hong Li
    Methods for Performance Optimization of Latency-Insensitive Systems
    Ph.D. in Computer Science, Columbia University 2010
    currently with Google, Inc., New York, NY.

- **Postdoctoral Candidates Supervised**

1. Biruk Seyoum (Ph.D. Scuola Sant'Anna di Pisa) 2021-present
2. Christian Pilato (Ph.D. Politecnico di Milano) 2013-2016
   currently with Politecnico di Milano, Italy.
3. Giuseppe Di Guglielmo (Ph.D. Univ. of Verona) 2012-2013
   currently with Fermilab, Batavia, Illinois.
4. Johnnie Chan (Ph.D. Columbia Univ.) 2012-2014
   currently with Google, Kirkland, WA.
5. Nicola Concer (Ph.D. Univ. of Bologna) 2009-2012
   currently with NXP Laboratories, Eindovhen, The Netherlands.
6. Michele Petracca (Ph.D. Politecnico di Torino) 2009-2011
   currently with Cadence Design Systems, San Jose, CA.
7. Francesco Leonardi (Ph.D. Univ. of Trento) 2009-2011
   currently with Google, Seattle, WA.

- **Associate Research Scientists (financially supported)**

1. Giuseppe Di Guglielmo (Ph.D. Univ. of Verona) 2013-2022
2. Paolo Mantovani (Ph.D. Columbia University) 2017-2021

- **Current Graduate Advising**

1. Guy Eichler, Ph.D. student, Computer Science September 2018 onwards
2. Kuan-Lin Chiu, Ph.D. student, Computer Science September 2018 onwards
3. Maico Cassel, Ph.D. student, Computer Science September 2019 onwards
4. Joseph Zuckerman, Ph.D. student, Computer Science September 2019 onwards
5. Gabriele Tombesi, Ph.D. student, Computer Science January 2021 onwards

- **Visiting Scholars and Visiting Students**

1. Gabriele Tombesi, MS student
   Politecnico di Torino (Italy) — March 2020 - September 2020
2. Biruk Seyoum, Ph.D. student
   Scuola Sant'Anna di Pisa (Italy) — February 2020 - August 2020
3. Bernardita Alejandra Stitic Leiva, MS student
   Politecnico di Torino (Italy) — December 2019 - April 2020
4. Lorenzo Ferretti, Ph.D. student
   University of Svizzera Italiana (Switzerland) — January 2019 - August 2019
5. Carmelo Apostoliti, MS student
   Politecnico di Torino (Italy) — September 2018 - March 2019
6. Alexander Misdorp, MS student
   Delft University of Technology (Netherlands) — March 2018 - June 2019
7. Georgios Zacharopoulos, Ph.D. student
   University of Svizzera Italiana (Switzerland) — January 2018 - June 2018
8. Christian Palmiero, MS student
   Politecnico di Torino (Italy) — July 2017 - December 2017
9. Simone Rossi, MS student
   Politecnico di Torino (Italy) — July 2017 - December 2017
10. Robert Margelli, MS student
    Politecnico di Torino (Italy) — March 2017 - August 2017
11. Edoardo Degrassi, MS student
    Politecnico di Torino (Italy) — September 2016 - February 2017
12. Marco Geuna, MS student
    Politecnico di Torino (Italy) — September 2016 - February 2017
13. Francesco Viggiano, MS student
    Politecnico di Torino (Italy) — March 2016 - August 2016
14. Simone Palombi, MS student
    Politecnico di Torino (Italy) — March 2016 - August 2016
15. Carlos Moratelli, Ph.D. student
    PUC do Rio Grande do Sul (Brazil) — August 2014 - February 2015
16. Daniele Jahier Pagliari, MS student
    Politecnico di Torino (Italy) — March 2014 - August 2014
17. Luca Ramini, MS student
    University of Ferrara (Italy) — June 2011 - December 2011
18. Nicola Bombieri, associate research scientist
    University of Verona (Italy) — August 2011 - November 2011
19. Roberto Casu, associate research scientist
    Politecnico di Torino (Italy) — November 2010 - March 2011

PUBLICATIONS

My h-index is 49.

My total citation count is 9,545.

Citation counts are reported from `scholar.google.com` when exceeding twenty citations.
Acceptance rates are reported for refereed conference papers whenever available.
PDF files for most publications are available at `www.cs.columbia.edu/~luca/research`

- **Refereed Journal Papers**

[**J42**] L. Piccolboni, D. Giri, and L. P. Carloni. Accelerators & security: The socket approach. *IEEE Computer Architecture Letters*, 21(2):65–68, Jul-Dec 2022.

[**J41**] Y. Jwa, G. Giuseppe Di Guglielmo, L. Arnold, L. Carloni, and G. Karagiorgi. Real-time inference with 2d convolutional neural networks on field programmable gate arrays for high-rate particle imaging detectors. *Frontiers of Artificial Intelligence*, 5:855184, 2022.

[**J40**] M. Ricci, B. Stitic, Luca L. Urbinati, G. Di Guglielmo, J. Vasquez, J.A. Tobon, L. P. Carloni, F. Vipiana, and M.R. Casu. Machine-learning-based microwave sensing: A case study for the food industry. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 11(3):503–514, March 2021.

[**J39**] L. Ferretti, J. Kwon, G. Ansaloni, G. Di Guglielmo, L. P. Carloni, and L. Pozzi. DB4HLS: A database of high-level synthesis design space explorations. *IEEE Embedded Systems Letters*, 13(4):194–197, Jan-Jun 2021.

[**J38**] D. Giri, K.-L. Chiu, G. Eichler, P. Mantovani, and L. P. Carloni. Accelerator integration for open-source SoC design. *IEEE Micro*, 41(4):8–14, Jul-Aug 2021.

[**J37**] L. Ferretti, J. Kwon, G Ansaloni, G. Di Guglielmo, L. P. Carloni, and L. Pozzi. Leveraging prior knowledge for effective design-space exploration in high-level synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 39(11):3736–3747, November 2020.
Citations = 24.

[**J36**] Q. Cheng, J. Kwon, M. Glick, M. Bahadori, L. P. Carloni, and K. Bergman. Silicon photonics codesign for deep learning. *Proceedings of the IEEE*, 108(8):1261–1282, August 2020.
Citations = 60.

[**J35**] Z. Zhu, G. Di Guglielmo, Q. Cheng, M. Glick, J. Kwon, H. Guan, L. P. Carloni, and K. Bergman. Photonic switched optically connected memory: An approach to address memory challenges in deep learning. *IEEE/OSA Journal of Lightwave Technology*, 38(10):2815–2825, May 2020.

[**J34**] D. Giri, P. Mantovani, and L. P. Carloni. Accelerators and coherence: An SoC perspective. *IEEE Micro*, 38(6):36–45, Nov-Dec 2018.
Citations = 32.

[**J33**] L. Piccolboni, G. Di Guglielmo, and L. P. Carloni. PAGURUS: Low-overhead dynamic information flow tracking on loosely-coupled accelerators. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(11):2685–2696, November 2018.

[**J32**] L. Piccolboni, P. Mantovani, G. Di Guglielmo, and L. P. Carloni. COSMOS: Coordination of high-level synthesis and memory optimization for hardware accelerators. *ACM Transactions on Embedded Computing Systems*, 16(5s):150:1–150:22, September 2017.
Citations = 48.

[**J31**] C. Pilato, P. Mantovani, G. Di Guglielmo, and L. P. Carloni. System-level optimization of accelerator local memory for heterogeneous systems-on-chip. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 36(3):435–448, March 2017.
Citations = 39.

[**J30**] D. Jahier Pagliari, M. R. Casu, and L. P. Carloni. Acceleration for breast cancer detection. *ACM Transactions on Embedded Computing Systems*, 16(3):80:1–80:25, March 2017.

[**J29**] L. P. Carloni. From latency-insensitive design to communication-based system-level design. *Proceedings of the IEEE*, 103(11):2133–2151, November 2015.
Citations = 56.

[**J28**] R. K. Brayton, L. P. Carloni, A. L. Sangiovanni-Vincentelli, and T. Villa. Design automation of electronic systems: Past accomplishments and challenges ahead [scanning the issue]. *Proceedings of the IEEE*, 103(11):1952–1957, November 2015.

[**J27**] R. Margolies, M. Gorlatova, J. Sarik, G. Stanje, J. Zhu, P. Miller, M. Szczodrak, B. Vigraham, L. P. Carloni, P. R. Kinget, I. Kymissis, and G. Zussman. Energy harvesting active networked tags (EnHANTs): Prototyping and experimentation. *ACM Transactions on Sensor Networks*, 11(4):62:1–26, November 2015.
Citations = 48.

[**J26**] Y. Jung and L. P. Carloni. Cloud-aided design for distributed embedded systems. *IEEE Design & Test*, 31(3):32–40, May-Jun 2014.

[**J25**] E. G. Cota, P. Mantovani, M. Petracca, M. Casu, and L. P. Carloni. Accelerator memory reuse in the dark silicon era. *IEEE Computer Architecture Letters*, 13(1):9–12, Jan-Jun 2014.
Citations = 27.

[**J24**] Y. J. Yoon, N. Concer, and L. P. Carloni. Virtual channels and multiple physical networks: Two alternatives to improve NoC performance. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 32(12):1906–1919, December 2013.
Citations = 63.

[**J23**] R. Collins and L. P. Carloni. Flexible filters in stream programs. *ACM Transactions on Embedded Computing Systems*, 13(3):45:1–45:26, December 2013.

[**J22**] N. Sturcken, E. J. O'Sullivan, N. Wang, P. Herget, B. Webb, L.T. Romankiw, M. Petracca, R. Davies, R. Fontana, G. M. Decad, I. Kymissis, A. V. Peterchev, L.P. Carloni, W.J. Gallagher, and K.L. Shepard. A 2.5D integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer. *IEEE Journal of Solid-State Circuits*, 48(1):244–254, January 2013.
Citations = 156.

[**J21**] N. Sturcken, M. Petracca, S. Warren, P. Mantovani, L.P. Carloni, A.V. Peterchev, and K.L. Shepard. A switched-inductor integrated voltage regulator with nonlinear feedback and NoC load in 45nm SOI. *IEEE Journal of Solid-State Circuits*, 47(8):1935–1945, August 2012.
Citations = 72.

[**J20**] J. Chan, G. Hendry, K. Bergman, and L. P Carloni. Physical-layer modeling and system-level design of chip-scale photonic interconnection networks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 30(10):1507–1520, October 2011.
Citations = 145.

[**J19**] G. Hendry, E. Robinson, V. Gleyzer, J. Chan, L. P Carloni, N. Bliss, and K. Bergman. Time-division-multiplexed arbitration in silicon nanophotonic networks-on-chip for high-performance chip multiprocessors. *Journal of Parallel and Distributed Computing*, 71(5):641–650, May 2011.
Citations = 51.

[**J18**] N. Concer, L. Bononi, M. Soulie, R. Locatelli, and L. P. Carloni. The connection-then-credit flow control protocol for heterogeneous multi-core systems-on-chip. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 29(6):869–882, June 2010.
Citations = 25.

[**J17**] L. P. Carloni, A. B Kahng, S. Muddu, A. Pinto, K. Samadi, and P. Sharma. Accurate predictive interconnect modeling for system-level design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 18(4):679–684, April 2010.
Citations = 10.

[**J16**] M. Petracca, B. G. Lee, K. Bergman, and L. P. Carloni. Photonic NoCs: System-level design exploration. *IEEE Micro*, 29(4):74–85, Jul-Aug 2009.
Selected for special issue on Top Picks from the 16th Annual IEEE Symposium on High-Performance Interconnects (HotI)
Citations = 51.

[**J15**] A. Pinto, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. A methodology for constrained-driven synthesis of on-chip communications. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 28(3):364–377, March 2009.
Citations = 24.

[**J14**] C.-H. Li and L. P. Carloni. Leveraging local intra-core information to increase global performance in block-based design of systems-on-chip. *IEEE Transactions*

on Computer-Aided Design of Integrated Circuits and Systems, 28(2):165–178, February 2009.
Citations = 12.

[J13] R. Collins and L. P. Carloni. Topology-based performance analysis and optimization of latency-insensitive systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(12):2277–2290, December 2008.
Citations = 12.

[J12] A. Shacham, K. Bergman, and L. P. Carloni. Photonic networks-on-chip for future generations of chip multi-processors. *IEEE Transactions on Computers*, 57(9):1246–1260, September 2008.
Citations = 1050.

[J11] A. Pinto, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. COSI: A framework for the design of interconnection networks. *IEEE Design & Test of Computers*, 25(5):402–415, Sep-Oct 2008.
Citations = 27.

[J10] A. Benveniste, B. Caillaud, L. P. Carloni, P. Caspi, and A. L. Sangiovanni-Vincentelli. Composing heterogeneous reactive systems. *ACM Transactions on Embedded Computing Systems*, 7(4):1–36, July 2008.
Citations = 53.

[J9] C. Pinello, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Fault-tolerant distributed deployment of embedded control software. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(5):906–919, May 2008.
Citations = 46.

[J8] A. Bonivento, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Platform-based design for wireless sensor networks. *Mobile Networks and Applications, The Journal of Special Issues on Mobility of Systems, Users, Data and Computing*, 11(4):469–485, August 2006.
Citations = 50.

[J7] L. P. Carloni, R. Passerone, A. Pinto, and A. L. Sangiovanni-Vincentelli. Languages and tools for hybrid systems design. *Foundations and Trends in Electronic Design Automation*, 1(1-2):1–194, July 2006.
Citations = 241.

[J6] L. P. Carloni and A. L. Sangiovanni-Vincentelli. A framework for modeling the distributed deployment of synchronous designs. *Journal of Formal Methods in System Design*, 28(2):93–110, March 2006.
Citations = 10.

[J5] L. P. Carloni and A. L. Sangiovanni-Vincentelli. Coping with latency in SOC design. *IEEE Micro*, 22(5):24–35, Sep-Oct 2002.
Citations = 184.

[J4] L. P. Carloni, K. L. McMillan, and A. L. Sangiovanni-Vincentelli. Theory of latency-insensitive design. *IEEE Transactions on Computer-Aided Design of*

Integrated Circuits and Systems, 20(9):1059–1076, September 2001.
Citations = 538.

[J3] E. I. Goldberg, L. P. Carloni, T. Villa, R. K. Brayton, and A. L. Sangiovanni-Vincentelli. Negative thinking in branch-and-bound: the case of unate covering. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 19(3):281–294, March 2000.
Citations = 24.

[J2] E. Charbon, P. Miliozzi, L. P. Carloni, A. Ferrari, and A. L. Sangiovanni-Vincentelli. Modeling digital substrate noise injection in mixed-signal ICs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 18(3):301–310, March 1999.
Citations = 104.

[J1] A. L. Oliveira, L. P. Carloni, T. Villa, and A. L. Sangiovanni-Vincentelli. Exact minimization of binary decision diagrams using implicit techniques. *IEEE Transactions on Computers*, 47(11):1282–1296, November 1998.
Citations = 36.

- **Refereed Conference Papers**

[C118] T. Tambe, J. Zhang, C. Hooper, T. Jia, P. N. Whatmough, J. Zuckerman, M. Cassel, E. J. Loscalzo, D. Giri, K. L. Shepard, L. P. Carloni, A. M. Rush, D. Brooks, and G.-Y. Wei. A 12nm 18.1TFLOPs/W sparse transformer processor with entropy-based early exit, mixed-precision predication and fine-grained power management. In *ISSCC Digest of Technical Papers*, pages 342–343, 2023.
Acceptance Rate = 30%.

[C117] B. Seyoum, D. Giri, K.-L. Chiu, and L. P. Carloni. An open-source platform for design and programming of partially reconfigurable heterogeneous SoCs. In *Proceedings of the International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, pages 25–26, October 2022.

[C116] T. Jia, P. Mantovani, M. Cassel Dos Santos, D. Giri, J. Zuckerman, E. J. Loscalzo, M. Cochet, K. Swaminathan, G. Tombesi, J. J. Zhang, N. Chandramoorthy, J.-D. Wellman, K. Tien, L.P. Carloni, K. Shepard, D. Brooks, G.-Y. Wei, and P. Bose. A 12nm agile-designed SoC for swarm-based perception with heterogeneous IP blocks, a reconfigurable memory hierarchy, and an 800MHz multiplane NoC. In *Proceedings of the 48th European Solid-State Circuits Conference*, September 2022.

[C115] D. Xu, A. B. Ozguler, G. Di Guglielmo, N. Tran, G. N. Perdue, L. Carloni, and F. Fahim. Neural network accelerator for quantum control. In *IEEE/ACM Third International Workshop on Quantum Computing Software (QCS)*, pages 43–49, November 2022.

[C114] J. Zuckerman, P. Mantovani, and L. P. Carloni. Enabling heterogeneous, multicore SoC research with RISC-V and ESP. In *The Proceedings of the Workshop on Computer Architecture Research with RISC-V (CARRV)*, May 2022.

[C113] G. Eichler, L. Piccolboni, D. Giri, and L. P. Carloni. MasterMind: many-accelerator SoC architecture for real-time brain-computer interfaces. In *Proceedings of the International Conference on Computer Design (ICCD)*, pages 101–108, October 2021.

Acceptance Rate = 24.4%.

[C112] J. Zuckerman, D. Giri, J. Kwon, P. Mantovani, and L. P. Carloni. Cohmeleon: Learning-based orchestration of accelerator coherence in heterogeneous SoCs. In *Proceedings of the IEEE/ACM International Symposium on Microarchitecture*, pages 350–365, October 2021.

Acceptance Rate = 22%.

[C111] S. Chattopadhyay, F. Lonsing, L. Piccolboni, D. Soni, P. Wei, X. Zhan, Y. Zhou, L. Carloni, D. Chen, J. Cong, R. Karri, Z. Zhang, C. Trippel, C. Barrett, and S. Mitra. Scaling up hardware accelerator verification using A-QED with functional decomposition. In *Formal Methods in Computer Aided Design (FMCAD)*, pages 42–52, October 2021.

[C110] L. Piccolboni, G. Di Guglielmo, S. Sethumadhavan, and L. P. Carloni. HARDROID: Transparent integration of crypto accelerators in Android. In *IEEE High Performance Extreme Computing Conference (HPEC)*, pages 1–6, September 2021.

[C109] L. Piccolboni, G. Di Guglielmo, L. P. Carloni, and S. Sethumadhavan. CRYLOGGER: detecting crypto misuses dynamically. In *IEEE Symposium on Security and Privacy*, May 2021.

Citations = 22. Acceptance Rate = 104/841 = 12.3%.

[C108] Farah Fahim, Benjamin Hawks, Christian Herwig, James Hirschauer, Sergo Jindariani, Nhan Tran, Luca Carloni, Giuseppe Di Guglielmo, Philip Harris, Jeffrey Krupa, Dylan Rankin, Manuel Blanco Valentin, Josiah Hester, Yingyi Luo, John Mamish, Seda Memik, Thea Aarrestad, Hamza Javed, Vladimir Loncar, Maurizio Pierini, Adrian Alan Pol, Sioni Summers, Javier Duarte, Scott Hauck, Shih-Chieh Hsu, Jennifer Ngadiuba, Mia Liu, Duc Hoang, Edward Kreinar, and Zhenbin Wu. hls4ml: an open-source co-design workflow to empower scientific low-power machine learning devices. In *tinyML 2021 Research Symposium*, pages 1–8, March 2021.

Citations = 56.

[C107] J. Kwon and L. P. Carloni. Transfer learning for design-space exploration with high-level synthesis. In *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, pages 218:1–218:6, November 2020.

Best Paper Award.

Citation = 25.

[C106] M. Hattink G. Di Guglielmo, L. P. Carloni, and K. Bergman. A scalable architecture for CNN accelerators leveraging high-performance memories. In *IEEE High Performance Extreme Computing Conference (HPEC)*, pages 1–6, September 2020.

[C105] O. Matthews, J. L. Aragon, T. J. Ham, D. Giri, A. Manocha, T. Sorensen, M. Orenes Vera, E. Tureci, L. P. Carloni, and M. Martonosi. MosaicSim: A lightweight, modular simulator for heterogeneous systems. In *The Proceedings of the International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pages 136–148, August 2020.

[C104] D. Giri, K.-L. Chiu, G. Eichler, P. Mantovani, N. Chandramoorthy, and L. P. Carloni. Ariane + NVDLA: seamless third-party IP integration with ESP. In *The Proceedings of the Workshop on Computer Architecture Research with RISC-V (CARRV)*, May 2020.

[C103] D. Giri, K.-L. Chiu, G. Di Guglielmo, P. Mantovani, and L. P. Carloni. ESP4ML: platform-based design of systems-on-chip for embedded machine learning. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 1049–1054, March 2020.
Citations = 35. Acceptance Rate = 194/748 = 26%.

[C102] P. Mantovani, R. Margelli, D. Giri, and L. P. Carloni. HL5: A 32-bit RISC-V processor designed with high-level synthesis. In *Proceedings Custom Integrated Circuits Conference (CICC)*, pages 1–8, March 2020.

[C101] G. Zacharopoulos, L. Ferretti, G. Ansaloni, G. Di Guglielmo, L. Carloni, and L. Pozzi. Compiler-assisted selection of hardware acceleration candidates from application source code. In *Proceedings of the International Conference on Computer Design (ICCD)*, November 2019.

[C100] L. Piccolboni, G. Di Guglielmo, and L. P. Carloni. KAIROS: incremental verification in high-level synthesis through latency-insensitive design. In *Formal Methods in Computer Aided Design (FMCAD)*, pages 105–109, October 2019.
Acceptance Rate = 27/61 = 44%.

[C99] K. Bhardwaj, P. Mantovani, L. P. Carloni, and S. M. Nowick. Towards a complete methodology for synthesizing bundled-data asynchronous circuits on FPGAs. In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, pages 180–185, August 2019.

[C98] L. P. Carloni, E. G. Cota, G. Di Guglielmo, D. Giri, J. Kwon, P. Mantovani, L. Piccolboni, and M. Petracca. Teaching heterogeneous computing with system-level design methods. In *Workshop on Computer Architecture Education (WCAE)*, pages 4:1–4:8, June 2019.

[C97] Y.-J. Jwa, G. Di Guglielmo, L. P. Carloni, and G. Karagiorgi. Accelerating deep neural networks for real-time data selection for high-resolution imaging particle detectors. In *The Proceeding of the New York Scientific Data Summit (NYSDS)*, pages 1–10, June 2019.

[C96] J. Kwon, M. Ziegler, and L. P. Carloni. A learning-based recommender system for autotuning design flows of industrial high-performance processors. In *Proceedings of the Design Automation Conference (DAC)*, pages 218:1–218:6, Las Vegas, NV, June 2019.
Citations = 31. Acceptance Rate = 202/815 = 25%.

[**C95**] L. Piccolboni, G. Di Guglielmo, and L. P. Carloni. Securing accelerators with dynamic information flow tracking. In *IEEE International Symposium on Hardware Oriented Security and Trust (HOST) - Hardware Demo*, May 2019.

[**C94**] E. G. Cota and L. P. Carloni. Cross-ISA machine instrumentation using fast and scalable dynamic binary translation. In *ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments (VEE)*, pages 74–87, April 2019.
Citations = 32. Acceptance Rate = 15/33 = 45%.

[**C93**] D. Giri, P. Mantovani, and L. P. Carloni. NoC-based support of heterogeneous cache-coherence models for accelerators. In *Proceedings of the Twelfth International Symposium on Networks-on-Chip (NOCS)*, pages 1:1–1:6, October 2018.
Citations = 26.

[**C92**] C. Palmiero, G. Di Guglielmo, L. Lavagno, and L. P. Carloni. Design and implementation of a dynamic information flow tracking architecture to secure a RISC-V core for IoT applications. In *IEEE High Performance Extreme Computing Conference (HPEC)*, pages 1–7, September 2018.
Citations = 35.

[**C91**] C. Pilato and L. P. Carloni. DarkMem: fine-grained power management of local memories for accelerators in embedded systems. In *Proceedings of the Asia and South Pacific Design Automation Conference (ASPDAC)*, pages 696–701, January 2018.

[**C90**] L. Piccolboni, P. Mantovani, G. Di Guglielmo, and L. P. Carloni. Broadening the exploration of the accelerator design space in embedded scalable platforms. In *IEEE High Performance Extreme Computing Conference (HPEC)*, pages 1–7, September 2017.

[**C89**] E. G. Cota, P. Bonzini, A. Bennee, and L. P. Carloni. Cross-ISA machine emulation for multicores. In *Proceedings of the International Symposium on Code Generation and Optimization (CGO)*, pages 210–220, February 2017.
Acceptance Rate = 26/114 = 22%.

[**C88**] P. Mantovani, E. G. Cota, C. Pilato, G. Di Guglielmo, and L. P. Carloni. Handling large data sets for high-performance embedded applications in heterogeneous systems-on-chip. In *Proceedings of the International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, pages 1–10, October 2016.
Citations = 34. Acceptance Rate = 28.5%.

[**C87**] M. Ziegler, H.-Y. Liu, and L. P. Carloni. Scalable auto-tuning of synthesis parameters for optimizing high-performance processors. In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, pages 180–185, August 2016.
Citations = 23.

[**C86**] P. Mantovani, E. G. Cota, K. Tien, C. Pilato, G. Di Guglielmo, K. Shepard, and L. P. Carloni. An FPGA-based infrastructure for fine-grained DVFS analysis

in high-performance embedded systems. In *Proceedings of the Design Automation Conference (DAC)*, pages 157:1–157:6, Austin, TX, June 2016.
Citations = 45. Acceptance Rate = 29%.

[C85] E. G. Cota, P. Mantovani, and L. P. Carloni. Exploiting private local memories to reduce the opportunity cost of accelerator integration. In *Proceedings of the ACM International Conference on Supercomputing*, pages 27:1–27:12, Istanbul, Turkey, June 2016.
Acceptance Rate = 24.2%.

[C84] M. Ziegler, H.-Y. Liu, G. Gristede, B. Owens, R. Nigaglioni, and L. P. Carloni. A synthesis-parameter tuning system for autonomous design-space exploration. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 1148–1151, March 2016.
Citations = 40. Acceptance Rate = 24%.

[C83] D. Jahier Pagliari, A. Pulimeno, J. A. Tobon, M. Vacca, F. Vipiana, M. R. Casu, R. Solimene, and L. P. Carloni. A low-cost, fast, and accurate microwave imaging system for breast cancer detection. In *Biomedical Circuits and Systems Conference (BioCAS)*, Atlanta, GA, October 2015.
Citations = 23.

[C82] D. Jahier Pagliari, M. R. Casu, and L. P. Carloni. Acceleration of microwave imaging algorithms for breast cancer detection via high-level synthesis. In *Proceedings of the International Conference on Computer Design (ICCD)*, pages 475–478, New York, NY, October 2015.

[C81] E. G. Cota, P. Mantovani, G. Di Guglielmo, and L. P. Carloni. An analysis of accelerator coupling in heterogeneous architectures. In *Proceedings of the Design Automation Conference (DAC)*, pages 202:1–202:6, San Francisco, CA, June 2015.
Citations = 85. Acceptance Rate = 20.5%.

[C80] Y. Jung and L. P. Carloni. ΣVP: Host-GPU multiplexing for efficient simulation of multiple embedded GPUs on virtual platforms. In *Proceedings of the Design Automation Conference (DAC)*, pages 106:1–106:6, San Francisco, CA, June 2015.
Acceptance Rate = 20.5%.

[C79] K. Tien, N. Sturcken, N. Wang, J.-W. Nah, B. Dang, E. O'Sullivan, P. Andry, M. Petracca, L. P. Carloni, W. Gallagher, and K. Shepard. An 82%-efficient multiphase voltage-regulator 3D interposer with on-chip magnetic inductors. In *Symposium on VLSI Circuits*, pages C192–C193, June 2015.
Citations = 20.

[C78] Y. Jung, K. Stratos, and L. P. Carloni. LN-Annote: an alternative approach to information extraction from emails using locally-customized named-entity recognition. In *Proceedings of the 24th International Conference on World Wide Web (WWW)*, pages 538–548, Florence, Italy, May 2015.
Acceptance Rate = 22%.

[C77] J. Brooks, S. Goyal, R. Subramany, Y. Lin, T. Middelkoop, L. Arpan, L. Carloni, and P. Barooah. An experimental investigation of occupancy-based energy-efficient control of commercial building indoor climate. In *IEEE Conference on Decision and Control (CDC)*, pages 5680–5685, Los Angeles, CA, December 2014.
Citations = 42.

[C76] C. Pilato, P. Mantovani, G. Di Guglielmo, and L. P. Carloni. System-level memory optimization for high-level synthesis of component-based SoCs. In *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pages 18:1–18:10, New Delhi, India, October 2014.
Citations = 22. Acceptance Rate = 30/117 = 26%.

[C75] G. Di Guglielmo, C. Pilato, and L. P. Carloni. A design methodology for compositional high-level synthesis of communication-centric SoCs. In *Proceedings of the Design Automation Conference (DAC)*, pages 128:1–128:6, San Francisco, CA, June 2014.
Acceptance Rate = 22%.

[C74] M. Szczodrak, O. Gnawali, and L. P. Carloni. Modeling and implementation of energy neutral sensing systems. In *International Workshop on Energy Neutral Sensing Systems (ENSSyS)*, pages 9:1–9:6, November 2013.

[C73] H.-Y. Liu and L. P. Carloni. On learning-based methods for design-space exploration with high-level synthesis. In *Proceedings of the Design Automation Conference (DAC)*, Austin, TX, June 2013.
Citations = 219. Acceptance Rate = 162/747 = 21.7%.

[C72] Y. Jung, J. Park, M. Petracca, and L. P. Carloni. netShip: a networked virtual platform for large-scale heterogeneous distributed embedded system. In *Proceedings of the Design Automation Conference (DAC)*, Austin, TX, June 2013.
Citations = 21. Acceptance Rate = 162/747 = 21.7%.

[C71] N. Bombieri, H.-Y. Liu, F. Fummi, and L. P. Carloni. A method to abstract RTL IP blocks into C++ code and enable high-level synthesis. In *Proceedings of the Design Automation Conference (DAC)*, Austin, TX, June 2013.
Acceptance Rate = 162/747 = 21.7%.

[C70] M. Szczodrak, Y. Yang, D. Cavalcanti, and L. P. Carloni. An open framework to deploy heterogeneous wireless testbeds for cyber-physical systems. In *IEEE Symposium on Industrial Embedded Systems (SIES)*, pages 215–224, June 2013.
Citations = 24.

[C69] M. Szczodrak, O. Gnawali, and L. P. Carloni. Dynamic reconfiguration of wireless sensor networks to support heterogeneous applications. In *IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS)*, pages 52–61, May 2013.
Citations = 45.

[C68] D. Whelihan, J. J. Hughes, S. M. Sawyer, E. Robinson, M. Wolf, S. Mohindra, J. Mullen, A. Klein, M. S. Beard, N. T. Bliss, J. Chan, R. Hendry, K. Bergman,

and L. P. Carloni. P-sync: a photonically enabled architecture for efficient non-local data access. In *IEEE International Symposium on Parallel and Distributed Processing (IPDPS)*, pages 189–200, May 2013.

Acceptance Rate = 21%.

[C67] M. Gorlatova, R. Margolies, J. Sarik, G. Stanje, J. Zhu, B. Vigraham, M. Szczodrak, L. P. Carloni, P. R. Kinget, I. Kymissis, and G. Zussman. Prototyping energy harvesting active networked tags (EnHANTs). In *Proceedings of the IEEE INFOCOM*, pages 585–589, April 2013.

Citations = 42.

[C66] Y. Jung, R. Neill, and L. P. Carloni. A broadband embedded computing system for MapReduce utilizing Hadoop. In *The Proceedings of the IEEE International Conference on Cloud Computing Technology and Science (CloudCom)*, pages 1–9, December 2012.

Best Paper Award.

Citations = 12. Acceptance Rate = 54/318 = 17%.

[C65] Y. J. Yoon, N. Concer, and L. P. Carloni. VENTTI: a vertically integrated framework for simulation and optimization of networks-on-chip. In *IEEE International System-on-Chip Conference*, pages 171–176, September 2012.

[C64] L. Ramini, D. Bertozzi, and L. P. Carloni. Engineering a bandwidth-scalable optical layer for a 3D multi-core processor with awareness of layout constraints. In *Proceedings of the Sixth International Symposium on Networks-on-Chip (NOCS)*, pages 185–192, Copenhagen, Denmark, May 2012.

Citations = 39.

[C63] H.-Y. Liu, M. Petracca, and L. P. Carloni. Compositional system-level design exploration with planning of high-level synthesis. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 641–646, Dresden, Germany, March 2012.

Best Paper Award.

Citations = 52. Acceptance Rate = 27%.

[C62] N. Sturcken, E. J. O'Sullivan, N. Wang, P. Herget, B. Webb, L. T. Romankiw, M. Petracca, R. Davies, R. Fontana, G. M. Decad, I. Kymissis, A. V. Peterchev, L. P. Carloni, W. J. Gallagher, and K. L. Shepard. A 2.5D integrated voltage regulator using coupled magnetic core inductors on silicon interposer delivering $10.8\text{A}/mm^2$. In *ISSCC Digest of Technical Papers*, pages 400–402, February 2012.

Citations = 91.

[C61] M. Szczodrak and L. P. Carloni. A complete framework for programming event-driven, self-reconfigurable low power wireless networks. In *International Conference on Embedded Networked Sensor Systems (SenSys)*, pages 415–416, November 2011.

Citations = 10.

[C60] G. Stanje, P. Miller, J. Zhu, A. Smith, O. Winn, R. Margolies, M. Gorlatova, J. Sarik, M. Szczodrak, B. Vigraham, L. P. Carloni, P. R. Kinget, I. Kymissis,

and G. Zussman. Organic solar cell-equipped energy harvesting active networked tag EnHANT prototypes. In *International Conference on Embedded Networked Sensor Systems (SenSys)*, pages 385–386, November 2011.
Citations = 15.

[C59] R. Neill, L. P. Carloni, A. Shabarshin, V. Sigaev, and S. Tcherepanov. Embedded processor virtualization for broadband grid computing. In *The Proceedings of the 12th IEEE/ACM International Conference on Grid Computing (Grid)*, pages 145–156, Lyon, France, September 2011.
Acceptance Rate = 26/89 = 29.2%.

[C58] N. Sturcken, M. Petracca, S. Warren, L.P. Carloni, A.V. Peterchev, and K.L. Shepard. An integrated four-phase buck converter delivering $1A/mm2$ with $700ps$ controller delay and network-on-chip load in 45-nm SOI. In *Proceedings Custom Integrated Circuits Conference (CICC)*, pages 1–4, 2011.
Citations = 25.

[C57] N. Concer, A. Vesco, R. Scopigno, and L. P. Carloni. A dynamic and distributed TDM slot-scheduling protocol for QoS-oriented networks-on-chip. In *Proceedings of the International Conference on Computer Design (ICCD)*, pages 31–38, October 2011.
Acceptance Rate = 57/206 = 27.7%.

[C56] H.-Y. Liu, I. Diakonikolas, M. Petracca, and L. P. Carloni. Supervised design space exploration by compositional approximation of Pareto sets. In *Proceedings of the Design Automation Conference (DAC)*, pages 399–404, San Diego, CA, June 2011.
Citations = 22. Acceptance Rate = 156/690 = 22.6%.

[C55] J. Zhu, G. Stanje, R. Margolies, M. Gorlatova, J. Sarik, Z. Noorbhaiwala, P. Miller, M. Szczodrak, B. Vigraham, L. P. Carloni, P. R. Kinget, I. Kymissis, and G. Zussman. Demo: prototyping UWB-enabled Enhants. In *International Conference on Mobile Systems, Applications, and Services (MobiSys)*, pages 387–388, June 2011.
Citations = 11.

[C54] F. Leonardi, A. Pinto, and L. P. Carloni. Synthesis of distributed execution platforms for cyber-physical systems with applications to high-performance buildings. In *International Conference on Cyber-Physical Systems (ICCPS)*, pages 215–224, Chicago, Illinois, April 2011.
Citations = 15. Acceptance Rate = 21/78 = 26.9%.

[C53] G. Hendry, J. Chan, K. Bergman, and L. P. Carloni. Vandal: A tool for the design specification of nanophotonic networks. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 782–787, Grenoble, France, March 2011.
Citations = 23. Acceptance Rate = 200/789 = 25.3%.

[C52] G. Hendry, E. Robinson, V. Gleyzer, J. Chan, L. P. Carloni, N. Bliss, and K. Bergman. Circuit-switched memory access in photonic interconnection net-

works for high-performance embedded computing. In *Proceedings of the ACM/-IEEE Conference on High Performance Computing*, pages 1–12, New Orleans, LO, November 2010.
Citations = 60. Acceptance Rate = 51/253 = 20.2%.

[C51] R. Collins and L. P. Carloni. Flexible filters for high-performance embedded computing. In *Proceedings of the Tenth Annual Workshop on High Performance Embedded Computing (HPEC)*, September 2010.

[C50] G. Hendry, J. Chan, S. Kamil, L. Oliker, J. Shalf, L. P. Carloni, and K. Bergman. Silicon nanophotonic network-on-chip using TDM arbitration. In *Proceedings of the 18th Annual IEEE Symposium on High-Performance Interconnects (HotI)*, pages 88–95, Stanford University, CA, August 2010.
Citations = 64.

[C49] Y. J. Yoon, N. Concer, M. Petracca, and L. P. Carloni. Virtual channels vs. multiple physical networks: A comparative analysis. In *Proceedings of the Design Automation Conference (DAC)*, pages 162–165, Anaheim, CA, June 2010.
Citations = 96. Acceptance Rate = 148/607 = 24.4%.

[C48] R. Neill, A. Shabarshin, and L. P. Carloni. A heterogeneous parallel system running Open MPI on a broadband network of embedded set-top devices. In *ACM International Conference on Computing Frontiers*, pages 187–196, Bertinoro, Italy, May 2010.
Citations = 12. Acceptance Rate = 30/113 = 26.5%.

[C47] C.-H. Li, S. Sonalkar, and L. P. Carloni. Exploiting local logic structures to optimize multi-core SoC floorplanning. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 1291–1296, Dresden, Germany, March 2010.
Acceptance Rate = 258/980 = 26.3%.

[C46] J. Chan, G. Hendry, A. Biberman, K. Bergman, and L. P. Carloni. PhoenixSim: A simulator for physical-layer analysis of chip-scale photonic interconnection networks. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 691–696, Dresden, Germany, March 2010.
Citations = 172. Acceptance Rate = 258/980 = 26.3%.

[C45] R. Collins, B. Vellore, and L. P. Carloni. Recursion-driven parallel code generation for multi-core platforms. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 190–195, Dresden, Germany, March 2010.
Citations = 20. Acceptance Rate = 258/980 = 26.3%.

[C44] R. Collins and L. P. Carloni. Flexible filters: Load balancing through backpressure for stream programs. In *EMSOFT'09: Proceedings of the Ninth ACM & IEEE International Conference on Embedded Software*, pages 205–214, Grenoble, France, October 2009.
Citations = 43. Acceptance Rate = 33/106 = 31.1%.

[C43] L. P. Carloni, P. Pande, and Y. Xie. Networks-on-chip in emerging interconnect paradigms: Advantages and challenges. In *Proceedings of the Third International Symposium on Networks-on-Chip (NOCS)*, pages 93–102, San Diego, CA, May 2009.
Citations = 230. Acceptance Rate = 29/126 = 23.0%.

[C42] N. Concer, L. Bononi, M. Soulie, R. Locatelli, and L. P. Carloni. CTC: an end-to-end flow control protocol for multi-core systems-on-chip. In *Proceedings of the Third International Symposium on Networks-on-Chip (NOCS)*, pages 193–202, San Diego, CA, May 2009.
Citations = 24. Acceptance Rate = 29/126 = 23.0%.

[C41] G. Hendry, S. Kamil, A. Biberman, J. Chan, B. Lee, M. Mohiyuddin, A. Jain, K. Bergman, L. P. Carloni, J. Kubiatowicz, L. Oliker, and J. Shalf. Analysis of photonic networks for a chip multi-processor using scientific applications. In *Proceedings of the Third International Symposium on Networks-on-Chip (NOCS)*, pages 104–113, San Diego, CA, May 2009.
Citations = 88. Acceptance Rate = 29/126 = 23.0%.

[C40] F. Leonardi, A. Pinto, and L. P. Carloni. A case study in distributed deployment of embedded software for camera networks. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 1006–1011, Nice, France, April 2009.
Acceptance Rate = 211/844 = 25.0%.

[C39] N. Concer, M. Petracca, and L. P. Carloni. Distributed flit-buffer flow control for networks-on-chip. In *Proceedings of the 6th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pages 215–220, Atlanta, GA, October 2008.
Citations = 28. Acceptance Rate = 44/143 = 30.8%.

[C38] N. Bliss, K. Asanovic, K. Bergman, L. Carloni, J. Kepner, and V. Stojanovic. Photonic many-core architecture study. In *Proceedings of the Eleventh Annual Workshop on High Performance Embedded Computing (HPEC)*, Lexington, MA, September 2008.

[C37] M. Petracca, B. G. Lee, K. Bergman, and L. P. Carloni. Design exploration of optical interconnection networks for chip multiprocessors. In *Proceedings of the 16th Annual IEEE Symposium on High-Performance Interconnects (HotI)*, pages 31–40, Stanford University, CA, August 2008.
Citations = 106. Acceptance Rate = 14/47 = 29.8%.

[C36] H. Wang, M. Petracca, A. Biberman, B. G. Lee, L. P. Carloni, and K. Bergman. Nanophotonic optical interconnection network architecture for on-chip and off-chip communications. In *Proceedings of the Optical Fiber Communication / National Fiber Optic Engineers Conference (OFC/NFOEC)*, San Diego, CA, February 2008.
Citations = 59.

[C35] L. Carloni, A. B. Kahng, S. Muddu, A. Pinto, K. Samadi, and P. Sharma. Interconnect modeling for improved system-level design optimization. In *Proceedings*

of the Asia and South Pacific Design Automation Conference (ASPDAC), pages 258–264, Los Alamitos, CA, USA, 2008.
Citations = 33. Acceptance Rate = 122/350 = 34.9%.

[C34] C.-H. Li and L. P. Carloni. Using functional independence conditions to optimize the performance of latency-insensitive systems. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 32–39, San Jose, CA, November 2007.
Acceptance Rate = 139/510 = 27.0%.

[C33] A. Pinto, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. A communication synthesis infrastructure for heterogeneous networked control systems and its application to building automation and control. In C. Kirsch and R. Wilhelm, editors, *EMSOFT'07: Proceedings of the Seventh ACM & IEEE International Conference on Embedded Software*, pages 21–29, Salzburg, Austria, October 2007.
Citations = 15. Acceptance Rate = 29/131 = 22.1%.

[C32] K. Bergman and L. P. Carloni. On-chip photonic communication for high-performance multi-core processors. In *Proceedings of the Eleventh Annual Workshop on High Performance Embedded Computing (HPEC)*, Lexington, MA, September 2007.
Best Paper Award.
Citation = 14 Acceptance Rate = 26/89 = 29.2%.

[C31] A. Shacham, B. G. Lee, A. Biberman, K. Bergman, and L. P. Carloni. Photonic NoC for DMA communications in chip multiprocessors. In *Proceedings of the 15th Annual IEEE Symposium on High-Performance Interconnects (HotI)*, pages 29–38, Stanford University, CA, August 2007.
Citations = 179.

[C30] R. Collins and L. P. Carloni. Topology-based optimization of maximal sustainable throughput in a latency-insensitive system. In *Proceedings of the Design Automation Conference (DAC)*, pages 410–416, San Diego, CA, June 2007.
Citations = 20. Acceptance Rate = 147/639 = 23.2%.

[C29] A. Shacham, K. Bergman, and L. P. Carloni. The case for low-power photonic networks-on-chip. In *Proceedings of the Design Automation Conference (DAC)*, pages 132–135, San Diego, CA, June 2007.
Citations = 105. Acceptance Rate = 147/639 = 23.2%.

[C28] C.-H. Li, R. Collins, S. Sonalkar, and L. P. Carloni. Design, implementation, and validation of a new class of interface circuits for latency-insensitive design. In *Proceedings of the Fifth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 13–22, Nice, France, June 2007.
Citations = 32. Acceptance Rate = 16/34 = 47.1%.

[C27] A. Shacham, K. Bergman, and L. P. Carloni. On the design of a photonic network-on-chip. In *Proceedings of the First International Symposium on Networks-on-Chip (NOCS)*, pages 53–64, Princeton, NJ, May 2007.
Citations = 395. Acceptance Rate = 28/102 = 27.5%.

[C26] A. Shacham, K. Bergman, and L. P. Carloni. Maximizing GFLOPS-per-Watt: High-bandwidth, low power photonic on-chip networks. In *Third Watson Conference on Interaction between Architecture, Circuits, and Compilers ($P = ac^2$)*, Yorktown Heights, NY, September 2006.
Citations = 35.

[C25] A. Benveniste, B. Caillaud, L. P. Carloni, P. Caspi, A. L. Sangiovanni-Vincentelli, and S. Tripakis. Communication by sampling in time-sensitive distributed systems. In S. L. Min and W. Yi, editors, *EMSOFT'06: Proceedings of the Sixth ACM & IEEE International Conference on Embedded Software*, pages 152–160, Seoul, Korea, October 2006.
Acceptance Rate = 31/94 = 33.0%.

[C24] A. Pinto, L. P. Carloni, R. Passerone, and A. L. Sangiovanni-Vincentelli. Interchange formats for hybrid systems: Abstract semantics. In J. P. Hespanha and A. Tiwari, editors, *Proceedings of the The 9th International Workshop on Hybrid Systems: Computation and Control (HSCC)*, volume 3927 of *Lecture Notes in Computer Science*, pages 491–506, Santa Barbara, California, March 2006.
Citations = 48. Acceptance Rate = 39/79 = 49.4%.

[C23] A. Pinto, L. P. Carloni, R. Passerone, and A. L. Sangiovanni-Vincentelli. Interchange semantics for hybrid system models. In I. Troch and F. Breitenecker, editors, *Proceedings of the 5th MATHMOD*, ARGESIM-Reports, Vienna, Austria, February 2006.

[C22] A. Bonivento, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Platform-based design of wireless sensor networks for industrial applications. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 1103–1107, Munich, Germany, February 2006.
Citations = 90. Acceptance Rate = 267/834 = 32.0%.

[C21] L. P. Carloni. The role of back-pressure in implementing latency-insensitive design. In M. Singh and J.P. Talpin, editors, *FMGALS 2005: Second International Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Architectures*, volume 146(2) of *Electronic Notes on Theoretical Computer Science*, pages 61–80, 2006.
Citations = 46.

[C20] A. Bonivento, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Rialto: A bridge between description and implementation of control algorithms for wireless sensor networks. In W. Wolf and W. Taha, editors, *Proceedings of the Fifth ACM International Conference on Embedded Software (EMSOFT)*, pages 183–186, Jersey City, NY, September 2005.
Citations = 15. Acceptance Rate = 25/88 = 28.0%.

[C19] A. Benveniste, B. Caillaud, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Tag machines. In W. Wolf and W. Taha, editors, *Proceedings of the Fifth ACM International Conference on Embedded Software (EMSOFT)*, pages 255–263, Jersey City, NY, September 2005.
Citations = 45. Acceptance Rate = 25/88 = 28.0%.

[**C18**] A. Pinto, A. L. Sangiovanni-Vincentelli, L. P. Carloni, and R. Passerone. Interchange formats for hybrid systems: Review and proposal. In M. Morari, L. Thiele, and F. Rossi, editors, *Proceedings of the 8th International Workshop on Hybrid Systems : Computation and Control (HSCC)*, volume 3414 of *Lecture Notes in Computer Science*, pages 526–541, Zurich, Switzerland, March 2005.
Citations = 39.

[**C17**] A. Benveniste, B. Caillaud, L. P. Carloni, P. Caspi, and A. L. Sangiovanni-Vincentelli. Heterogeneous reactive systems modeling: Capturing causality and the correctness of loosely time-triggered architectures (LTTA). In G. Buttazzo and S. Edwards, editors, *Proceedings of the Fourth ACM International Conference on Embedded Software (EMSOFT)*, pages 220–229, Pisa, Italy, September 2004.
Citations = 37. Acceptance Rate 31/87 = 35.6%.

[**C16**] A. Benveniste, B. Caillaud, L. P. Carloni, P. Caspi, and A. L. Sangiovanni-Vincentelli. Causality and scheduling constraints in heterogeneous reactive systems modeling. In F.S.d. Boer, M.M. Bonsangue, S. Graf, and W.P. de Roever, editors, *Proceedings of the 2nd International Symposium on Formal Methods for Components and Objects, Nov. 4-7, 2003*, volume 3188 of *Lecture Notes in Computer Science*, pages 1–16, Leiden, The Netherlands, August 2004.

[**C15**] C. Pinello, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Fault-tolerant deployment of embedded software for cost-sensitive real-time feedback-control applications. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 1164–1169, Paris, France, February 2004.
Citations = 77. Acceptance Rate = 181/780 = 23.2%.

[**C14**] A. Benveniste, L. P. Carloni, P. Caspi, and A. L. Sangiovanni-Vincentelli. Heterogeneous reactive systems modeling and correct-by-construction deployment. In R. Alur and I. Lee, editors, *Proceedings of the Third International Conference on Embedded Software (EMSOFT)*, volume 2855 of *Lecture Notes in Computer Science*, pages 35–50, Philadelphia, PA, October 2003.
Citations = 64. Acceptance Rate = 20/60 = 33.3%.

[**C13**] A. Pinto, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Efficient synthesis of networks on chip. In *Proceedings of the International Conference on Computer Design (ICCD)*, pages 146–151, San Jose, CA, October 2003.
Citations = 188. Acceptance Rate = 61/233 = 26.2%.

[**C12**] L. P. Carloni and A. L. Sangiovanni-Vincentelli. A formal modeling framework for deploying synchronous designs on distributed architectures. In *FMGALS 2003: First International Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Architectures*, pages 11–31, Pisa, Italy, September 2003.
Citations = 12.

[**C11**] L. P. Carloni and A. L. Sangiovanni-Vincentelli. Combining retiming and recycling to optimize the performance of synchronous circuits. In *Proceedings of the 16th Symposium on Integrated Circuits and System Design, SBCCI 2003*, Sao

Paulo, Brazil, September 2003.
Citations = 20.

[C10] A. Pinto, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Constraint-driven communication synthesis. In *Proceedings of the Design Automation Conference (DAC)*, pages 783–788, New Orleans, LO, June 2002.
Citations = 104. Acceptance Rate = 147/491 = 30.0%.

[C9] S. Zanella, A. Neviani, E. Zanoni, E. Charbon, P. Miliozzi, C. Guardiani, L. P. Carloni, and A. L. Sangiovanni-Vincentelli. Modeling of substrate noise injected by digital libraries. In *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 2001.
Citations = 11. Acceptance Rate = 36/93 = 38.7%.

[C8] L. P. Carloni and A. L. Sangiovanni-Vincentelli. Performance analysis and optimization of latency insensitive systems. In *Proceedings of the Design Automation Conference (DAC)*, pages 361–367, Los Angeles, CA, June 2000.
Selected as candidate best paper.
Citations = 105. Acceptance Rate = 142/390 = 36.0%.

[C7] L. P. Carloni, E. I. Goldberg, T. Villa, R. K. Brayton, and A. L. Sangiovanni-Vincentelli. Aura II: Combining negative thinking and branch-and-bound in unate covering problems. In L.M. Silveira, R. Reis, and S. Devadas, editors, *VLSI: Systems on a Chip, IFIP Tenth International Conference on Very Large Scale Integration (VLSI '99)*, volume 162 of *IFIP Conference Proceedings*, pages 346–361, Lisboa, Portugal, December 1999.

[C6] L. P. Carloni, K. L. McMillan, A. Saldanha, and A. L. Sangiovanni-Vincentelli. A methodology for "correct-by-construction" latency insensitive design. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 309–315, San Jose, CA, November 1999.
Citations = 233. Acceptance Rate = 102/318 = 32.0%.

[C5] L. P. Carloni, K. L. McMillan, and A. L. Sangiovanni-Vincentelli. Latency insensitive protocols. In N. Halbwachs and D. Peled, editors, *Proceedings of the 11th International Conference on Computer-Aided Verification*, volume 1633, pages 123–133, Trento, Italy, July 1999.
Citations = 77. Acceptance Rate = 34/107 = 31.7%.

[C4] E. I. Goldberg, L. P. Carloni, T. Villa, R. K. Brayton, and A. L. Sangiovanni-Vincentelli. Negative thinking by incremental problem solving: Application to unate covering. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 91–98, San Jose, CA, November 1997.
Citations = 15. Acceptance Rate = 29/126 = 23.0%.

[C3] L. P. Carloni, P. C. McGeer, A. Saldanha, and A. L. Sangiovanni-Vincentelli. Trace driven logic synthesis - application to power minimization. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 581–588, San Jose, CA, November 1997.
Acceptance Rate = 29/126 = 23.0%.

[**C2**] A. L. Oliveira, L. P. Carloni, T. Villa, and A. L. Sangiovanni-Vincentelli. An implicit formulation for exact BDD minimization of incompletely specified functions. In R. Reis and L. Claesen, editors, *VLSI: Integrated Systems on Silicon, IFIP Eight International Conference on Very Large Scale Integration (VLSI '97)*, pages 315–326, Gramado, Brazil, August 1997. Chapman-Hall.

[**C1**] P. Miliozzi, L. P. Carloni, E. Charbon, and A. L. Sangiovanni-Vincentelli. SUBWAVE: a methodology for modeling digital substrate noise injection in mixed-signal ICs. In *Proceedings Custom Integrated Circuits Conference (CICC)*, pages 385–388, San Diego, CA, May 1996.
Citations = 71.

- **Invited Conference Papers**

[**I14**] M. Cassel Dos Santos, T. Jia, M. Cochet, K. Swaminathan, J. Zuckerman, P. Mantovani, D. Giri, J. J. Zhang, E. J. Loscalzo, G. Tombesi, K. Tien, N. Chandramoorthy, J.-D. Wellman, D. Brooks, G.-Y. Wei, K. Shepard, L.P. Carloni, and P. Bose. A scalable methodology for agile chip development with open-source hardware components. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 1–9, November 2022.

[**I13**] M. M. Ziegler, J. Kwon, H.-Y. Liu, and L. P. Carloni. Online and offline machine learning for industrial design flow tuning. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 1–9, November 2021.

[**I12**] P. Mantovani, D. Giri, G. Di Guglielmo, L. Piccolboni, J. Zuckerman, E. G. Cota, M. Petracca, C. Pilato, and L. P. Carloni. Agile SoC development with Open ESP. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, pages 1–9, November 2020.
Citations = 70.

[**I11**] L. P. Carloni. Scalable open-source system-on-chip design. In *Proceedings of the 28th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 7–9, October 2020. "Extended abstract for invited talk".

[**I10**] D. Giri, P. Mantovani, and L. P. Carloni. Runtime reconfigurable memory hierarchy in embedded scalable platforms. In *Proceedings of the Asia and South Pacific Design Automation Conference (ASPDAC)*, pages 719–726, January 2019.

[**I9**] Y. J. Yoon, P. Mantovani, and L. P. Carloni. System-level design of networks-on-chip for heterogeneous systems-on-chip. In *Proceedings of the Eleventh International Symposium on Networks-on-Chip (NOCS)*, pages 9:1–9:6, October 2017.

[**I8**] L. P. Carloni. The case for embedded scalable platforms. In *Proceedings of the Design Automation Conference (DAC)*, pages 17:1–17:6, Austin, TX, June 2016.
Citations = 49.

[**I7**] C. Pilato, Q. Xu, P. Mantovani, G. Di Guglielmo, and L. P. Carloni. On the design of scalable and reusable accelerators for big data applications. In *ACM International Conference on Computing Frontiers*, pages 406–411, Como, Italy, May 2016.

[**I6**] P. Mantovani, G. Di Guglielmo, and L. P. Carloni. High-level synthesis of accelerators in embedded scalable platforms. In *Proceedings of the Asia and South Pacific Design Automation Conference (ASPDAC)*, pages 204–211, Macau, China, January 2016.
Citations = 30.

[**I5**] M. Casale-Rossi, A. Sangiovanni-Vincentelli, L. Carloni, B. Courtois, H. de Man, A. Domic, and J. Rabaey. PANEL: The heritage of Mead & Conway: What has remained the same, what was missed, what has changed, what lies ahead. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pages 171–175, Grenoble, France, March 2013.

[**I4**] M. Petracca, K. Bergman, and L. P. Carloni. Photonic networks-on-chip: Opportunities and challenges. In *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 2789–2792, Seatte, WA, May 2008.
Citations = 27.

[**I3**] A. L. Sangiovanni-Vincentelli, L. P. Carloni, F. De Bernardinis, and M. Sgroi. Benefits and challenges of platform-based design. In *Proceedings of the Design Automation Conference (DAC)*, pages 409–414, San Diego, CA, June 2004.
Citations = 234.

[**I2**] L. P. Carloni and A. L. Sangiovanni-Vincentelli. On-chip communication design: Roadblocks and avenues. In *Proceedings of the 1st IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pages 75–76, Newport Beach, CA, October 2003. "Extended abstract for invited talk".

[**I1**] L. P. Carloni, F. De Bernardinis, A. L. Sangiovanni-Vincentelli, and M. Sgroi. The art and science of integrated systems design. In *Proceedings of the 28th European Solid-State Circuits Conference*, pages 25–36, Florence, Italy, September 2002. Published also in *Proceedings of the 32th European Solid-State Device Research Conference.*
Citations = 53.

- **Books**

[**A1**] K. Bergman, L. P. Carloni, A. Biberman, J. Chan, and G. Hendry. *Photonic Network-on-Chip Design*, volume 68 of *Integrated Circuits and Systems*. Springer, 2014.
Citations = 137.

- **Book Chapters**

  [**B5**] M. M. Ziegler, J. Kwon, H.-Y. Liu, and L. P. Carloni. The interplay of online and offline machine learning for design flow tuning. In J. Hu H. Ren, editor, *Machine Learning Applications in Electronic Design Automation*, Industrial Information Technology Series, chapter 13. Springer, Florida, January 2023.

  [**B4**] M. M. Ziegler, H.-Y. Liu, G. Gristede, B. Owens, R. Nigaglioni, J. Kwon, and L. P. Carloni. SynTunSys: A synthesis parameter autotuning system for optimizing high-performance processors. In X. Li I. M. Elfadel, D. S. Boning, editor, *Machine Learning in VLSI Computer-Aided Design*, Industrial Information Technology Series, chapter 22. Springer, Florida, August 2019.

  [**B3**] L. P. Carloni, F. De Bernardinis, C. Pinello, A. L. Sangiovanni-Vincentelli, and M. Sgroi. Platform-based design for embedded systems. In R. Zurawski, editor, *The Embedded Systems Handbook*, Industrial Information Technology Series, chapter 22. CRC Press, Florida, August 2005.
  Citations = 77.

  [**B2**] L. P. Carloni, F. De Bernardinis, A. L. Sangiovanni-Vincentelli, and M. Sgroi. Platform-based and derivative design. In R. Zurawski, editor, *The Industrial Information Technology Handbook*, Industrial Electronics Series, chapter 93. CRC Press, Florida, November 2004.

  [**B1**] L. P. Carloni, K. L. McMillan, A. Saldanha, and A. L. Sangiovanni-Vincentelli. A methodology for "correct-by-construction" latency insensitive design. In A. Kuehlmann, editor, *The Best of ICCAD - 20 Years of Excellence in Computer-Aided Design*, chapter 12, pages 143–158. Kluwer Academic Publishers, 2003.

PATENTS

- A. Shacham, K. Bergman, and L. P. Carloni. *Systems and Methods for On-Chip Data Communication*. U.S. Patent 8,340,517 issued on December 5, 2012.
- A. Saldanha, P. McGeer, and L. Carloni. *Creation of Structured Data From Plain Text*. U.S. Patent 6,714,939 issued on March 30, 2004.

INVITED LECTURES, SEMINARS, COLLOQUIA

1. *"ESP: An Open-Source Platform for Heterogeneous Computing".* IEEE CASS Webinars hosted by the Rio Grande do Sul Chapter Virtual Seminar, January 2023

2. *"Open-Source Hardware for Heterogeneous Computing."* Invited Talk, University of Bologna, Bologna, Italy, November 2022.

3. *"Hardware/Software Co-design with High-Level Synthesis."* Talk as part of Tutorial at 59 Design Automation Conference, San Francisco, CA, July 2022.

4. *"Open-Source Hardware for Heterogeneous Computing."* Invited Talk, Politecnico di Torino, Torino, Italy, June 2022.

5. *"IBM Research AI Hardware Forum 2022."* Invited Speaker, IBM T.J. Watson Research Center, Yorktown Heights, NY, October 2022.

6. *"Open-Source Hardware for Heterogeneous Computing with ESP and RISC-V."* Conference Talk, RISC-V Spring Week 2022, Paris, France, April 2022.

7. *"Open-Source Hardware for Heterogeneous Computing."* Invited Talk, Workshop on Data-Driven Applications for Industrial and Societal Challenges, Conference on Design, Automation, and Test in Europe (DATE), Virtual Workshop, March 2022.

8. *"The Open-Source ESP Platform and Its Application to Accelerating Embedded Machine Learning."* Invited Talk, Global Foundries, Virtual Seminar, February 2022.

9. *"ESP: an Open-Source Platform for Collaborative Design of Heterogeneous Systems."* Invited Talk, Workshop on Modeling & Simulation of Systems and Applications (ModSim), Virtual Conference, October 2021.

10. *"System-Level Design of Machine Learning Accelerators with the Open-Source ESP Platform."* Invited Talk, MLSyS Workshop on Benchmarking Machine Learning Workloads on Emerging Hardware, Virtual Conference, February 2021.

11. *"ESP: An Open-Source Platform for Heterogeneous Computing."* HSC Seminar, University of California at Santa Cruz, Virtual Seminar, February 2021.

12. *"Scalable Open-Source System-on-Chip Design."* Invited Talk, VLSI-SoC (International Conference on Very Large Scale Integration), Virtual Conference, October 2020.

13. *"ESP: An Open-Source Platform for Heterogeneous Computing."* Invited Talk, Qualcomm, Virtual Seminar, September 2020.

14. *"ESP: An Open-Source Platform for Heterogeneous Computing."* Virtual Computer Architecture Seminar, University of Wisconsin-Madison, Virtual Seminar, September 2020.

15. *"Accelerating Embedded Machine Learning with the Open-Source ESP Infrastructure."* Invited Talk, MLSyS'20 Workshop on Software-Hardware Co-design for Machine Learning, Austin, TX, March 2020.

16. *"Open ESP - The Heterogeneous Open-Source Platform for Developing RISC-V Systems."* Conference Talk, FOSDEM'20, Brussels, Belgium, February 2020.

17. *"ESP: An Open-Source Platform for Heterogeneous Computing."* Invited Talk, Interuniversity Microelectronics Centre (IMEC), Leuven, Belgium, January 2020.

18. *"ESP: The Open-Source SoC Platform."* Invited Talk as part of Tutorial at VLSID Conference, Bangalore, India, January 2020.

19. *"Prototyping RISC-V Based Heterogeneous Systems-on-Chip with the ESP Open-Source Platform."* Invited Talk, RISC-V Summit, San Jose, CA, December 2019.

20. *"ESP: An Open-Source Platform for Heterogeneous Computing."* Invited Talk, ETH Zurich, Zurich, Switzerland, October 2019.

21. *"ESP: An Open-Source Platform for Heterogeneous Computing."* Invited Talk, University of Modena, Modena, Italy, November 2019.

22. *"Embedded Scalable Platforms for Heterogeneous Computing."* Keynote Talk, Cyber-Physical Systems Summer School, Alghero, Italy, September 2019.

23. *"Teaching Heterogeneous Computing with System-Level Design Methods."* Paper presentation, Workshop on Computer Architecture Education (WCAE), Newton, MA, June 2019.

24. *"Embedded Scalable Platforms for Heterogeneous Computing."* Invited Talk, MathWorks Research Summit, Newton, MA, June 2019.

25. *"Embedded Scalable Platforms for Heterogeneous Computing."* Invited Talk, Harvard University, Cambridge, MA, April 2019.

26. *"Embedded Scalable Platforms for Heterogeneous Computing."* Invited talk (online), ATC (Advanced Technology Center) Project Webinar Series, Webinar, April 2019.

27. *"How High-Level Synthesis Enables Design for Reusability of Hardware Accelerators."* Invited Talk, "Quo vadis, Logic Synthesis?" Workshop, Conference on Design, Automation, and Test in Europe (DATE), Florence, Italy, March 2019.

28. *"Dynamic Information Flow Tracking on Heterogeneous Systems-on-Chip."* Invited Talk, DARPA SSITH PI Meeting, Menlo Park, CA, January 2019.

29. *"Runtime Reconfigurable Memory Hierarchy in Embedded Scalable Platforms."* Invited Talk, 24th Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2019.

30. *"Embedded Scalable Platforms for Domain-Specific System-on-Chip Design."* Invited Talk, Politecnico di Milano, Milano, Italy, December 2018.

31. *"How System-Level Design Can Benefit the Progress of Open-Source Hardware."* Invited Talk, Fourth Open Source Supercomputing (OpenSuCo) Workshop at Supercomputing Conference, Dallas, TX, November 2018.

32. *"DECADES: Deeply-Customized Accelerator-Oriented Data Supply Systems Synthesis."* Invited Talk, DARPA Electronics Resurgence Initiative (ERI) Inaugural Summit, San Jose, CA, July 2018.

33. *"Embedded Scalable Platforms for Design and Programming of Heterogeneous Systems-on-Chip."* Lightning Talk for Accelerated Compute Research Summit, Google Inc., Mountain View, CA, June 2018.

34. *"Embedded Scalable Platforms for Domain-Specific System-on-Chip Design."* Invited Talk, IBM T.J. Watson Research Center, Yorktown Heights, NY, May 2018.

35. *"Contribution to Panel on: Networks-on-Chip: Past, Present and Future."* Invited Talk at ACM/IEEE International Symposium on Networks-on-Chip (NOCS), Seoul, South Korea, October 2017.

36. *"Designing Multi-Bank Memories for Heterogeneous Architectures."* Invited Talk as part of Tutorial at Embedded Systems Week (ESWEEK), Seoul, South Korea, October 2017.

37. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, NVIDIA Corporation, Santa Clara, CA, August 2017.

38. *"Scalable Platforms and High-Level Synthesis for System-on-Chip Design."* Invited Talk, IBM T.J. Watson Research Center, Yorktown Heights, NY, July 2017.

39. *"Scalable Architectures for Specialization and Reuse in Heterogeneous System-on-Chip Design."* Invited Talk, DARPA MTO - Electronics Resurgence Initiative (ERI) Workshop, San Jose, CA, July 2017.

40. *"Scalable Platforms and High-Level Synthesis for System-on-Chip Design."* Invited Talk, MaxLinear, Irvine, CA, April 2017.

41. *"Scalable and Flexible Design Methodologies for Heterogeneous Systems-on-Chip."* Invited Talk, DARPA PERFECT Intelligent Design of Electronic Assets (IDEA) Workshop, Arlington, VA, April 2017.

42. *"Scalable Platforms for System-on-Chip Design."* Invited Talk, Faculty of Informatics - Univ. della Svizzera Italiana, Lugano, Switzerland, March 2017.

43. *"Contributions to Answer the Question: How to Deliver Sustained Scalability via Innovation Beyond the End of Moore's Law?"* Invited Talk, Computing Beyond 2025 Workshop, Center for Future Architectures Research (C-FAR), University of Michigan at Ann Arbor, MI, December 2016.

44. *"System-Level Design and High-Level Synthesis for Embedded Scalable Platforms."* Invited Talk, CDNLive - Cadence User Conference in Boston, Boston, MA, September 2016.

45. *"Embedded Scalable Platforms."* Invited Talk, DARPA PERFECT Meeting, Arlington, VA, July 2016.

46. *"The Case for Embedded Scalable Platforms."* Invited Talk, Design Automation Conference (DAC), Austin, TX, June 2016.

47. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, Silicon Labs, Austin, TX, June 2016.

48. *"Contributions to Panel on: Productive and Cost-Effective Design for Future Heterogeneous Systems"* Invited Talk, Center for Future Architectures Research (C-FAR), University of Michigan at Ann Arbor, MI, May 2016.

49. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, Qualcomm, San Diego, CA, April 2016.

50. *"System-Level Design and High-Level Synthesis for Embedded Scalable Platforms."* Invited Talk, CDNLive - Cadence User Conference in Silicon Valley, San Jose, CA, April 2016.

51. *"Embedded Scalable Platforms."* Invited Talk, DARPA PERFECT Meeting at UC Berkeley, Berkeley, CA, January 2016.

52. *"High-Level Synthesis of Accelerators in Embedded Scalable Platforms."* Invited Talk, 21st Asia and South Pacific Design Automation Conference (ASP-DAC), Macau, China, January 2016.

53. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* SWARMLab Seminar Series, UC Berkeley, Berkeley, CA, January 2016.

54. *"System-Level Design of Heterogeneous System-on-Chip Architectures."* Invited Talk, 28th Symposium on Integrated Circuits and Systems Design (SBCCI) and Chip in Bahia, Salvador, Brazil, September 2015.

55. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, Google Inc., Mountain View, CA, June 2015.

56. *"A Scalable Methodology for Embedded Scalable Platforms."* Invited Talk, Suite for Embedded Applications and Kernels (SEAK) Workshop, San Francisco, CA, June 2015.

57. *"Prototyping Heterogeneous System-on-Chip Architectures: A System-Level Design Approach."* Talk, Workshop on Architectural Research Prototyping (WARP), Portland, OR, June 2015.

58. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, Politecnico di Torino, Torino, Italy, May 2015.

59. *"Embedded Scalable Platforms."* Invited Talk, DARPA PERFECT Meeting at IBM Austin, Austin, TX, January 2015.

60. *"Embedded Scalable Platforms."* Invited Talk, DARPA PERFECT Meeting, Arlington, VA, June 2014.

61. *"Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, University of Bologna, Bologna, Italy, April 2014.

62. *"Scalable and Compositional Design of Heterogeneous Systems-on-Chip."* Invited Talk, IBM T.J. Watson Research Center, Yorktown Heights, NY, January 2014.

63. *"Embedded Scalable Platforms."* Invited Talk, DARPA PERFECT Meeting at UC Berkeley, Berkeley, CA, January 2014.

64. *"Heterogeneous System-on-Chip: The Emerging Platform for Embedded Systems."* Invited Talk, Instituto Tecnologico de Aeronautica, Sao Jose dos Campos, Brazil, November 2013.

65. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, Universidade Estadual de Campinas, Campinas, Brazil, November 2013.

66. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Invited Talk, Intel Labs, Hillsboro, OR, August 2013.

67. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* Seminar Series of Department of Electronics and Information, Politecnico di Milano, Milano, Italy, June 2013.

68. *"Scalable Design of Heterogeneous System-on-Chip Platforms."* INESC-ID / IST Seminar, Technical University of Lisbon, Lisbon, Portugal, June 2013.

69. *"Embedded Scalable Platforms."* Invited Talk, DARPA PERFECT Meeting, Arlington, VA, June 2013.

70. *"Towards Scalable Synthesis for System-on-Chip Platforms."* Online Seminar, STARnet C-FAR e-Workshop Series, April 2013.

71. *"The Heritage of Mead & Conway."* Contribution as Invited Panelist, Conference on Design, Automation, and Test in Europe (DATE), Grenoble, France, March 2013.

72. *"From Latency-Insensitive to Communication-Based Design."* Invited Talk in Tutorial "A Design Automation of Electronic Systems: Past Accomplishments and Challenges Ahead – A Tribute to Robert Brayton" Conference on Design, Automation, and Test in Europe (DATE), Grenoble, France, March 2013.

73. *"Embedded Scalable Platforms."* Invited Talk, DARPA PERFECT Kickoff Meeting, Arlington, VA, January 2013.

74. *"The Empire Strikes Back or Attack of the Clones? The Once and Future CAD"* Contribution as Invited Panelist, International Conference on Computer-Aided Design (ICCAD), San Jose, CA, November 2012.

75. *"Communication-Based System-Level Design."* Invited Talk, Gigascale Systems Research Center (GSRC) Annual Review, UC Berkeley, Berkeley, CA, October 2012.

76. *"Platform-Based Design of Distributed Embedded Systems."* Invited Talk, Philips Research North America Briarcliff, NY, July 2012.

77. *"Chip-Scale Silicon Photonics Networks for Emerging Computing Platforms."* Invited Talk, D43D Workshop, Lausanne, Switzerland, June 2012.

78. *"Design Technologies for Photonic Interconnects: Needs and Challenges."* Invited Talk, Workshop on More than Moore Technologies, Design Automation Conference, San Francisco, CA, June 2012.

79. *"System-Level Design Methods for Heterogeneous SoC Platforms."* Seminar Series of Department of Informatics, University of Verona, Verona, Italy, March 2012.

80. *"System-Level Design Methods for Heterogeneous SoC Platforms."* IBM Computer Architecture Seminar, IBM T.J. Watson Research Center, Yorktown Heights, NY, February 2012.

81. *"Design Technologies for Emerging Computing Platforms."* Invited Talk, NSF Workshop on Emerging Technologies for Interconnect, Washington DC, February 2012.

82. *"System-Level Design Methods for System-on-Chip Platforms."* ECE Colloquium, Boston University, Boston, MA, January 2012.

83. *"System-Level Design Methods for System-on-Chip Platforms."* Invited Talk, Qualcomm New Jersey Research Center, Bridgewater, NJ, December 2011.

84. *"Supervised Design Space Exploration for Systems-on-Chip."* Invited Talk, Gigascale Systems Research Center (GSRC) Annual Review, UC Berkeley, Berkeley, CA, November 2011.

85. *"Communication-Based Design and Design Reuse for Multi-Core SoC Platforms."* Invited Talk, Intel Labs, Hillsboro, OR, November 2011.

86. *"Communication-Based Design and Design Reuse for Multi-Core Systems-on-Chip."* Invited Talk, Politecnico di Torino, Torino, Italy, May 2015.

87. *"The Role of Communication in System-on-Chip Design."* Invited Talk, Conference on Design, Automation and Test in Europe, Grenoble, France, March 2011.

88. *"Emerging Silicon-Photonics Technologies for Multi-Core Platform Architectures."* Keynote Address, HiPEAC Workshop on Interconnection Network Architecture: On-Chip, Multi-Chip (INA-OCMC), Crete, Greece, January 2011.

89. *"Emerging Silicon-Photonics Technologies for Network-on-Chip Design."* Keynote Address, Design Automation Conference Workshop on Diagnostic Services in Network-on-Chips, Anaheim, CA, June 2010.

90. *"Communication-Based Design of Flexible System-on-Chip Platforms."* Invited Talk, Xilinx Inc., San Jose, CA, June 2010.

91. *"Emerging Silicon-Photonics Technologies for High-Performance Computing Systems."* Invited Talk, International Supercomputing Conference, Hamburg, Germany, June 2010.

92. *"System-Level Design of Embedded Platform Architectures."* Invited Seminar, School of Engineering, Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, Switzerland, May 2010.

93. *"System-Level Design of Embedded Platform Architectures."* Invited Seminar, Center for Silicon System Implementation Seminar Series, Carnegie Mellon University, Pittsburgh, PA, April 2010.

94. *"System-Level Design of Embedded Platform Architectures."* Invited Seminar, Joint Computer Architecture / Integrated Circuits and Systems Seminar Series, University of Texas at Austin, Austin, TX, February 2010.

95. *"System-Level Design of Embedded Platform Architectures."* Invited Seminar, School of Electrical and Computer Engineering, Georgia Tech, Atlanta, GA, February 2010.

96. *"Theme Overview: Platform Architectures."* Joint talk with M. Martonosi (Princeton Univ.), Gigascale Systems Research Center (GSRC) Workshop, Princeton University, November 2009.

97. *"System-Level Design of Embedded Platform Architectures."* Invited Seminar, Penn Cyber-Physical Systems Seminar, U. of Pennsylvania, Philadelphia, PA, October 2009.

98. *"Communication-Based Design: A Three-Year Retrospective."* GSRC Annual Symposium, San Jose, CA, September 2009.

99. *"Future of Architecture: Programmable System Architectures."* Joint talk with M. Martonosi (Princeton Univ.), Gigascale Systems Research Center (GSRC) Workshop, Dallas, TX, March 2009.

100. *"On-Chip Communication and System-Level Design Exploration."* Invited Talk, Computer Systems Laboratories, Cornell University, NY, February 2009.

101. *"On-Chip Communication and System-Level Design Exploration."* Invited Talk, NEC Laboratories America, NEC, Princeton, NJ, December 2008.

102. *"Communication Synthesis and System-Level Design Exploration."* Invited Talk at "Workshop on the Foundations and Applications of Component-Based Design", Embedded Systems Week (ESWEEK), Atlanta, GA, October 2008.

103. *"Computation vs. Communication Tradeoffs in the Design of Distributed Embedded Systems."* Invited Talk. United Technologies Research Center, Hartford, CT, September 2008.

104. *"Bridging the Gap between System-Level Design and Physical Implementation with Communication-Based Design."* Invited Talk at "4th Integrated Design System Workshop - Open Access: A Platform for Continuous Evolution and Innovation", 45^{th} Design Automation Conference (DAC), Anaheim, CA, May 2008.

105. *"Communication-Based System-Level Design."* Invited Talk at "Austin Conference on Integrated Systems & Circuits", Austin, TX, May 2007.

106. *"Towards Compositional Design for Distributed Embedded Systems."* Invited Talk. United Technologies Research Center, Hartford, CT, October 2006.

107. *"Formal Verification of Hybrid Systems."* Lecture at the tutorial on "Tools for Hybrid Embedded Systems: Modeling, Verification, and Design" at the 43rd Design Automation Conference (DAC), San Francisco, CA, July 2006.

108. *"Communication-Based Design and Latency-Insensitive Protocols."* Invited Talk, STMicroelectronics, Grenoble, France, July 2006.

109. *"Towards Compositional Design for Distributed Embedded Systems."* Invited Talk, Workshop on "Long Term Challenges in High Confidence Composable (Evolutionary) Embedded Systems" held under the auspices of NSF, the EU IST Program, and TEKES, the Science and Technology Agency of Finland, Helsinki, Finland, June 2006.

110. *"Correct-by-Construction Methodologies for Robust Electronic System-Level Design."* Invited Lecture, International Symposium on VLSI Design, Automation, and Test (VLSI), Hsinchu, Taiwan, April 2006.

111. *"Correct-by-Construction Methodologies for Robust Electronic System-Level Design."* Invited Lecture, Institut National de Recherche en Informatique et en Automatique (INRIA), Sophie-Antipolis, France, March 2006.

112. *"Latency-Insensitive Design - A Correct-by-Construction Methodology for Distributed Systems-on-Chip."* Invited Seminar, Department of Electrical Engineering, Princeton University, PA, April 2005.

113. *"Correct-by-Construction Design Methods for Heterogeneous Distributed Systems."* CSE Department Colloquium, Department of Computer Science & Engineering, University of Washington, April 2004.

114. *"Correct-by-Construction Design Methods for Heterogeneous Distributed Systems."* Invited Seminar, Department of Electrical Engineering, UCLA, April 2004.

115. *"Correct-by-Construction Design Methods for Heterogeneous Distributed Systems."* Invited Seminar, Department of Computer Science, Columbia University, March 2004.

116. *"Correct-by-Construction Design Methods for Heterogeneous Distributed Systems."* Invited Seminar, Department of Computer Science and Engineering, University of California at San Diego, February 2004.

117. *"Latency-Insensitive Design: A Correct-by-Construction Methodology for Designing Systems-on-Chip with Nanometer Technologies."* Invited Seminar, Baskin School of Engineering, University of California, Santa Cruz, February 2004.

118. *"Latency-Insensitive Design."* Invited Talk, Strategic CAD Laboratories, Intel Corporation, Hillsboro, OR, January 2004.

119. *"On-Chip Communication Design: Roadblocks and Avenues."* Invited talk for special session of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, Newport Beach, CA, October 2003.

TEACHING

- *CSEE E6868. Embedded Scalable Platforms*, Columbia University, Spring 2017-23
- *CSEE W4868. System-on-Chip Platforms*, Columbia University, Fall 2016-23.
- *COMS E6998. Topics in Computer Science: Embedded Scalable Platforms*, Columbia University, Spring 2015-16
- *CSEE E6868. System-on-Chip Platforms*, Columbia University, Spring 2013 and Fall 2014-15.
- *COMS E6998. Topics in Computer Science: System-on-Chip Design*, Columbia University, Spring 2011-12.
- *CSEE 4824. Computer Architecture*, Columbia University, Fall 2004-12 and Summer 2017-19.
- *CSEE 6847. Distributed Embedded Systems*, Columbia University, Spring 2006-09.
- *CSEE 6988-03. Distributed Concurrent Systems*, Columbia University, Spring 2005.

PROFESSIONAL ACTIVITIES

- **Journal Editorial Board Memberships**

- Associate Editor, *IEEE Transactions on Computers* 2022 - onwards
- Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2014 - onwards
- Associate Editor, *ACM Trans. on Embedded Computing Systems* 2006 - 2013, 2020 - onwards
- Associate Editor, *Sustainable Computing: Informatics and Systems* 2010 - 2013
- Associate Editor, *IEEE Transactions on Industrial Informatics* 2008 - 2010

- **Journal Special Issues**
  - Editor, *Special Issue on Compiler Frameworks and Co-design Methodologies for Heterogeneous Systems-on-Chip* of the journal *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 2022

- **Conference Chairmanships**
  - General Chair, *Embedded Systems Week (ESWEEK)*, Montreal, Canada 2013
  - General Vice Chair, *Embedded Systems Week (ESWEEK)*, Tampere, Finland 2012

- **Conference Program Committee Chairmanships**
  - "Embedded Systems for Machine Learning" Topic Committee Chair, *Conference on Design, Automation, and Test in Europe (DATE)*, Grenoble, France 2020-22
  - "System-on-Chip and HW/SW Codesign" Topic Committee Chair, *Design Automation Conference (DAC)*, Las Vegas, California 2019
  - "System-on-Chip and HW/SW Codesign" Topic Committee Chair, *Design Automation Conference (DAC)*, Austin, Texas 2018
  - "Network on Chip" Topic Committee Chair, *Conference on Design, Automation, and Test in Europe (DATE)*, Dresden, Germany 2018
  - "System-on-chip and HW/SW Codesign" Topic Committee Chair, *Design Automation Conference (DAC)*, Austin, Texas 2017
  - "Network on Chip" Topic Committee Chair, *Conference on Design, Automation, and Test in Europe (DATE)*, Dresden, Germany 2017
  - "System-on-chip and HW/SW Codesign" Topic Committee Chair, *Design Automation Conference (DAC)*, Austin, Texas 2016
  - "Network on Chip" Topic Committee Co-Chair, *Conference on Design, Automation, and Test in Europe (DATE)*, Dresden, Germany 2016

- Program Committee Co-Chair, *The 10th ACM-IEEE International Conference on Formal Methods and Models on for Codesign (MEMOCODE)*, Arlington, VA 2012
- Program Committee Co-Chair, *The 10th ACM International Conference on Embedded Software (EMSOFT)*, Scottsdale, Arizona 2010
- Program Committee Co-Chair, *The 4th ACM/IEEE International Symposium on Networks-on-Chips (NoCS)*, Grenoble, France 2010
- Program Committee Co-Chair, *The 8th ACM-IEEE International Conference on Formal Methods and Models on for Codesign (MEMOCODE)*, Grenoble, France 2010
- Program Committee Co-Chair, *The IEEE Symposium on Industrial Embedded Systems (SIES)*, Lausanne, Switzerland 2009

- **Conference Organization**
  - Organizer of the "First Workshop on Open-Source Computer Architecture Research (OSCAR)", as part of the *International Symposium on Computer Architecture (ISCA)*, New York, Ny 2022
  - Organizer and moderator of the tutorial on "ESP: the Open-Source Research Platform for Agile SoC Design and Programming" *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS))* Virtual Conference 2021
  - Organizer and moderator of the tutorial on "ESP: an Open-Source Platform for Agile SoC Development" *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)* Virtual Conference 2021
  - Organizer and moderator of the tutorial on "ESP: an Open-Source Platform for Agile SoC Development" *IEEE/ACM International Symposium on Microarchitecture (MICRO)* Virtual Conference 2020
  - Organizer and moderator of the tutorial on "ESP: An Open-Source Platform for Interdisciplinary Research on SoC Design and Programming" *ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS))* Virtual Conference 2020
  - Organizer and moderator of the tutorial on "Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms" *Embedded Systems Week (ESWEEK)*, New York, NY 2019
  - Co-Organizer and Co-Chair of the Workshop on "Accelerating Artificial Intelligence for Embedded Autonomy (AAIEA)" at the *Embedded Systems Week (ESWEEK)*, New York, NY 2019

- Co-Organizer and Co-Chair of the Workshop "Quo vadis, Logic Synthesis?" *Conference on Design, Automation, and Test in Europe (DATE)* Florence, Italy 2019
- Organizer and Chair of the Special Session "Radios for the Next 50 Billion Devices" *Design Automation Conference (DAC)*, Austin, TX 2017
- Special Session and Tutorial Chair *The 33rd IEEE International Conference on Computer Design (ICCD)*, New York, NY 2015
- Member of Steering Committee *Embedded Systems Week (ESWEEK)*, New Delhi, India 2014
- Member of Steering Committee *Embedded Systems Week (ESWEEK)*, Montreal, Canada 2013
- Publications Chair, *ACM/IEEE International Symposium on Networks-on-Chips (NoCS)*, Pittsburgh, PA 2011
- Local Arrangements Co-Chair, *The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, New York, NY 2009
- Local Arrangement Co-Chair, *IEEE Symposium on High-Performance Interconnects (HotI)*, New York, NY 2009
- Tutorial Chair, *Embedded Systems Week (ESWEEK)*, Grenoble, France 2009
- Publications Chair, *ACM/IEEE International Symposium on Networks-on-Chips (NoCS)*, San Diego, CA 2009
- Tutorial Chair, *Embedded Systems Week (ESWEEK)*, Atlanta, GA 2008
- Panel Moderator, *Industry Forum on Optical Interconnects at the 16th IEEE Symposium on High-Performance Interconnects*, Stanford, CA 2008
- Panel Organizer and Chair, *Sixth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Anaheim, CA 2008
- Publications Chair, *ACM/IEEE International Symposium on Networks-on-Chips (NoCS)*, Newcastle University, UK 2008
- Local Arrangements Chair, *First ACM/IEEE International Symposium on Networks-on-Chips (NoCS)*, Princeton, PA 2007
- Industrial Liaison Chair, *ACM Conference on Embedded Software (EMSOFT)*, Seoul, South Korea 2006
- Organizer and moderator of the tutorial on "Tools for Hybrid Embedded Systems: Modeling, Verification, and Design", *43rd Design Automation Conference*, San Francisco, CA 2006

- **Program Committee Memberships**
  - Conference on Design, Automation, and Test in Europe (DATE) 2005-2018, 2020-22

- Design Automation Conference (DAC) 2008-2010, 2016-2019
- ACM/IEEE International Symposium on Networks-on-Chip (NOCS) 2007-2022
- IEEE/ACM Intl. Symposium on Low Power Electronics and Design (ISLPED) 2017-2019
- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) 2017-2023
- IEEE High Performance Extreme Computing (HPEC) 2018-2021
- International Conference on Computer-Aided Design (ICCAD) 2006-2009, 2018, 2021
- ACM International Conference on Computing Frontiers (CF) 2016-2017
- IEEE Symposium on High-Performance Interconnects (HotI) 2009-2010, 2013-2016
- International Parallel & Distributed Processing Symposium (IPDPS) 2015-2016
- ACM Conference on Embedded Software (EMSOFT) 2005-2007, 2009-2011, 2014
- ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) 2008-2012, 2014
- IEEE International Green Computing Conference (IGCC) 2010, 2013
- International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD) 2012
- IEEE Optical Interconnects Conference (OI) 2012
- International Conference on Cyber-Physical Systems (ICCPS) 2011-2012
- IEEE Symposium on Industrial Embedded Systems (SIES) 2009, 2011-2012
- Workshop on the Interaction between Nanophotonic Devices and Systems 2011
- Conference on Hybrid Systems Computation and Control (HSCC) 2009
- Workshop on Synchronous Languages, Applications, and Programming 2006
- IEEE International Conference on Computer Design (ICCD) 2005

- **Journal Reviewer**
  - ACM Computing Surveys
  - ACM Journal of Emerging Technologies in Computing Systems
  - ACM Transactions on Architecture and Code Optimization
  - ACM Transactions on Design Automation of Electronic Systems
  - ACM Transactions on Embedded Computing Systems
  - Foundations and Trends in Electronic Design Automation
  - IEEE Computer Architecture Letters

  - IEEE Micro
  - IEEE Signal Processing Magazine
  - IEEE Transactions on CAD of Integrated Circuits and Systems
  - IEEE Transactions on Computers
  - IEEE Transactions on Industrial Informatics
  - IEEE Transactions on Parallel and Distributed Systems
  - IEEE Transactions on Very Large Scale Integration Systems
  - IET Computers & Digital Techniques
  - International Journal of Control
  - International Journal on Formal Methods in System Design
  - Journal of VLSI Signal Processing Systems

- **Conference Reviewer**

  - Conference on Design, Automation, and Test in Europe (DATE)
  - Design Automation Conference (DAC)
  - IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
  - IEEE International Conference on Computer Design (ICCD)
  - International Conference on Embedded Software (EMSOFT)
  - International Conference on VLSI Design
  - IEEE Symposium on High-Performance Interconnects (HotI)
  - Asia and South Pacific Design Automation Conference (ASPDAC)
  - International Symposium on Computer Architecture (ISCA)
  - IEEE/ACM International Symposium on Microarchitecture (MICRO)
  - International Symposium on High-Performance Computer Architecture (HPCA)
  - International Workshop on Logic Synthesis (IWLS)

- **Proposal Reviewer**

  - Reviewer, National Science Foundation.
  - Reviewer, United Kingdom Engineering and Physical Sciences Research Council.

- **Government Workshops**

  - Invited speaker at panel on *Design of Robust Cyber-Physical Systems*, as part of the kickoff meeting of DyNARUM (Dynamic Network Analysis for Robust Uncertainty Management), a DARPA project, Pasadena, CA, January 2007.

- Participant, workshop on *On- and Off-Chip Interconnection Networks for Multicore Systems* supported by NSF and the Industry-University Cooperative Research Program of the UC Discovery Grant, Stanford, CA, December 2006.
- Participant, NSF-IST-TEKES workshop on *Long Term Challenges in High Confidence Composable Embedded Systems*, Helsinki, Finland, June 2006.

- **Member of Professional Organizations**
  - ACM Senior Member (Special Interest Group on Design Automation, Special Interest Group on Embedded Systems)
  - IEEE Fellow (Circuits and Systems Society, Computer Society)