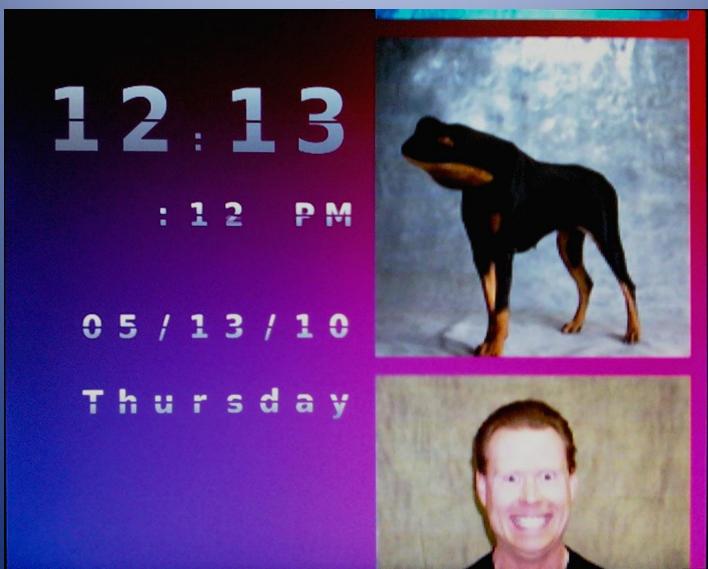
Digital Photo Frame and Clock

Embedded System Design Spring 2010 Alex Bell, Ridwan Sami, Geoff Young

Overview of Project

- Combination of digital photo frame and clock
- Bitmap images are saved on SDRAM
- The NIOS processor does timekeeping and image selection
- Hardware composites images and time onto VGA monitor

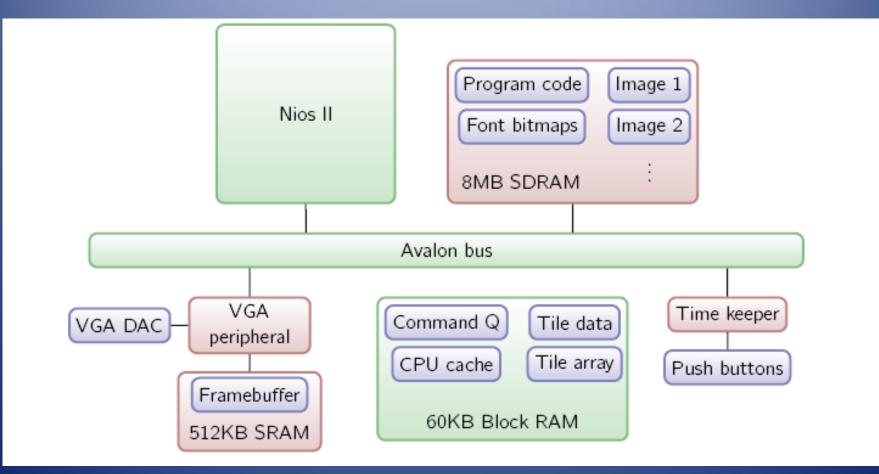
Layout



Objectives

- Displaying images in random order scrolling on screen
- Displaying time and date textually
- Letters and numbers should change by flipping animation
- Each frame should pixel-perfect (no tearing and no visual artifacts)
- Additional graphical effects (shading)

Hardware: Overview



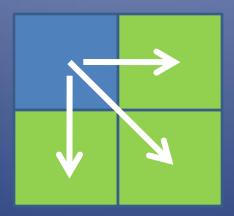
VGA Controller

SRAM directly integrated into VGA controller 16-bit R5G6B5 pixel format

- 1. 160 × 1024 pixels frame buffer stored SRAM
- 2. Processor commands queued before execution to arbitrate RAM access
- 3. VGA peripheral reads SRAM when painting right half of screen
- 4. Queue is emptied and data written to SRAM/block RAM when painting left side and not painting tiles

SRAM

- 256 × 1024 buffer of 16-bit pixels
- 160 × 240 region of buffer is visible at any given instant
 - Pixels quadrupled when displayed to fix 320 x 480 area of screen





- Tiles bitmaps located in block RAM
 Organizational choice
- 72 tiles: 32 × 32 pixels, 4 bits alpha each

61% of 60KB block RAM used

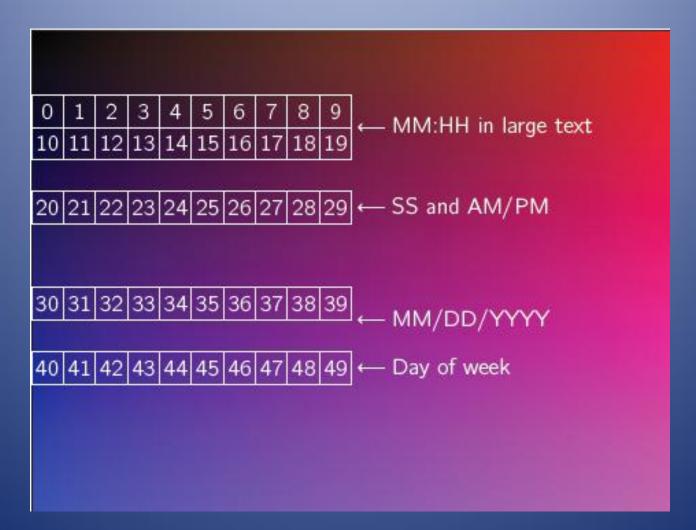
Tiles

- 40 tiles consist of 0 9 in "large format" sets of 4 tiles
- 10 tiles consists of the digits 0 9
- Remaining tiles are letters and punctuation



Example of a large format tile





Blending and the Alpha Channel

$$c_o = c_f \alpha + c_b (1 - \alpha)$$

- C_f : Current foreground value
- C_b : Current background value
- α : Alpha value ("0000" to "1111")
- 1 : Value of "1111"
- C_o: Final channel value sent to VGA DAC

Hardware: Animation States

• Flipping action modeled after gravitational acceleration



Interlacing due to poor cell phone video quality

Software

 Series of command codes are used to call hardware functions

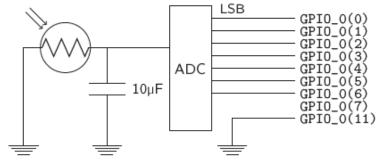
 Hardware functions fill tile display array with number pointers to current tile, pointer to animate tile, animation state and tinting of tile

Timer Module

- Counts clock cycles and interrupts NIOS every second
- Interrupts NIOS if button was pressed
- Additional timer debounces
- Supplies address with which NIOS checks reason for interrupt

Light Sensor

- Photoresistor is exposed to incident light
- Microchip coded in PBASIC acts as an A/D converter
- Microchip outputs 8-bit unsigned to DE2 board's parallel I/O part from 8 pins
- Hardware interprets data and adjusts background brightness



Timing

- SRAM VGA buffer is filled 64 rows below current level of visible pictures
- All our peripheral read/write requests operate in one cycle (no stalling)
- Block RAM requires one cycle read and two cycle write, solution entails compensated address decleration one pixel ahead
- SDRAM timing implemented automatically by SOPC builder, required 3ns clock advancement for SDRAM clock via PLL

Issues

- SDRAM requires 3ns clock advance versus main clock
- Implementation of block RAM requires explicit declaration and read write timing constraints for large read write arrays
- Occasional visual artifacts present in animation

Lessons Learned Advice for Future Students

- Focus on one area of interest rather than trying to add in every cool feature you can think of
- Reusing other peoples code is not simple and usually a great deal of additional work and may cause errors in external cause caused by integration
- SRAM data pins must be set to tri-state when done writing

Lessons Learned Continued

- All group members don't have to be present to work on the project, sometimes work can not be parallelized and one member may have to work alone
- Keep regular backups of your source code (or use a source control system) and realize that if you go over your account quota you will end up saving a blank file in the place of your code