Litigation Support Curriculum Vitae

Stephen A. Edwards, Ph.D.
Department of Computer Science, Columbia University
1214 Amsterdam Avenue, MC 0401
New York, NY 10027–7003
(212) 853–8433
sedwards@cs.columbia.edu
http://www.cs.columbia.edu/~sedwards/

Expertise

Processors	**Software**	**Compilers**	**IC Design**
Processor Architecture	Embedded Software	Assembly Optimization	Electronic Design Automation
Pipelines	Real-time Systems	Linkers and Loaders	Logic Synthesis
Historical Supercomputers	RTOSes		Place-and-route, DRC, LVS

Employment

Columbia University, New York 2006–present
Associate professor, Department of Computer Science; Tenure awarded June, 2008

Columbia University, New York 2001–2006
Assistant professor, Department of Computer Science

Synopsys, Mountain View, California 1998–2001
Senior R&D Engineer
Member of Advanced Technology (Research) Group.
Developed and implemented efficient Esterel compiler used to speed simulation in CoCentric System Studio system-level design environment. (1998-1999)

Simplex Solutions, Sunnyvale, California 1997–1998
Senior Member of Technical Staff.
Developed a hierarchical layout-versus-schematic comparison tool.

Education

University of California, Berkeley Ph.D in Electrical Engineering 1994–1997

University of California, Berkeley M.S. in Electrical Engineering. 1992–1994

California Institute of Technology B.S. with Honors, Electrical Engineering 1988–1992

Litigation Support Experience

I was retained by the **parties in bold**. These are completed cases in which my involvement has been disclosed publicly; I may have additional ongoing engagements that I am not at libery to disclose.

DLA Piper LLP 2024–
ACQIS v. **ZT Group International** 6:23-cv-00881, WDTX
Expert witness in patent dispute over computer bus communications

K&L Gates 2024–
ACQIS v. **Quanta Computer** 6:23-cv-265, WDTX
Expert witness in patent dispute over computer bus communications
Wrote invalidiy and non-infringement reports. Deposed 8/26/2025

Allen & Overy Shearman Sterling LLP 2024–
ACQIS v. **Hon Hai Precision Industry** 6:23-cv-264, WDTX
Expert witness in patent dispute over computer bus communications

K&L Gates 2024
CyboEnergy v. **Hoymiles Power Electronics** 2:23-cv-311, EDTX
Expert witness in patent dispute over solar power inverters
Wrote declaration. Parties settled.

Hogan Lovells/Willkie Farr & Gallagher 2021–2024
Synopsys v. Real Intent 5:20-cv-02819-EJD, NDC
Expert witness in contract dispute involving Electronic Design Automation (EDA) software
Wrote three expert reports. Deposed 1/10/2024, 8/28/2024. Testified 10/18/2024.

Greenberg Traurig/Erise IP 2022–2024
ACQIS v. **Asustek** 6:20-cv-00966-ADA, WDTX
Expert witness in patent dispute over computer bus communications
Wrote invalidity, non-infringement reports. Deposed 7/18/2022, 6/30/2023. Testified 3/20/2024.

Greenberg Traurig 2022
ACQIS v. **Acer** 2:21-vc-00275-JRG-RSP, EDTX
Expert witness in patent dispute over computer bus communications
Wrote invalidity report. Settled 8/2022.

Irell & Manella 2022–2023
Google v. **Valtrus Innovations** IPR2022-01406
Expert witness in patent dispute over dynamic partitioning in virtual machines
Wrote declaration for *inter partes* review. Deposed 10/17/2023.

Munck Wilson Mandala 2020–
Ceiva Opco v. Amazon.com 2:22-cv-02709-AB-MAA, CDCA
Expert witness in patent dispute over digital picture frames
Wrote infringement reports, rebuttals. Deposed 10/24/2023, 11/16/2023.

DLA Piper LLP 2021
ACQIS v. **Samsung Electronics** 2:20-cv-00295-JRG, EDTX
Expert witness in patent dispute over computer bus communications
Wrote declarations for *inter partes* review and invalidity. Deposed 10/28/2021. Settled 12/2021.

Hogan Lovells 2020–2021
Synopsys v. Avatar Integrated Systems 3:20-cv-04151-WHO, NDCA
Expert witness in EDA software patent
Wrote expert report on infringement. Deposed 6/6/2021.

ThompsonKnight 2020
US v. **Mao**
Expert witness in criminal complaint involving solid-state disk drive technology
Analyzed evidence. Defendant pleaded guilty to a lesser charge 11/2020.

The Wiesner Law Firm, P.C. 2019
Abira v. **Comtron** PAS-C-41-19, Superior Court NJ
Expert witness in a software-as-a-service case involving a medical testing database system
Deposed 7/8/2019. Testified 7/9/2019.

Durie Tangri 2019
Intel
Expert witness regarding patent on surge current reduction in integrated circuits
Wrote declaration for *inter partes* review.

Orrick, Herrington & Sutcliffe LLP 2017–2018
Synopsys v. Ubiquiti 3:17-cv-00561-WHO, NDCA
Expert witness in EDA software licensing case
Wrote expert and rebuttal reports. Deposed 10/2018. Settled 1/2019.

Aiken Gump Strauss Hauer & Feld LLP 2017
AMD v. **VIZIO** et al. ITC 337-TA-1044
Expert witness in US ITC patent dispute over graphics processors (GPUs)
Wrote invalidity report. Deposed 9/2017. Testified 11/2017. Wrote IPR declaration (IPR2018-00561).

McKool Smith 2017
IMAX v. **Three-Dimensional Media Group and UNIPAT.org**
Expert witness in arbitration matter involving image processing software for cinema
Examined code. Wrote report. Testified 7/2017.

Kirkland & Ellis 2016–2017
Future Link Systems LLC v. **Intel Corporation** 1:14-cv-00377, DDC
Expert witness in patent dispute regarding isolation circuitry around powered-off blocks
Wrote declaration for an *Inter Partes* review (IPR2016-01400). Deposed 2/17/2017. Settled 8/2017.

Jones Day 2016
Synopsys v. ATopTech 3:13-cv-02965 MMC (DMR), NDCA
Expert witness in patent dispute regarding hierarchical place and route (US 6,567,967)
Wrote infringement report. Deposed 10/2016.

Latham & Watkins LLP 2015
Samsung v. **NVIDIA** ITC 337-TA-941
Expert witness in US ITC dispute over patent on computer bus architecture (US 6,173,349)
Wrote invalidity, noninfringment reports. Deposed 6/2015; Testified 8/2015.

Paduano & Weintraub LLP 2015–2017
Stanacard v. **Rubard** 1:12-cv-05176 (CM), SDNY
Expert witness in copyright/patent dispute over software for telecom calling-card system (US 7,346,156)
Wrote expert report. Deposed 7/2015. Settled 1/2017.

Lee Tran & Liang LLP 2014
VIZIO v. Gemtek SACV13-160 JLS (RNBx), CDCA
Retained expert on software development procedures for embedded code
Wrote export report. Deposed 5/2014. Testified 9/2014.

Fish & Richardson P.C. 2014
Mobotix IPR2013-00335
Patent on video surveillance cameras
Wrote declaration for *Inter Partes* review.

Fish & Richardson P.C. 2012
Graphics Properties Holdings v. **Research in Motion** ITC 337-TA-836
Expert witness in patent dispute over processor architecture
Wrote invalidity and noninfringement reports. Deposed 11/2012. Case settled.

Arnold & Porter, LLP 2010
SJ Labs v. i2Telecom International
Reviewed Windows VoIP code for alleged copying
Case Dropped.

Baker Botts 2009–2010
Red Bend v. Google 09-cv-11813-DPW, EDMA
Expert witness in dispute over software binary differencing patent
Wrote declarations; infringement report. Deposed 2/10/2010.

Honors and Awards

ESWEEK/CASES Test-of-Time Award July 2023
For our 2008 CASES paper "Predictable Programming on a Precision Timed Architecture"
Given to one paper per year with highest impact published at a previous conference

Best paper award March 2006
Design Automation and Test in Europe
Munich, Germany (given to 2 of 800+ submissions)

Senior Member 2006
IEEE (Institute of Electrical and Electronics Engineers)
This is the main professional organization for Electrical Engineers

National Science Foundation Faculty Early Career Development ("CAREER") Award 2002
"Designing Embedded Systems with Domain-Specific Languages"
I won this award the first time I applied.

NSF Graduate Research Fellowship 1994–1996
Three years tuition & stipend, awarded annually to about 800 of 5000 applicants.

California Fellowship in Microelectronics 1992–1993
One year tuition plus stipend.

Caltech Merit Award 1990–1991, 1991–1992
One year full tuition, awarded annually to about 45 of 800 undergraduates.

Research Support

DARPA HR001125CE027: $6.5M (my share $384k) 2025–2028
Machine learning and Optimization-guided Compilers for Heterogeneous Architectures (MOCHA)
with Perspecta Labs.

DARPA HR0011-19-C-0106: $6.4M (my share $517k) 2019–2024
Secure Handling of Isolated Executables without Leaking Data (SHIELD)
with Perspecta Labs.

NIH 1RF1MH120034-01: $500k total (my share $260k) 2020–2022
Generating a Formal Set of Collaborative Standards for Sharing Behavioral Data and Task Designs to Enable Reproducibility in Neuroscience
with Adam Kepecs of Washington University.

NSF CCF-SHF 1162124: $1.2M total (my share $600k) 2012–2016
SHF:Medium:Compiling Parallel Algorithms to Memory Systems
with Martha A. Kim.

NSF CCF-SHF 1065338: $625k total (my share $208k) 2011–2014
SHF:Medium:Type-Specific Instruction Processing
with Martha A. Kim and Ken Ross.

NSF CSR-EHS 0720292: $1.2M total (my share $200k) 2007–2010
CSR–EHS:PRET: Precision Timed Architectures
with Edward A. Lee et al.

NSF CSR-EHS 0614799: $240k 2006–2008
CSR-EHS:SHIM: Developing Embedded Systems with Deterministic Concurrency

Gift from Altera, $20k 2006
Hardware Software Co-Synthesis from SHIM,

Publications

My ORCID: 0000-0003-2609-4861

Patent

US Patent 7,100,164. "Method & Apparatus for Converting a Concurrent Control Flow Graph into a Sequential Control Flow Graph." Filed January 6th, 2000, issued August 29th, 2006.

Books

[1] Dumitru Potop-Butucaru, Stephen A. Edwards, and Gérard Berry. *Compiling Esterel*. Springer, January 2007.

[2] Stephen A. Edwards. *Languages for Digital Embedded Systems*. Kluwer, Boston, Massachusetts, September 2000.

Chapters in Books

[3] Stephen A. Edwards. Further experiences teaching an FPGA-based embedded systems class. In Roger Chamberlain, Walid Taha, and Martin Törngren, editors, *Cyber Physical Systems. Model-Based Design*, number 11615 in Lecture Notes in Computer Science, pages 222–230. Springer, May 2019.

[4] Stephen A. Edwards. On determinism. In Patricia Derler, Marten Lohstroh, and Marjan Sirjani, editors, *Principles of Modeling: Essays dedicated to Edward A. Lee on the Occasion of his 60th Birthday*, volume 10760 of *Lecture Notes in Computer Science*, pages 240–253. Springer, Berkeley, California, October 2017.

[5] Stephen A. Edwards and Joseph T. Buck. System-level specification and modeling languages. In Luciano Lavagno, Igor L. Markov, Grant Martin, and Louis K. Scheffer, editors, *Electronic Design Automation for IC System Design, Verification, and Testing*, chapter 4, pages 59–74. CRC Press, December 2016.

[6] Stephen A. Edwards and Joseph T. Buck. Design and verification languages. In Luciano Lavagno, Igor L. Markov, Grant Martin, and Louis K. Scheffer, editors, *Electronic Design Automation for IC System Design, Verification, and Testing*, chapter 15, pages 373–400. CRC Press, December 2016.

[7] Stephen A. Edwards and Nalini Vasudevan. Compiling SHIM. In Sandeep K. Shukla and Jean-Pierre Talpin, editors, *Synthesis of Embedded Software: Frameworks and Methodologies for Correctness by Construction*, chapter 4, pages 121–146. Springer, January 2010.

[8] Stephen A. Edwards. Design and verification languages. In Luciano Lavagno, Grant Martin, and Lou Scheffer, editors, *Electronic Design Automation for Integrated Circuits Handbook*. CRC Press, Boca Raton, Florida, January 2006.

[9] Stephen A. Edwards. Languages for embedded systems. In Richard Zurawski, editor, *The Embedded Systems Handbook*, pages 7–1–7–19. CRC Press, Boca Raton, Florida, January 2005.

[10] Stephen A. Edwards. Languages for embedded systems. In Richard Zurawski, editor, *The Industrial Information Technology Handbook*, pages 85–1–85–18. CRC Press, Boca Raton, Florida, December 2004.

Journal Papers

All journal papers were peer-reviewed. The Proceedings of the IEEE papers were invited, as all papers in that journal are.

[11] John Hui and Stephen A. Edwards. The sparse synchronous model on real hardware. *ACM Transactions on Embedded Computing Systems*, 23(5), August 2024.

[12] Stephen A. Edwards, Richard Townsend, Martha Barker, and Martha A. Kim. Compositional dataflow circuits. *ACM Transactions on Embedded Computing Systems*, 18(1):5, February 2019.

[13] Lisa Wu, Martha A. Kim, and Stephen A. Edwards. Cache impacts of datatype acceleration. *Computer Architecture Letters*, 11(1):21–24, January 2012. Selected as one of the "Best Papers from Computer Architecture Letters" in 2011.

[14] Nalini Vasudevan and Stephen A. Edwards. Buffer sharing in rendezvous programs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 29(10):1471–1480, October 2010.

[15] Marcio Buss, Daniel Brand, Vugranam Sreedhar, and Stephen A. Edwards. A novel analysis space for pointer analysis and its application for bug finding. *Science of Computer Programming*, 75(11):921–942, November 2010.

[16] Cristian Soviani, Ilija Hadžić, and Stephen A. Edwards. Synthesis and optimization of pipelined packet processors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 28(2):231–244, February 2009.

[17] Osama Neiroukh, Stephen A. Edwards, and Xiaoyu Song. Transforming cyclic circuits into acyclic equivalents. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(10):1775–1787, October 2008.

[18] Stephen A. Edwards and Jia Zeng. Code generation in the Columbia Esterel Compiler. *EURASIP Journal on Embedded Systems*, 2007:Article ID 52651, 31 pages, February 2007.

[19] Cristian Soviani, Olivier Tardieu, and Stephen A. Edwards. Optimizing sequential cycles through Shannon decomposition and retiming. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 26(3):456–467, March 2007.

[20] Stephen A. Edwards. The challenges of synthesizing hardware from C-like languages. *IEEE Design & Test of Computers*, 23(5):375–386, September 2006.

[21] Stephen A. Edwards and Olivier Tardieu. SHIM: A deterministic model for heterogeneous embedded systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 14(8):854–867, August 2006.

[22] Stephen A. Edwards. Experiences teaching an FPGA-based embedded systems class. *ACM SIGBED Review*, 2(4):56–62, October 2005. Originally presented at the Workshop on Embedded Systems Education.

[23] Stephen A. Edwards and Edward A. Lee. The semantics and execution of a synchronous block-diagram language. *Science of Computer Programming*, 48(1):21–42, July 2003. 16 citations on Google Scholar.

[24] Stephen A. Edwards. Tutorial: Compiling concurrent languages for sequential processors. *ACM Transactions on Design Automation of Electronic Systems*, 8(2):141–187, April 2003. 19 citations on Google Scholar.

[25] Albert Benveniste, Paul Caspi, Stephen A. Edwards, Nicolas Halbwachs, Paul Le Guernic, and Robert de Simone. The synchronous languages 12 years later. *Proceedings of the IEEE*, 91(1):64–83, January 2003. Invited. 174 citations on Google Scholar.

[26] Stephen A. Edwards. An Esterel compiler for large control-dominated systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 21(2):169–183, February 2002. 37 citations on Google Scholar.

[27] Stephen Edwards, Luciano Lavagno, Edward A. Lee, and Alberto Sangiovanni-Vincentelli. Design of embedded systems: Formal models, validation, and synthesis. *Proceedings of the IEEE*, 85(3):366–390, March 1997. Invited. 272 citations on Google Scholar.

Conference Papers

All conference papers were peer-reviewed. In my area, conference papers are preferred over journals because conferences are more selective and more widely read.

[28] Matthew Edwin Weingarten, Michael Grieco, Stephen A. Edwards, and Tanvir Ahmed Khan. Icicle: Open-source hardware support for top-down microarchitectural analysis on RISC-V. In *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC)*, Irvine, California, USA, October 2025.

[29] John Hui, Kyle J. Edwards, and Stephen A. Edwards. Timestamp peripherals for precise real-time programming. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Hamburg, Germany, September 2023.

[30] Maxwell Levatich, Robert Brotzman, Benjamin Flin, Ta Chen, Rajesh Krishnan, Michael Kaplan, and Stephen A. Edwards. C program partitioning with fine-grained security constraints and post-partition verification. In *Proceedings of the IEEE Military Communications Conference (MILCOM)*, pages 285–291, Rockville, Maryland, USA, November 2022. IEEE.

[31] Robert Krook, John Hui, Bo Joel Svensson, Stephen A. Edwards, and Koen Claessen. Creating a language for writing real-time applications for the internet of things. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Shanghai, China, October 2022.

[32] Martha Barker, Stephen A. Edwards, and Martha Kim. Synthesized in-BRAM garbage collection for accelerators with immutable memory. In *Proceedings of Field Programmable Logic and Applications (FPL)*, Belfast, UK, August 2022.

[33] Stephen A. Edwards and John Hui. The sparse synchronous model. In *Forum on Specification and Design Languages (FDL)*, Kiel, Germany, September 2020. 17 / 39 = 43%.

[34] Andrea Lottarini, João P. Cerqueira, Thomas J. Repetti, Stephen A. Edwards, Kenneth A. Ross, Mingoo Seok, and Martha A. Kim. Master of none acceleration: A comparison of accelerator architectures for analytical query processing. In *Proceedings of the International Symposium on Computer Architecture (ISCA)*, pages 762–773. Association for Computing Machinery, June 2019. 62/365 = 17%.

[35] Stephen A. Edwards, Richard Townsend, and Martha A. Kim. Compositional dataflow circuits. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 175–184, Vienna, Austria, September 2017. Association for Computing Machinery. 15/48 = 31%.

[36] Andrea Lottarini, Stephen A. Edwards, Kenneth A. Ross, and Martha A. Kim. Network synthesis for database processing units. In *Proceedings of the Design Automation Conference (DAC)*, Austin, Texas, June 2017. ACM.

[37] Richard Townsend, Martha A. Kim, and Stephen A. Edwards. From functional programs to pipelined dataflow circuits. In *Proceedings of Compiler Construction (CC)*, pages 76–86, Austin, Texas, February 2017. ACM. 13/53 = 25%.

[38] Bingyi Cao, Kenneth A. Ross, Martha A. Kim, and Stephen A. Edwards. Implementing latency-insensitive dataflow blocks. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 179–187, Austin, Texas, September 2015. The Institute of Electrical and Electronics Engineers (IEEE).

[39] Kuangya Zhai, Richard Townsend, Lianne Lairmore, Martha A. Kim, and Stephen A. Edwards. Hardware synthesis from a recursive functional language. In *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pages 83–93, Amsterdam, The Netherlands, October 2015. IEEE. 540/1741 = 31%.

[40] Stephen A. Edwards and Hiren Patel. MEMOCODE 2014 software design contest: Space invaders emulator. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, page 185, Lausanne, Switzerland, October 2014. The Institute of Electrical and Electronics Engineers (IEEE). Invited.

[41] Stephen A. Edwards. MEMOCODE 2012 hardware/software codesign contest: DNA sequence aligner. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 85–90, Arlington, Virginia, July 2012.

[42] Nalini Vasudevan, Kedar Namjoshi, and Stephen A. Edwards. Simple and fast biased locks. In *Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pages 65–74, Vienna, Austria, September 2010.

[43] Stephen A. Edwards, Sungjun Kim, Edward A. Lee, Isaac Liu, Hiren D. Patel, and Martin Schoeberl. A disruptive computer design idea: Architectures with repeatable timing. In *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, Lake Tahoe, CA, October 2009.

[44] Baolin Shao, Nalini Vasudevan, and Stephen A. Edwards. Compositional deadlock detection for rendezvous communication. In *Proceedings of the International Conference on Embedded Software (Emsoft)*, pages 59–66, Grenoble, France, October 2009. 33/106 = 31%.

[45] Nalini Vasudevan and Stephen A. Edwards. Buffer sharing in CSP-like programs. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Cambridge, Massachusetts, July 2009. 15/42 = 36%.

[46] Nalini Vasudevan and Stephen A. Edwards. A determinizing compiler. In *Programming Languages Design and Implementation (PLDI) - Fun Ideas and Thoughts Session*, Dublin, Ireland, June 2009.

[47] Nalini Vasudevan, Olivier Tardieu, Julian Dolby, and Stephen A. Edwards. Compile-time analysis and specialization of clocks in concurrent programs. In *Proceedings of Compiler Construction (CC)*, volume 5501 of *Lecture Notes in Computer Science*, pages 48–62, York, United Kingdom, March 2009.

[48] Nalini Vasudevan and Stephen A. Edwards. Celling SHIM: Compiling deterministic concurrency to a heterogeneous multicore. In *Proceedings of the Symposium on Applied Computing (SAC)*, volume III, pages 1626–1631, Honolulu, Hawaii, March 2009. 1084/316 = 29%.

[49] Ben Lickly, Isaac Liu, Sungjun Kim, Hiren D. Patel, Stephen A. Edwards, and Edward A. Lee. Predictable programming on a precision timed architecture. In *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pages 137–146, Atlanta, Georgia, October 2008. **2023 CASES/ESWEEK Test-of-Time award**.

[50] Nalini Vasudevan and Stephen A. Edwards. Static deadlock detection for the SHIM concurrent language. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 49–58, Anaheim, California, June 2008.

[51] Nalini Vasudevan, Satnam Singh, and Stephen A. Edwards. A deterministic multi-way rendezvous library for Haskell. In *Proceedings of the International Parallel and Distributed Processing Symposium (IPDPS)*, pages 1–12, Miami, Florida, April 2008. 105/410 = 25%.

[52] Stephen A. Edwards, Nalini Vasudevan, and Olivier Tardieu. Programming shared memory multiprocessors with deterministic message-passing concurrency: Compiling SHIM to Pthreads. In *Proceedings of Design, Automation, and Test in Europe (DATE)*, pages 1498–1503, Munich, Germany, March 2008.

[53] Marcio Buss, Daniel Brand, Vugranam Sreedhar, and Stephen A. Edwards. Flexible pointer analysis using assign-fetch graphs. In *Proceedings of the Symposium on Applied Computing (SAC)*, pages 234–239, Fortaleza, Ceará, Brazil, March 2008. 384/1307 = 29.3%.

[54] Stephen A. Edwards and Edward A. Lee. The case for the precision timed (PRET) machine. In *Proceedings of the 44th Design Automation Conference*, pages 264–265, San Diego, California, June 2007. 8/54 = 15% ("WACI" track).

[55] Haim Cohen and Stephen A. Edwards. {sets}—a lightweight constraint programming language based on ROBDDs. In *Proceedings of the IADIS International Conference on Applied Computing*, Salamanca, Spain, February 2007.

[56] Olivier Tardieu and Stephen A. Edwards. Scheduling-independent threads and exceptions in SHIM. In *Proceedings of the International Conference on Embedded Software (Emsoft)*, pages 142–151, Seoul, Korea, October 2006. 31/94 = 33%.

[57] Olivier Tardieu and Stephen A. Edwards. R-SHIM: Deterministic concurrency with recursion and shared variables. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, page 202, Napa, California, July 2006. 17 papers + 6 posters / 43 = 53%.

[58] Nicholas Jun Hao Ip and Stephen A. Edwards. A processor extension for cycle-accurate real-time software. In *Proceedings of the IFIP International Conference on Embedded and Ubiquitous Computing (EUC)*, volume 4096 of *Lecture Notes in Computer Science*, pages 449–458, Seoul, Korea, August 2006. approx. 125/500 = 25%.

[59] Stephen A. Edwards and Olivier Tardieu. Efficient code generation from SHIM models. In *Proceedings of Languages, Compilers, and Tools for Embedded Systems (LCTES)*, pages 125–134, Ottawa, Canada, June 2006. 21/83 = 25%.

[60] Cristian Soviani, Ilija Hadžić, and Stephen A. Edwards. Synthesis of high-performance packet processing pipelines. In *Proceedings of the 43rd Design Automation Conference*, pages 679–682, San Francisco, California, July 2006. 180/865 = 20%.

[61] Cristian Soviani, Olivier Tardieu, and Stephen A. Edwards. Optimizing sequential cycles through Shannon decomposition and retiming. In *Proceedings of Design, Automation, and Test in Europe (DATE)*, pages 1085–1090, Munich, Germany, March 2006. 233/834 = 28%, **Best paper award**.

[62] Osama Neiroukh, Stephen A. Edwards, and Xiaoyu Song. An efficient algorithm for the analysis of cyclic circuits. In *Proceedings of the Symposium on VLSI (ISVLSI)*, pages 303–308, Karlsruhe, Germany, March 2006. 64/151 = 42%.

[63] Jia Zeng and Stephen A. Edwards. Separate compilation for synchronous modules. In *Proceedings of the 2nd International Conference on Embedded Software and Systems (ICESS)*, volume 3820 of *Lecture Notes in Computer Science*, pages 129–140, Xi'an, China, December 2005. 140/360 = 39% overall, 63/360 = 17% for proceedings.

[64] Olivier Tardieu and Stephen A. Edwards. Approximate reachability for dead code elimination in Esterel*. In *Proceedings of the Third International Symposium on Automated Technology for Verification and Analysis (ATVA)*, volume 3707 of *Lecture Notes in Computer Science*, pages 323–337, Taipei, Taiwan, October 2005. 33/95 = 35%.

[65] Stephen A. Edwards and Olivier Tardieu. SHIM: A deterministic model for heterogeneous embedded systems. In *Proceedings of the International Conference on Embedded Software (Emsoft)*, pages 37–44, Jersey City, New Jersey, September 2005. 25/88 = 28%, 10 citations on Google Scholar.

[66] Stephen A. Edwards and Olivier Tardieu. Deterministic receptive processes are Kahn processes. In *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, pages 37–44, Verona, Italy, July 2005. 17/47 = 36%.

[67] Christopher L. Conway, Kedar S. Namjoshi, Dennis Dams, and Stephen A. Edwards. Incremental algorithms for inter-procedural analysis of safety properties. In *Proceedings of the 17th International Conference on Computer-Aided Verification (CAV)*, volume 3576 of *Lecture Notes in Computer Science*, pages 449–461, Edinburgh, Scotland, June 2005. 32/123 = 26%.

[68] Stephen A. Edwards. The challenges of hardware synthesis from C-like languages. In *Proceedings of Design, Automation, and Test in Europe (DATE)*, pages 66–67, Munich, Germany, March 2005. 176/825 = 21%. 17 citations on Google Scholar., Invited.

[69] Jia Zeng, Cristian Soviani, and Stephen A. Edwards. Generating fast code from concurrent program dependence graphs. In *Proceedings of Languages, Compilers, and Tools for Embedded Systems (LCTES)*, pages 175–181, Washington, DC, June 2004. 28/120 = 23%.

[70] Christopher L. Conway and Stephen A. Edwards. NDL: A domain-specific language for device drivers. In *Proceedings of Languages, Compilers, and Tools for Embedded Systems (LCTES)*, pages 30–36, Washington, DC, June 2004. 28/120 = 23%.

[71] Stephen A. Edwards. Making cyclic circuits acyclic. In *Proceedings of the 40th Design Automation Conference*, pages 159–162, Anaheim, California, June 2003. 152/628 = 24%. 13 citations on Google Scholar.

[72] Stephen Jan, Paolo de Dios, and Stephen A. Edwards. Porting a network cryptographic service to the RMC2000: A case study in embedded software development. In *Designers' Forum: Design Automation and Test in Europe Conference and Exhibition*, pages 150–155, Munich, Germany, March 2003. 98 long + 54 short + 36 designer's forum/590 = 32%, Also appears as Chapter 13 of *Embedded Software for SoC*, Jerraya, Yoo, Verkest and Wehn eds., Kluwer, 2003.

[73] Sandeep Shukla, Stephen A. Edwards, Jean-Pierre Talpin, and Rajesh K. Gupta. Tutorial: High level modeling and validation methodologies for embedded systems: bridging the productivity gap. In *Proceedings of the 16th International Conference on VLSI Design*, pages 9–14, New Delhi, India, January 2003.

[74] Stephen A. Edwards, Tony Ma, and Robert Damiano. Using a hardware model checker to verify software. In *Proceedings of the 4th International Conference on ASIC (ASICON)*, pages 85–90, Shanghai, China, October 2001.

[75] Stephen A. Edwards. Compiling Esterel into sequential code. In *Proceedings of the 37th Design Automation Conference*, pages 322–327, Los Angeles, California, June 2000. Association for Computing Machinery. 154/445 = 35%, Cited by 47 in Google Scholar.

[76] Gitanjali Swamy, Stephen Edwards, and Robert Brayton. Efficient verification and synthesis using design commonalities. In *Proceedings of the Eleventh International Conference on VLSI Design (VLSI'98)*, pages 542–551, Chennai, India, January 1998.

[77] Robert K. Brayton, Gary D. Hachtel, Alberto L. Sangiovanni-Vincentelli, Fabio Somenzi, Adnan Aziz, Szu-Tsung Cheng, Stephen A. Edwards, Sunil P. Khatri, Yuji Kukimoto, Abelardo Pardo, Shaz Qadeer, Rajeev K. Ranjan, Shaker Sarwary, Thomas R. Shiple, Gitanjali Swamy, and Tiziano Villa. VIS. In *Formal Methods in Computer-Aided Design (FMCAD)*, volume 1166, pages 248–256, Palo Alto, California, November 1996.

[78] Robert K. Brayton, Gary D. Hachtel, Alberto Sangiovanni-Vincentelli, Fabio Somenzi, Adnan Aziz, Szu-Tsung Cheng, Stephen Edwards, Sunil Khatri, Yuji Kukimoto, Abelardo Pardo, Shaz Qadeer, Rajeev K. Ranjan, Shaker Sarwary, Thomas R. Shiple, Gitanjali Swamy, and Tiziano Villa. VIS: A system for verification and synthesis. In *Proceedings of the 8th International Conference on Computer-Aided Verification (CAV)*, volume 1102 of *Lecture Notes in Computer Science*, pages 428–432, New Brunswick, New Jersey, July 1996. Springer. 32/93 = 34%, 367 citations on Google Scholar.

Workshop Papers

All workshop papers were peer-reviewed. Those at IWLS have limited distribution.

[79] Marten Lohstroh, Edward A. Lee, Stephen A. Edwards, and David Broman. Logical time for reactive software. In *Workshop on Time-Centric Reactive Software (TCRS)*, pages 313—318, San Antonio, TX, USA, May 2023.

[80] John Hui and Stephen A. Edwards. Towards sparse synchronous programming in Lua. In *Workshop on Time-Centric Reactive Software (TCRS)*, pages 361—366, San Antonio, TX, USA, May 2023.

[81] Stephen A. Edwards. Further experiences teaching an FPGA-based embedded systems class. In *Proceedings of the Workshop on Embedded Systems Education (WESE)*, Turin, Italy, October 2018.

[82] Bingyi Cao, Kenneth A. Ross, Stephen A. Edwards, and Martha A. Kim. Deadlock-free joins in DB-Mesh, an asynchronous systolic array accelerator. In *Proceedings of the Workshop on Data Management on New Hardware (DaMoN)*, Chicago, Illinois, May 2017. Article No. 5.

[83] Richard Townsend, Martha A. Kim, and Stephen A. Edwards. Resource allocation for hardware implementations of map. In *Proceedings of the Workshop on Architectures and Systems for Big Data (ASBD)*, Minneapolis, Minnesota, June 2014.

[84] Stephen A. Edwards, Alain Girault, and Klaus Schneider. Synchronous Programming (Dagstuhl Seminar 13471). *Dagstuhl Reports*, 3(11):117–143, March 2014.

[85] Martha A. Kim and Stephen A. Edwards. Computation vs. memory systems: Pinning down accelerator bottlenecks. In *Proceedings of the Workshop on Architectural and Microarchitectural Support for Binary Translation (AMAS-BT)*, Saint-Malo, France, June 2010.

[86] Nalini Vasudevan and Stephen A. Edwards. Determinism should ensure deadlock-freedom. In *Proceedings of the 2nd USENIX Workshop on Hot Topics in Parallelism (HotPar)*, Berkeley, California, June 2010.

[87] Nalini Vasudevan and Stephen A. Edwards. Ensuring deterministic concurrency through compilation. In *Proceedings of the IEEE International Parallel and Distributed Processing Symposium Workshops*, Atlanta, USA, April 2010.

[88] Stephen A. Edwards. Concurrency and communication: Lessons from the SHIM project. In *Proceedings of the Workshop on Software Technologies for Future Embedded and Ubiquitious Systems (SEUS)*, volume 5860 of *Lecture Notes in Computer Science*, pages 276–287, Newport Beach, California, November 2009. Springer.

[89] Stephen A. Edwards, Sungjun Kim, Edward A. Lee, Hiren D. Patel, and Martin Schoeberl. Reconciling repeatable timing with pipelining and memory hierarchy. In *Proceedings of the Workshop on Reconciling Performance with Predictability (RePP)*, Grenoble, France, October 2009.

[90] Stephen A. Edwards and Jia Zeng. Static elaboration of recursion for concurrent software. In *Proceedings of the Workshop on Partial Evaluation and Program Manipulation (PEPM)*, pages 71–80, San Francisco, California, January 2008. 20/74 = 27%.

[91] Cristian Soviani and Stephen A. Edwards. FIFO sizing for high-performance pipelines. In *Proceedings of the International Workshop on Logic Synthesis (IWLS)*, San Diego, California, June 2007.

[92] Olivier Tardieu and Stephen A. Edwards. Instantaneous transitions in Esterel. In *Proceedings of the Workshop on Model-Driven High-Level Programming of Embedded Systems (SLA++P)*, Braga, Portugal, March 2007. 9/16 = 56%.

[93] Becky Plummer, Mukul Khajanchi, and Stephen A. Edwards. An Esterel virtual machine for embedded systems. In *Proceedings of Synchronous Languages, Applications, and Programming (SLAP)*, Electronic Notes in Theoretical Computer Science, pages 1–14, Vienna, Austria, March 2006.

[94] Jia Zeng, Chuck Mitchell, and Stephen A. Edwards. A domain-specific language for generating dataflow analyzers. In *Proceedings of the Sixth Workshop on Language Descriptions, Tools and Applications*, Vienna, Austria, April 2006. 7/21 = 33%.

[95] Stephen A. Edwards. Using program specialization to speed SystemC fixed-point simulation. In *Proceedings of the Workshop on Partial Evaluation and Program Manipulation (PEPM)*, pages 21–28, Charleston, South Carolina, January 2006. 17/29 = 59%.

[96] Cristian Soviani, Stephen A. Edwards, and Angelos Keromytis. Adding a flow-oriented paradigm to commodity operating systems. In *Proceedings of the Workshop on Interaction between Operating System and Computer Architecture (IOSCA)*, pages 1–6, Austin, Texas, October 2005.

[97] Marcio Buss, Stephen A. Edwards, Bin Yao, and Daniel Waddington. Pointer analysis for source-to-source transformations. In *Proceedings of the 5th International Workshop on Source Code Analysis and Manipulation (SCAM)*, pages 139–148, Budapest, Hungary, September 2005. 18/48 = 38%.

[98] Cristian Soviani, Olivier Tardieu, and Stephen A. Edwards. High-level optimization by combining retiming and Shannon decomposition. In *Proceedings of the International Workshop on Logic Synthesis (IWLS)*, pages 16–23, Lake Arrowhead, California, June 2005. 33/67 = 49%.

[99] Cristian Soviani and Stephen A. Edwards. Challenges in synthesizing fast control-dominated circuits. In *Proceedings of the International Workshop on Logic Synthesis (IWLS)*, pages 326–332, Lake Arrowhead, California, June 2005. 34 posters/67 = 51%.

[100] Stephen A. Edwards. SHIM: A language for hardware/software integration. In *Proceedings of Synchronous Languages, Applications, and Programming (SLAP)*, Electronic Notes in Theoretical Computer Science, Edinburgh, Scotland, April 2005. 9/17 = 53%.

[101] Stephen A. Edwards. SHIM: A language for hardware/software integration. In *Proceedings of SYNCHRON*, Schloss Dagstuhl, Germany, December 2004.

[102] Stephen A. Edwards. The challenges of hardware synthesis from C-like languages. In *Proceedings of the International Workshop on Logic Synthesis (IWLS)*, pages 509–516, Temecula, California, June 2004. 33 talks/70 = 47%.

[103] Stephen A. Edwards, Vimal Kapadia, and Michael Halas. Compiling Esterel into static discrete-event code. In *Proceedings of Synchronous Languages, Applications, and Programming (SLAP)*, volume 153(4) of *Electronic Notes in Theoretical Computer Science*, pages 107–121, Barcelona, Spain, March 2004. Elsevier Science. 7/10 = 70%, 12 citations on Google Scholar.

[104] Stephen A. Edwards. High-level synthesis from the synchronous language Esterel. In *Proceedings of the International Workshop on Logic Synthesis (IWLS)*, New Orleans, Louisiana, June 2002. 22 long talks/80 = 28%. 14 citations on Google Scholar.

[105] Stephen A. Edwards. ESUIF: An open Esterel compiler. In *Proceedings of Synchronous Languages, Applications, and Programming (SLAP)*, volume 65(5) of *Electronic Notes in Theoretical Computer Science*, page 71, Grenoble, France, April 2002. Elsevier Science. 13/16 = 81%.

[106] Stephen A. Edwards. Compiling Esterel into sequential code. In *Proceedings of the 7th International Workshop on Hardware/Software Codesign (CODES)*, pages 147–151, Rome, Italy, May 1999. Association for Computing Machinery. 20/90 = 22%.

[107] Gitanjali Swamy, Stephen Edwards, and Robert Brayton. Efficient verification and synthesis using design commonalities. In *Proceedings of the International Workshop on Logic Synthesis (IWLS)*, Tahoe City, California, May 1997.

[108] Arlindo L. Oliveira and Stephen Edwards. Limits of exact algorithms for inference of minimum size finite state machines. In *Proceedings of the Seventh Annual Workshop on Algorithmic Learning Theory (ALT)*, volume 1160 of *Lecture Notes in Computer Science*, pages 59–66, Sydney, Australia, October 1996. Springer-Verlag. 16 long + 8 short/41 = 59%.

Theses

[109] John Hui. *Sparse Synchronous Programming with Temporal Abstractions*. PhD thesis, Columbia University, New York, New York, USA, October 2024.

[110] Richard Townsend. *Compiling Irregular Software to Specialized Hardware*. PhD thesis, Columbia University, Department of Computer Science, New York, New York, June 2019. Also technical report CUCS–002–19.

[111] Nalini Vasudevan. *Efficient, Deterministic and Deadlock-free Concurrency*. PhD thesis, Columbia University, New York, New York, USA, March 2011. CUCS–013–11.

[112] Marcio Buss. *Summary-Based Pointer Analysis Framework for Modular Bug Finding*. PhD thesis, Columbia University, New York, New York, USA, February 2008. CUCS–013–08.

[113] Jia Zeng. *Partial Evaluation for Code Generation from Domain-Specific Languages*. PhD thesis, Columbia University, New York, New York, USA, November 2007. CUCS–048–07.

[114] Cristian Soviani. *High Level Synthesis for Packet Processing Pipelines*. PhD thesis, Columbia University, New York, New York, USA, October 2007. CUCS–041–07.

[115] Stephen Anthony Edwards. *The Specification and Execution of Heterogeneous Synchronous Reactive Systems*. PhD thesis, University of California, Berkeley, May 1997. 44 citations on Google Scholar, Available as UCB/ERL M97/31.

[116] Stephen Edwards. An Esterel compiler for a synchronous/reactive development system. Master's thesis, University of California, Berkeley, June 1994. Available as UCB/ERL M94/43.

Technical Reports

[117] Stephen A. Edwards. The FHW project: High-level hardware synthesis from Haskell programs. Technical Report CUCS–003–19, Columbia University, Department of Computer Science, New York, New York, USA, August 2019.

[118] Richard Townsend, Martha A. Kim, and Stephen A. Edwards. Hardware in Haskell: Implementing memories in a stream-based world. Technical Report CUCS-017-15, Columbia University, Department of Computer Science, September 2015.

[119] Kuangya Zhai, Richard Townsend, Lianne Lairmore, Martha A. Kim, and Stephen A. Edwards. Hardware synthesis from a recursive functional language. Technical Report CUCS–007–15, Columbia University, Department of Computer Science, April 2015.

[120] Stephen A. Edwards. Functioning hardware from functional programs. Technical Report CUCS–027–13, Columbia University, Department of Computer Science, New York, New York, USA, October 2013.

[121] Stephen A. Edwards. A finer functional Fibonacci on a fast FPGA. Technical Report CUCS–005–13, Columbia University, Department of Computer Science, New York, New York, USA, February 2013.

[122] Stephen A. Edwards. Reconstructing Pong on an FPGA. Technical Report CUCS–0023–12, Columbia University, Department of Computer Science, New York, New York, USA, December 2012.

[123] Neil Deshpande and Stephen A. Edwards. Statically unrolling recursion to improve opportunities for parallelism. Technical Report CUCS–011–12, Columbia University, Department of Computer Science, New York, New York, USA, July 2012.

[124] Stephen A. Edwards. Functional Fibonacci to a fast FPGA. Technical Report CUCS–010–12, Columbia University, Department of Computer Science, New York, New York, USA, June 2012.

[125] Sungjun Kim, Hiren D. Patel, and Stephen A. Edwards. Using a model checker to determine worst-case execution time. Technical Report CUCS–038–09, Columbia University, Department of Computer Science, New York, New York, USA, September 2009.

[126] Devesh Dedhia. Example application under PRET environment — programming a MultiMediaCard. Technical Report CUCS–005–09, Columbia University, Department of Computer Science, New York, New York, USA, January 2009.

[127] Stephen A. Edwards. Retrocomputing on an FPGA. *Circuit Cellar*, 233:24–35, December 2009. Not peer-reviewed.

[128] Keerti Joshi and Delvin Kellebrew. A MPEG decoder in SHIM. Technical Report CUCS–057–08, Columbia University, Department of Computer Science, New York, New York, USA, December 2008.

[129] Nishant R. Shah. Memory issues in PRET machines. Technical Report CUCS–059–08, Columbia University, Department of Computer Science, New York, New York, USA, December 2008.

[130] David Lariviere and Stephen A. Edwards. uClinux on the Altera DE2. Technical Report CUCS–055–08, Columbia University, Department of Computer Science, New York, New York, USA, December 2008.

[131] Ravindra Babu Ganapathi and Stephen A. Edwards. SHIM optimization: Elimination of unstructured loops. Technical Report CUCS–054–08, Columbia University, Department of Computer Science, New York, New York, USA, December 2008.

[132] Dave Aaron Smith, Nalini Vasudevan, and Stephen Edwards. Static deadlock detection in SHIM with an automata type checking system. Technical Report CUCS–053–08, Columbia University, Department of Computer Science, New York, New York, USA, December 2008.

[133] Nalini Vasudevan, Olivier Tardieu, Julian Dolby, and Stephen A. Edwards. Analysis of clocks in x10 programs (extended). Technical Report CUCS–052–08, Columbia University, Department of Computer Science, New York, New York, USA, December 2008.

[134] Ben Lickly, Isaac Liu, Sungjun Kim, Hiren D. Patel, Stephen A. Edwards, and Edward A. Lee. Predictable programming on a precision timed architecture. Technical Report UCB/EECS-2008-40, University of California, Berkeley, April 2008.

[135] Marcio Buss, Daniel Brand, Vugranam Sreedhar, and Stephen A. Edwards. A new abstraction for summary-based pointer analysis. Technical Report RC24104, IBM, New York, July 2007.

[136] Chen-Chun Huang, Javier Coca, Yashket Gupta, and Stephen A. Edwards. An implementation of a Renesas H8/300 microprocessor with a cycle-level timing extension. Technical Report CUCS–051–06, Columbia University, Department of Computer Science, New York, New York, USA, December 2006.

[137] Nalini Vasudevan and Stephen A. Edwards. A JPEG decoder in SHIM. Technical Report CUCS–048–06, Columbia University, Department of Computer Science, New York, New York, USA, December 2006.

[138] Smridh Thapar, Olivier Tardieu, and Stephen A. Edwards. Arrays in SHIM: A proposal. Technical Report CUCS–047–06, Columbia University, Department of Computer Science, New York, New York, USA, December 2006.

[139] Stephen A. Edwards and Edward A. Lee. The case for the precision timed (PRET) machine. Technical Report UCB/EECS-2006-149, EECS Department, University of California, Berkeley, November 2006.

[140] Neesha Subramaniam, Ohan Oda, and Stephen A. Edwards. Macshim: Compiling matlab to a scheduling-independent concurrent language. Technical Report CUCS–038–06, Columbia University, Department of Computer Science, New York, New York, USA, September 2006.

[141] Olivier Tardieu and Stephen A. Edwards. Specifying confluent processes. Technical Report CUCS–037–06, Columbia University, Department of Computer Science, New York, New York, USA, September 2006.

[142] Olivier Tardieu and Stephen A. Edwards. Scheduling-independent threads and exceptions in SHIM. Technical Report CUCS–036–06, Columbia University, Department of Computer Science, New York, New York, USA, September 2006.

[143] Marcio Buss, Stephen A. Edwards, Bin Yao, and Daniel Waddington. Pointer analysis for C programs through AST traversal. Technical Report CUCS–028–05, Columbia University, Department of Computer Science, New York, New York, USA, August 2005.

[144] Christopher L. Conway, Kedar S. Namjoshi, Dennis Dams, and Stephen A. Edwards. Incremental algorithms for inter-procedural analysis of safety properties. Technical Report CUCS–018–05, Columbia University, Department of Computer Science, New York, New York, USA, July 2005.

[145] Stephen A. Edwards and Chun Li. Determining interfaces using type inference. Technical Report CUCS–052–04, Columbia University, Department of Computer Science, New York, New York, USA, December 2004.

[146] Cristian Soviani, Jia Zeng, and Stephen A. Edwards. Sequential challenges in synthesizing Esterel. Technical Report CUCS–051–04, Columbia University, Department of Computer Science, New York, New York, USA, December 2004.

[147] Stephen A. Edwards. Design and verification languages. Technical Report CUCS–046–04, Columbia University, Department of Computer Science, New York, New York, USA, November 2004.

[148] Hanoril Estevez and Stephen A. Edwards. Live CD cluster performance. Technical Report CUCS–037–04, Columbia University, Department of Computer Science, New York, New York, USA, October 2004.

[149] Cristian Soviani, Jia Zeng, and Stephen A. Edwards. Improved controller synthesis from Esterel. Technical Report CUCS–015–04, Columbia University, Department of Computer Science, New York, New York, USA, March 2004.

[150] Stephen A. Edwards. Design languages for embedded systems. Technical Report CUCS–009–03, Columbia University, Department of Computer Science, New York, New York, USA, May 2003.

Professional Activities

Professional Society Memberships

Senior Member, IEEE 2006–

Member, ACM 2006–

Member, IEEE 1994–2006

Standarization Committees

Vice Chair, IEEE P1778 Esterel Standardization Committee, 2007–2009

Journal Activities

- IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems
  Top journal in my area.
  Associate Editor 2006–
  Guest Editor, special section on the Intl. Workshop on Logic and Synthesis May 2006
  Reviewer 1994, 2001–2003, 2006–2009, 2013, 2017–2018, 2023
- ACM Transactions on Embedded Computer Systems
  Associate Editor 2008–
  Reviewer 2004, 2006–2007, 2009–2011, 2016–2018
- IEEE Transactions on Industrial Informatics
  Associate Editor 2007–
  Reviewer 2009
- EURASIP International Journal of Embedded Systems
  Associate Editor 2004–
  Reviewer 2007–2010
- IEEE Embedded Systems Letters
  Reviewer 2010–
- Real-Time Systems
  Reviewer 2010
- Science of Computer Programming
  Reviewer 2010–2011, 2018, 2019
- Journal of Systems Architecture
  Reviewer 2013
- Proceedings of the IEEE
  Reviewer 2015
- Computer Architecture Letters
  Reviewer 2019

Conference/Workshop Activities

- Design Automation Conference (DAC)
  Top conference in my area; 15%-20% paper acceptance rate
  Technical Subcommittee Chair, *Managed four TPC members and 50+ papers.* 2006–2007, 2011
  TPC Member, *Responsible for 30+ paper reviews per year.* 2004–2006, 2012, 2024–2025
  Reviewer 1996–2004, 2008–

- Design, Automation, and Test in Europe (DATE)
  Second-to-top conference in my area.
  Topic Committee Member 2002–2004, 2007

- International Conference on Computer-Aided Design (ICCAD)
  Third-to-top conference in my area.
  TPC Subcommittee Chair, *Invited to head new embedded systems software track* 2011

- International Workshop on Logic and Synthesis (IWLS)
  Main workshop for logic synthesis, approx. 100 attendees
  Program Chair 2006
  General Chair 2005
  Publicity and Publications Chair 2003–2004
  TPC Member 2003–2009, 2011–2012, 2015, 2017, 2018

- Embedded Systems Week
  Local Arrangements Chair 2005
  Publicity Chair (EMSOFT conference) 2003–2004
  TPC Member (EMSOFT conference) 2004–2006, 2010, 2013, 2015, 2023, 2024
  TPC Member (CODES+ISSS conference) 2008, 2009, 2010
  Reviewer (EMSOFT conference) 2008, 2011, 2014, 2016

- Time-Centric Reactive Software (TCRS) Workshop Organizing Committe Member, 2023
  TPC Member, 2023–2024

- Synchronous Languages, Applications, and Programming (SLAP)
  Steering Committee Member 2006–
  TPC Member 2002–2006

- Memocode conference
  General Chair 2023–2024
  Program Chair 2007–2008
  Design Contest Chair 2012
  Publicity Chair 2003–2004, 2006
  TPC Member 2003–2007, 2009, 2011–2012, 2017–2022
  Panel Organizer 2009

- Languages, Compilers, and Techniques for Embedded Systems (LCTES)
  TPC Member 2006, 2010

- IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)
  TPC Member 2005, 2006

- Forum on Specification & Design Languages (FDL) TPC Member 2016, 2017, 2023, 2024, 2025

- Embedded and Ubiquitous Computing (EUC)
  TPC Member 2006–2008
- International Conference on Computer Design (ICCD)
  TPC Member 2004–2005
- Applications of Concurrency to System Design (ACSD)
  TPC Member 2004–2008
- Workshop on Modeling, Validation and Heterogeneity (MoVaH)
  TPC Member 2008
- ACM SIGPLAN Workshop on Partial Evaluation and Program Manipulation (PEPM)
  TPC Member 2008
- International Conference on Hybrid Systems: Computation and Control (HSCC)
  TPC Member 2008
- Language Descriptions Tools, Analysis (LDTA)
  TPC Member 2009
- International Conference on Software Language Engineering (SLE)
  TPC Member 2009, 2010
- Real-time Systems Symposium (RTSS)
  TPC Member 2009
- IEEE Intl. Conf. on Compilers, Architectures, and Synthesis of Embedded Systems (CASES)
  TPC Member 2013, 2014, 2025

Invited Talks

Keynotes

Language Design is LEGO Design and Library Design. September 3, 2019
Presented at Forum on Specification and Design Languages. University of Southampton, UK.

Haskell to Hardware and Other Dreams. December 7, 2016
Presented at Synchron, Bamberg, Germany.

Functioning Hardware from Functional Specifications June 26, 2014
Presented at Applications of Concurrency to System Design (ASCSD), Tunis, Tunisia.

Compiling Parallel Algorithms to Memory Systems June 2, 2012
Presented at the 2012 Electronic System Level Synthesis Conf. (ESLsyn), San Francisco, California.

Conferences/Other

Ubiquitous Unix Units. October 22, 2019
Presented at Unix50. Nokia Bell Labs, Murray Hill, NJ.

Net Booting/Installing Vintage Computers from a Raspberry Pi. May 3, 2019
Presented at Vintage Computer Festival — East. Infoage Science Center, Wall, New Jersey.

The Altair 8800 Computer: The Start of the Personal Computer Revolution. April 11, 2018
Presented at the CSTA Central NJ Meeting, Princeton, New Jersey.

Functioning Hardware from Functional Specifications November 18, 2014
Presented at IBM Programming Languages Day, T. J. Watson Research Center, New York.

Functioning Hardware from Functional Specifications July 22, 2014
Presented at the DIMACS Workshop on Multicore and Cryptography, Hoboken, New Jersey.

Functioning Hardware from Functional Specifications November 18, 2013
Presented at the SYNCHRON workshop, Schloss Dagstuhl, Germany.

Compiling Parallel Algorithms to Memory Systems May 29, 2012
Presented at the Resource-Aware Functional Programming (RAWFP) Workshop, Göteborg, Sweden.

From Recursive Functions to Real FPGAs March 4, 2012
Presented at Compiling Complete Programs into Circuits (CCPC), London, UK.

High-level Synthesis from Functional Languages October 19, 2012
Presented at Synchronics Days, Paris, France.

What Do We Do With 10^{12} Transistors? The Case for Precision Timing February 21, 2008
Presented at the DSRC TeraChip Workshop, Stanford, California.

Verification Challenges in the SHIM Concurrent Language May 18, 2007
Invited talk at the Third Northeast Verification Seminar, NEC, Princeton, New Jersey.

Verification: What Works and What Does Not? May 18, 2007
Panel at the Third Northeast Verification Seminar, NEC, Princeton, New Jersey.

Using and Compiling Esterel July 11th, 2005
Invited Tutorial, Memocode conference, Verona, Italy.

The Future of Embedded Linux. June 30, 2005
Panel at C3Expo, New York, NY.

Languages for Embedded Systems August 2–6, 2004
Week-long course at National Chiao Tung University, Hsinchu, Taiwan.

Linux for EDA November 2003
Tutorial at the International Conference on Computer-Aided Design (ICCAD), San Jose, California.

High-Level Modeling and Validation Methodologies for Embedded Systems:
Bridging the Productivity Gap January 4, 2003
Presented at VLSI Design 2003, New Delhi, India.
With Sandeep K. Shukla, Jean Pierre Talpin, and Rajesh K. Gupta.

System-on-a-chip and the Coming Design Revolution November 1, 2002
Invited talk at the Emerging Information Technology Conference (EITC), Princeton, New Jersey.

Scaling the Abstraction Cliff: High-level Languages for System Design March 2001
Tutorial A2 at the Design, Automation and Test in Europe (DATE 2001) Munich, Germany.

Universities/Industry

The Sparse Synchronous Model April 30, 2024
Presented at Chalmers University, Göteborg, Sweden.

The Sparse Synchronous Model April 25, 2024
Presented at Technische Universität Dresden, Germany.

CPUs, GPUs, and the Rise of Software Parallelism December 16, 2013
Presented at Chalmers University, Göteborg, Sweden, as an introduction to Joel Svensson's PhD Defense.

Functioning Hardware from Functional Specifications December 17, 2013
Presented at Chalmers University, Göteborg, Sweden.

Compiling Parallel Algorithms to Memory Systems June 26, 2012
Presented to the PARKAS group, DI, École Normale Supérieure.

Compiling Parallel Algorithms to Memory Systems April 16, 2012
Presented at Jane Street, New York, NY

Concurrency and Communication: Lessons from the SHIM Project August 6, 2010
Cambridge University, UK

Concurrency and Communication: Lessons from the SHIM Project July 23, 2010
Microsoft Research, Cambridge, UK

Concurrency and Communication: Lessons from the SHIM Project July 5, 2010
University of the Philippines, Manila

Programming Shared Memory Multiprocessors with Deterministic Message-Passing Concurrency:
Compiling SHIM to Pthreads August 8, 2008
National Taiwan University, Taipei, Taiwan

What Do We Do With 10^{12} Transistors? The Case for Precision Timing February 20, 2008
Google, Mountain View, California

Precision-Timed (PRET) Machines January 9, 2007
Altera, San Jose, California

Precision-Timed (PRET) Machines July 6, 2007
National Taiwan University, Taipei, Taiwan

SHIM: A Scheduling-Independent Concurrent Language for Embedded Systems May 10, 2007
Princeton University, New Jersey

SHIM: A Scheduling-Independent Concurrent Language for Embedded Systems April 27, 2007
University of Pennsylvania, Philadelphia

SHIM: A Scheduling-Independent Concurrent Language for Embedded Systems March 16, 2007
MIT, Boston, Massachusetts

SHIM: A Scheduling-Independent Concurrent Language for Embedded Systems March 13, 2007
CEA, Grenoble, France

SHIM: A Scheduling-Independent Concurrent Language for Embedded Systems November 8, 2006
University of California, Berkeley

The Challenges of Hardware Synthesis from C-Like Languages September 18, 2006
ECSI-UBS Workshop on High Level Synthesis, Darmstadt, Germany.

SHIM: A Deterministic Language for Embedded Systems August 28, 2006
SpringSoft, Hsinchu, Taiwan.

SHIM: A Deterministic Language for Embedded Systems August 28, 2006
National Chiao Tung University (NCTU), Hsinchu, Taiwan.

SHIM: A Deterministic Language for Embedded Systems August 23, 2006

Microsoft Research, Bangalore, India.

SHIM: A Deterministic Language for Embedded Systems — August 11, 2006
Tsinghua University, Hsinchu, Taiwan.

SHIM: A Deterministic Language for Embedded Systems — August 10, 2006
National Taiwan University, Taipei.

SHIM: A Deterministic Language for Embedded Systems — August 4, 2006
Seoul National University, Korea.

SHIM: A Deterministic Language for Embedded Systems — July 21, 2006
University of Kiel, Germany.

SHIM: A Deterministic Model for Heterogeneous Embedded Systems — December 9, 2005
Verimag, Grenoble, France.

SHIM: A Deterministic Model for Heterogeneous Embedded Systems — November 10, 2005
University of California at Berkeley.

SHIM: A Deterministic Model for Heterogeneous Embedded Systems — November 9, 2005
Xilinx, San Jose, California.

SHIM: A Deterministic Model for Heterogeneous Embedded Systems — October 7th, 2005
National Instruments and the University of Texas at Austin.

SHIM: A Deterministic Model for Heterogeneous Embedded Systems — August 16th, 2005
Tsinghua University, Hsinchu, Taiwan.

Deterministic Receptive Processes are Kahn Processes. — June 22, 2005
INRIA, Sophia-Antipolis, France.

SHIM: A Language for Hardware/Software Integration. — April 7, 2005
University of California, Irvine.

Using and Compiling Esterel — August 17, 2004
National Chung Cheng University, Chai-Yi, Taiwan.

Making cyclic circuits acyclic — March 3, 2003
Carnegie Mellon, Pittsburgh.

Compiling Esterel — January 13, 2003
Indian Institute of Technology, Delhi.

Compiling Esterel into Better Circuits and Faster Simulations. — November 5, 2002
Intel, Hillsboro, Oregon.

Compiling Esterel — October 10, 2002
Cambridge University, UK.

Compiling Esterel — September 5, 2002
University of California, Berkeley.

Compiling Esterel — August 26, 2002
University of Calgary, Alberta, Canada.

Compiling Esterel — August 19, 2002
Microsoft Research, Redmond, Washington.

High-level Synthesis from the Synchronous Language Esterel — August 8, 2002

Intel, Hillsboro, Oregon.

An Overview of the Electronic Design Automation (EDA) Field — July 16, 2002
Yuan Ze University, Chungli, Taiwan.

Compiling Esterel — July 8, 2002
National Taiwan University (Taida), Taipei, Taiwan.

Compiling Esterel — April 2002
A discussion of my first Esterel compiler along with ongoing work on ESUIF.
Princeton, New Jersey.

ESUIF: An Open Esterel Compiler — March 2002
A work-in-progress description of the ESUIF Esterel compiler.
IRISA/INRIA Rennes, France.

Esterel and Other Projects — October 2001
A summary of existing Esterel work and future plans
Intel, Hillsboro, Oregon.

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