IP Cores and Platform Designer

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IP Cores

IP Integration with Quartus

IP Integration with Platform Designer

Bus Bridges

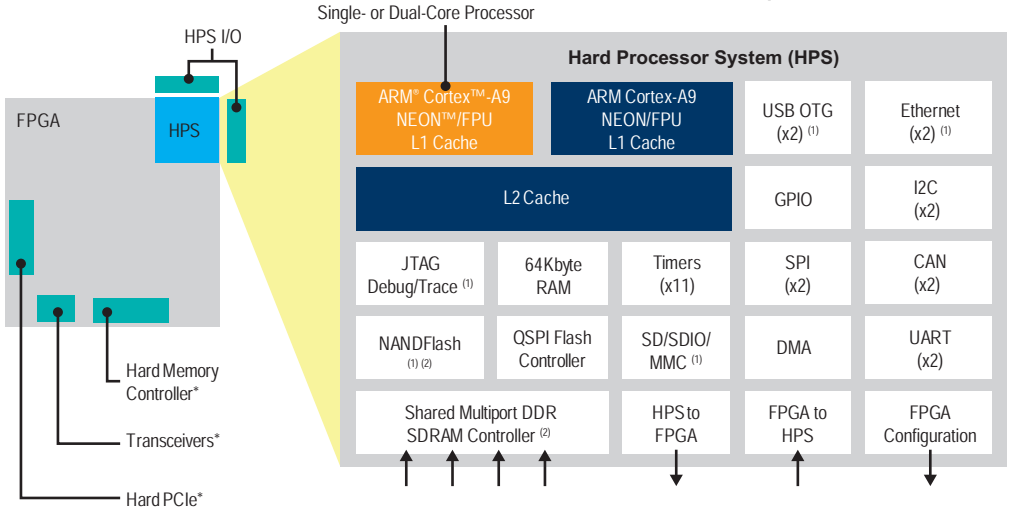
Control and Data Planes

IP Cores

Cyclone V SoC: A Mix of Hard and Soft IP Cores

IP = Intellectual Property
Hard = wires & transistors

Core = block, design, circuit, etc.
Soft = implemented w/ FPGA



Source: Altera

Example IP Cores

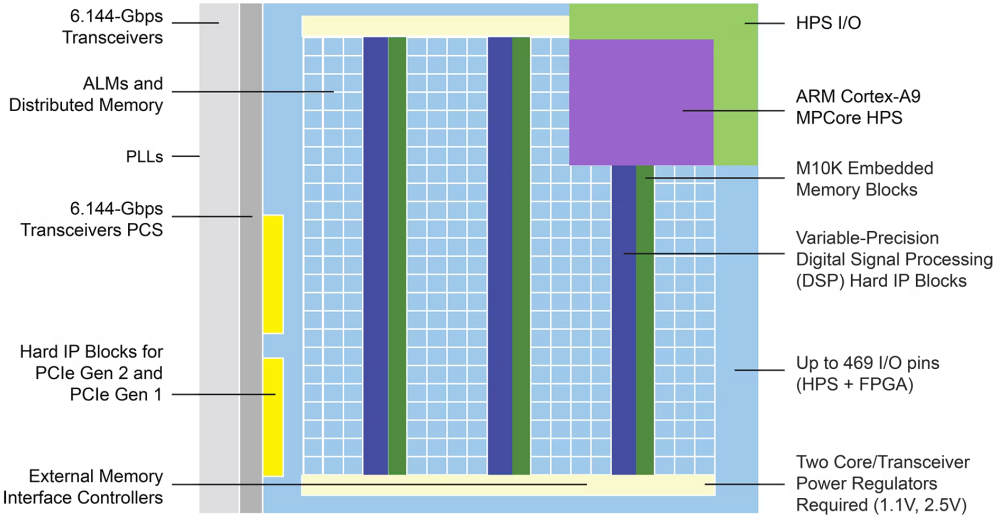
CPUs: ARM (hard), NIOS-II (soft)

Highspeed I/O: Hard IP Blocks for High Speed Transceivers (PCI Express, 10Gb Ethernet)

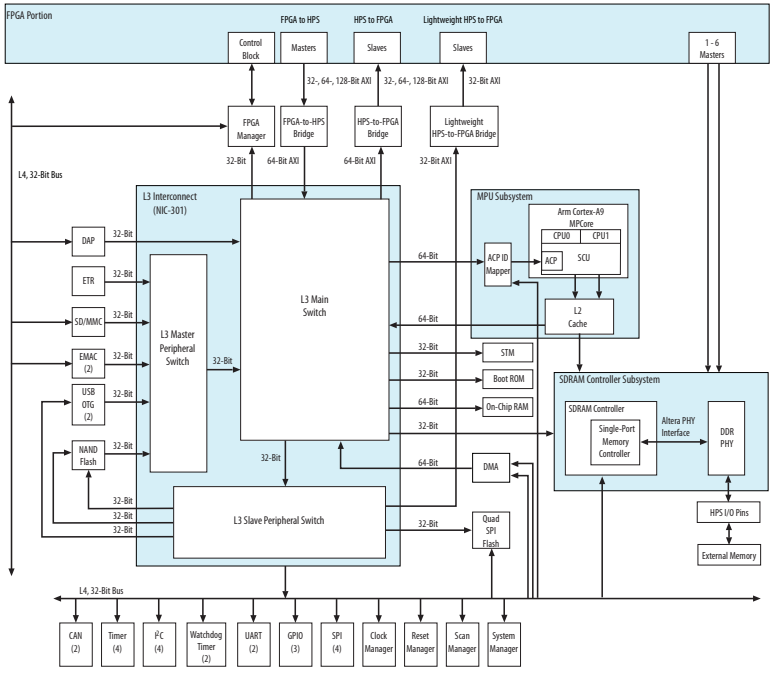
Memory Controllers: DDR3

Clock and Reset signal generation: PLLs

Cyclone V SoC: FPGA layout



Source: Altera



Cyclone V SoC: HPS Block Diagram

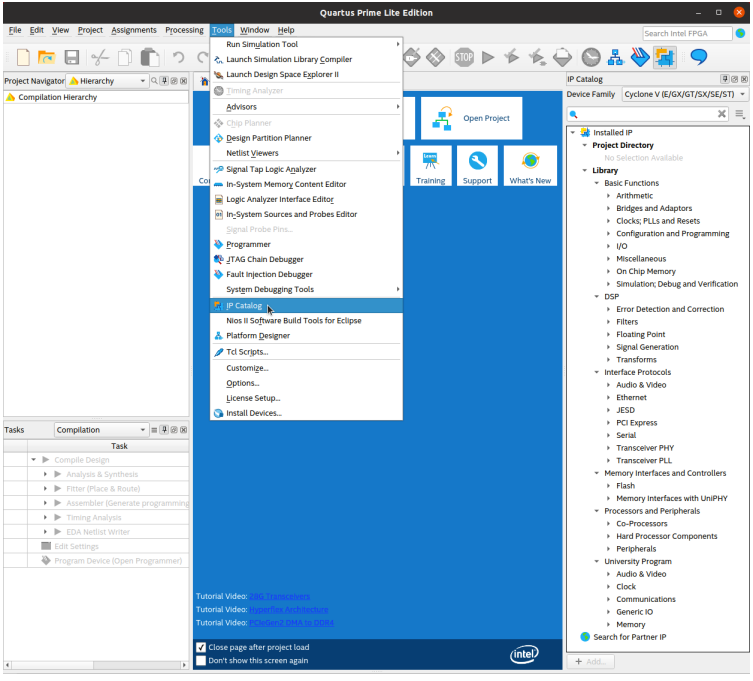
These are all hard IP cores

Source: Altera Cyclone V Hard Processor System Technical Reference Manual

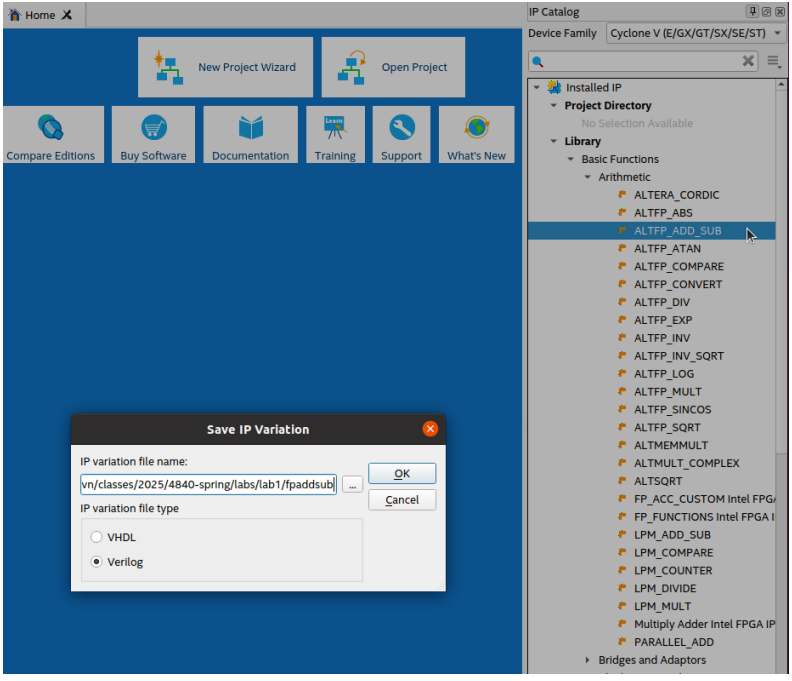
IP Integration with Quartus

The IP Catalog in Quartus

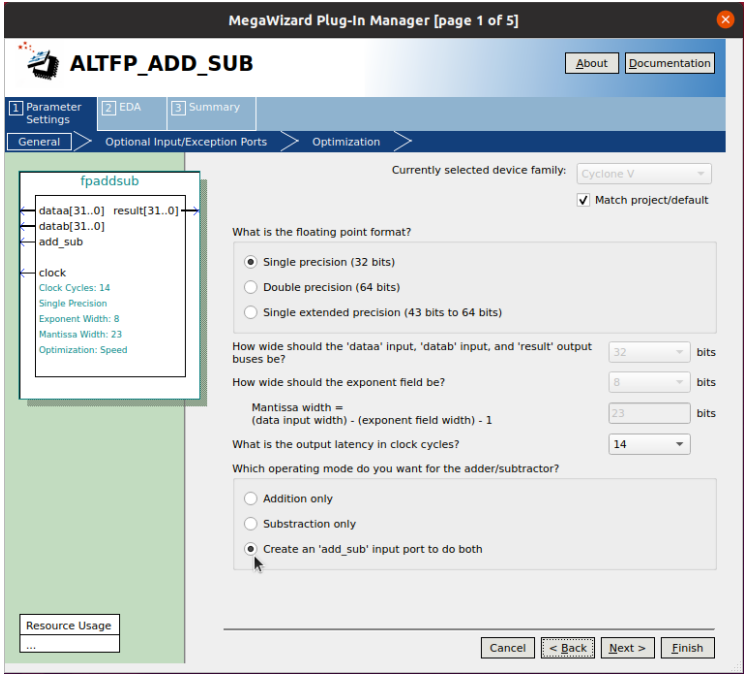
Formerly the “Megawizard”



Selecting a floating-point add/sub IP core



Setting its parameters



Resulting fpaddsub.v

```
module fpaddsub ( add_sub, clock, dataa, datab, result);
  input           add_sub, clock;
  input   [31:0]  dataa, datab;
  output  [31:0]  result;

  wire [31:0] sub_wire0;
  wire [31:0] result = sub_wire0[31:0];

  altfp_add_sub   altfp_add_sub_component (.add_sub (add_sub),
                                           .clock (clock),
                                           .dataa (dataa),
                                           .datab (datab),
                                           .result (sub_wire0));

  defparam altfp_add_sub_component.denormal_support = "NO",
           altfp_add_sub_component.direction = "VARIABLE",
           altfp_add_sub_component.optimize = "SPEED",
           altfp_add_sub_component.pipeline = 14,
           altfp_add_sub_component.reduced_functionality = "NO",
           altfp_add_sub_component.width_exp = 8,
           altfp_add_sub_component.width_man = 23;
endmodule
```

Megawizard IP Cores

Core-specific interfaces on each

Arithmetic: $+$, $-$, $\times$, $\div$, Multiply-Accumulate, ECC

Floating Point: $+$, $-$, $\times$, $\div$

Gate Functions: Shift Registers, Decoders, Multiplexers

I/O Functions: PLL, temp sensor, remote update, high speed transceivers

Memory: Single/Dual-port RAMs, Single/Dual-clock FIFOs, Shift registers

DSP: FFT, ECC, FIR, etc.

Video: large suite

Some megafunctions are only available on certain FPGAs

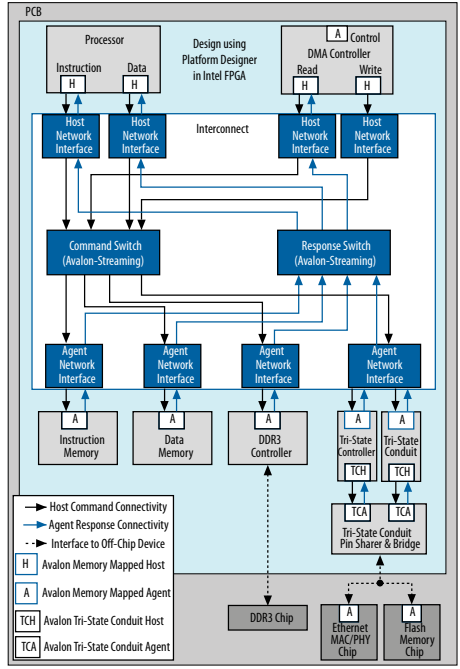
IP Integration with Platform Designer

Altera Platform Designer

Generates the interconnect logic for connecting a mix of IP Cores with Avalon/AXI/APB/ACE interfaces

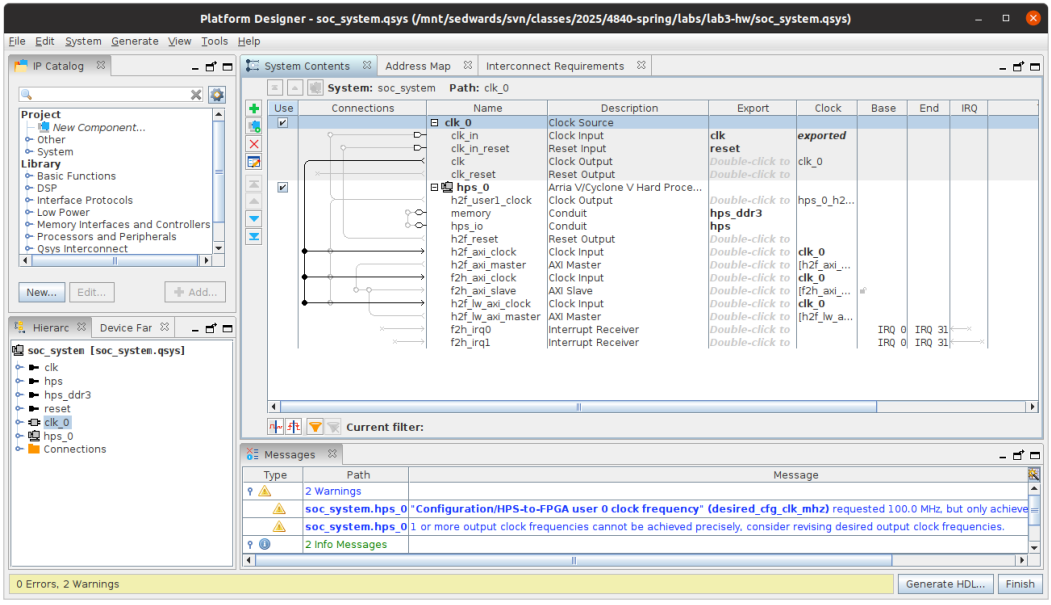
You specify the components and their connections and Platform Designer generates the Verilog for it all

Formerly “Qsys”



Source: Altera Platform Designer User Guide

Platform Designer



Bus Bridges

Bus Bridges

A bus bridge connects two, often different, buses.

Enables multiple clock domains, different protocols (e.g., AXI $\leftrightarrow$ Avalon), bus widths, etc.

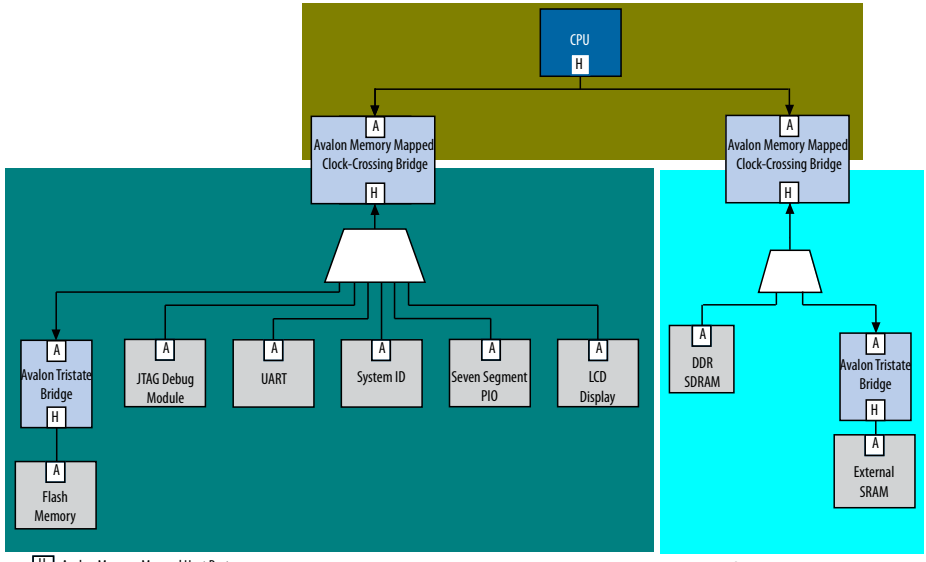
Example Bridge Types:

SOC HPS $\leftrightarrow$ FPGA Bridge

Avalon MM Clock Crossing Bridge

Avalon MM Pipeline Bridge

Clock Crossing Bridge Example



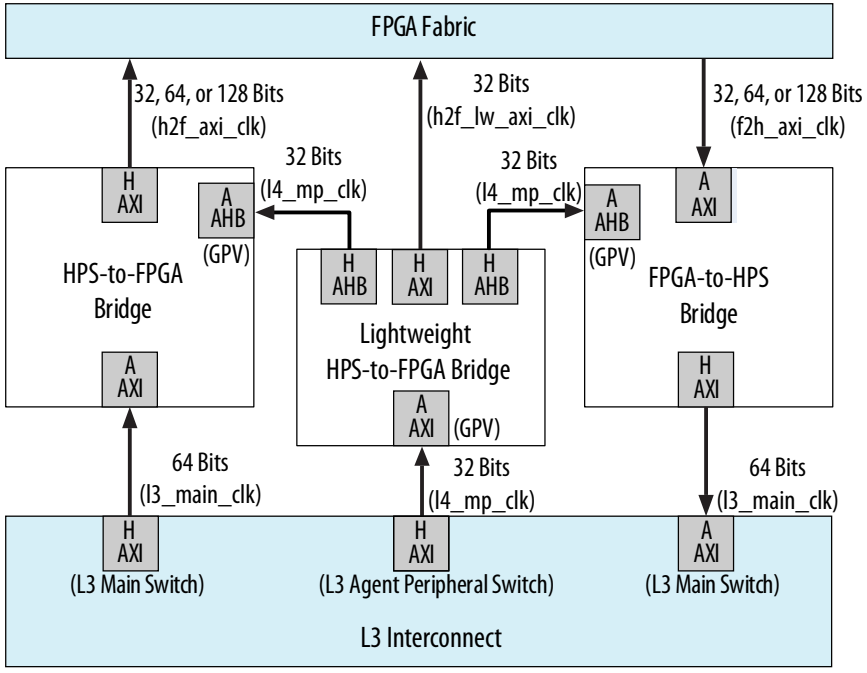
Source: Altera Platform Designer User Guide

Cyclone V HPS-FPGA Bridges

32-bit lightweight for configuration

32/64/128 high-performance FPGA agents

32/64/128 high-performance FPGA hosts



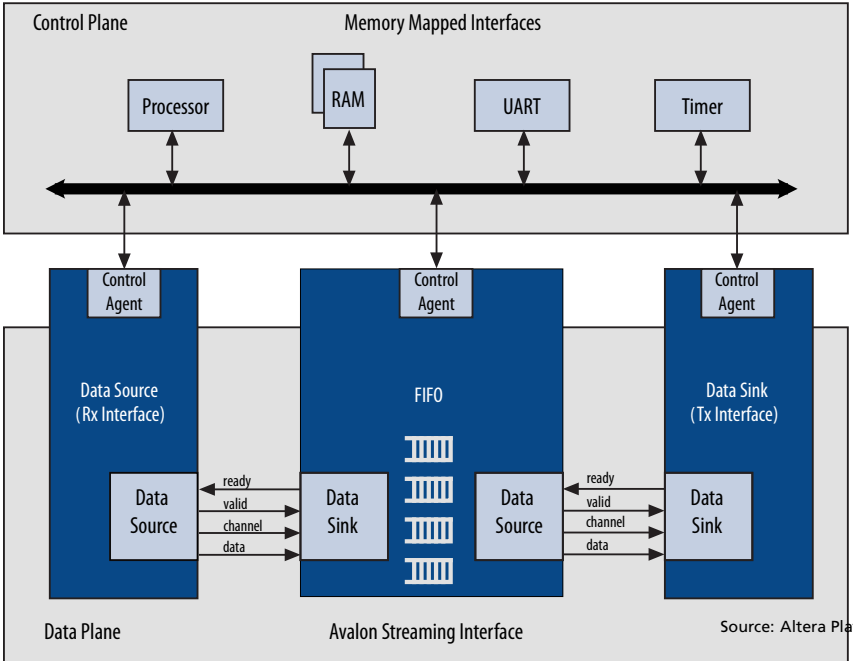
Control and Data Planes

Control vs. Data Planes

Control Plane: Memory mapped registers typically used for configuring devices, querying status, initiating transactions, etc (low bandwidth)

Data Plane: Streaming directed graphs for actually moving and processing large amounts of data (audio/video, network packets, etc); high bandwidth

A single IP core can have both MM and ST interfaces (including multiple of each).



Source: Altera Platform Designer User Guide

References to Altera Documentation

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Quartus Prime Standard Edition User Guide: Platform Designer

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