

# IP Cores and Platform Designer

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IP Cores

IP Integration with Quartus

IP Integration with Platform Designer

Bus Bridges

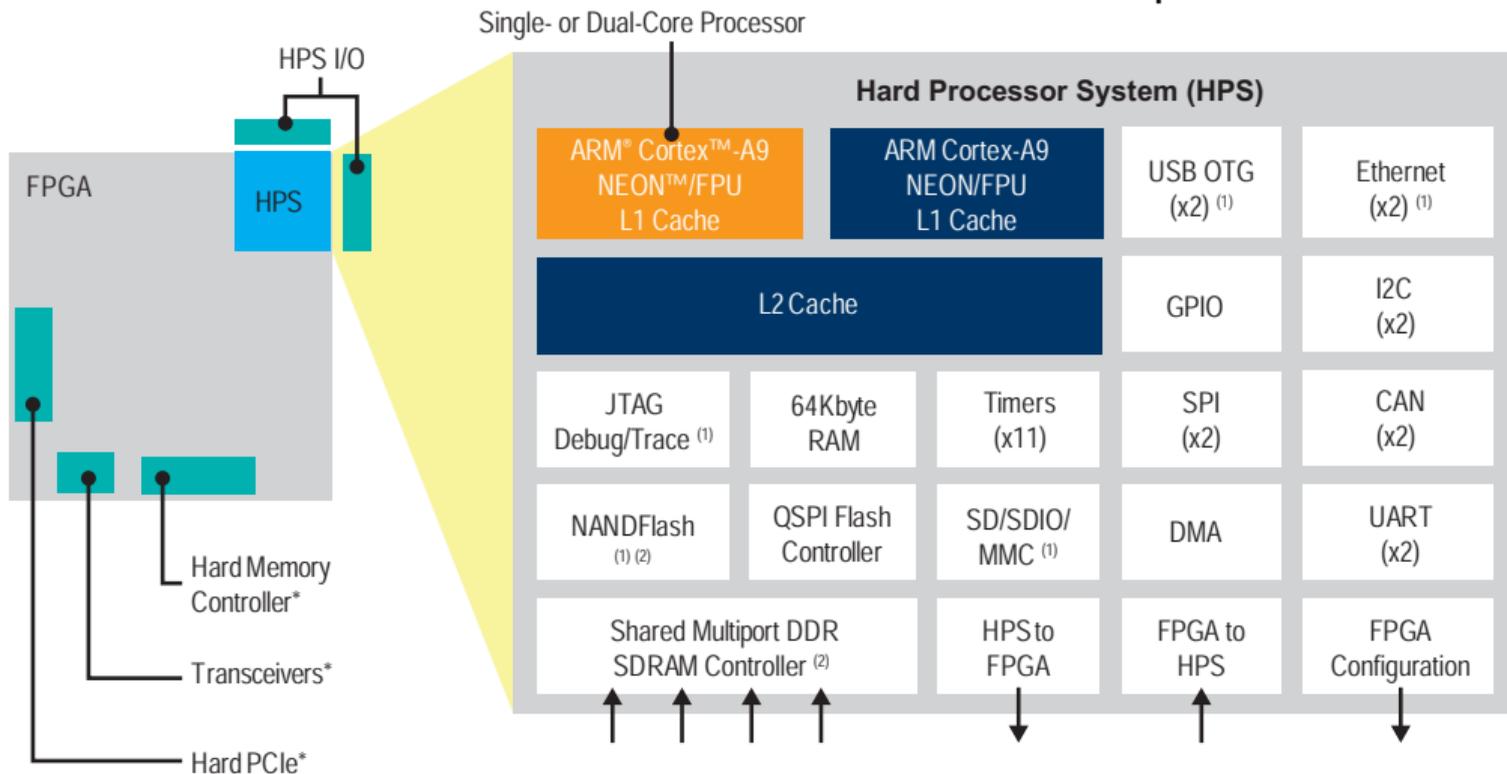
Control and Data Planes

# IP Cores

# Cyclone V SoC: A Mix of Hard and Soft IP Cores

IP = Intellectual Property  
Hard = wires & transistors

Core = block, design, circuit, etc.  
Soft = implemented w/ FPGA



## Example IP Cores

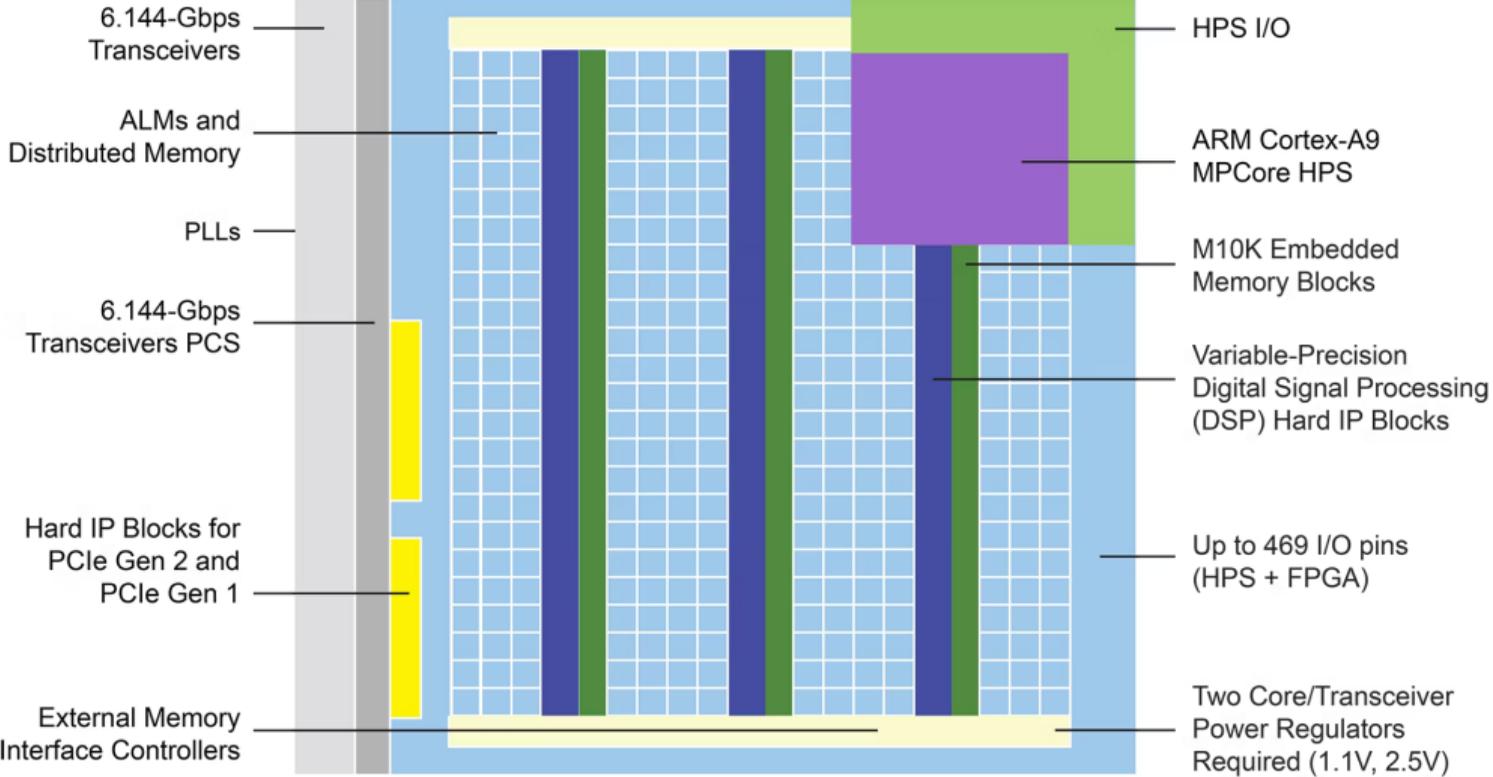
**CPUs:** ARM (hard), NIOS-II (soft)

**Highspeed I/O:** Hard IP Blocks for High Speed Transceivers (PCI Express, 10Gb Ethernet)

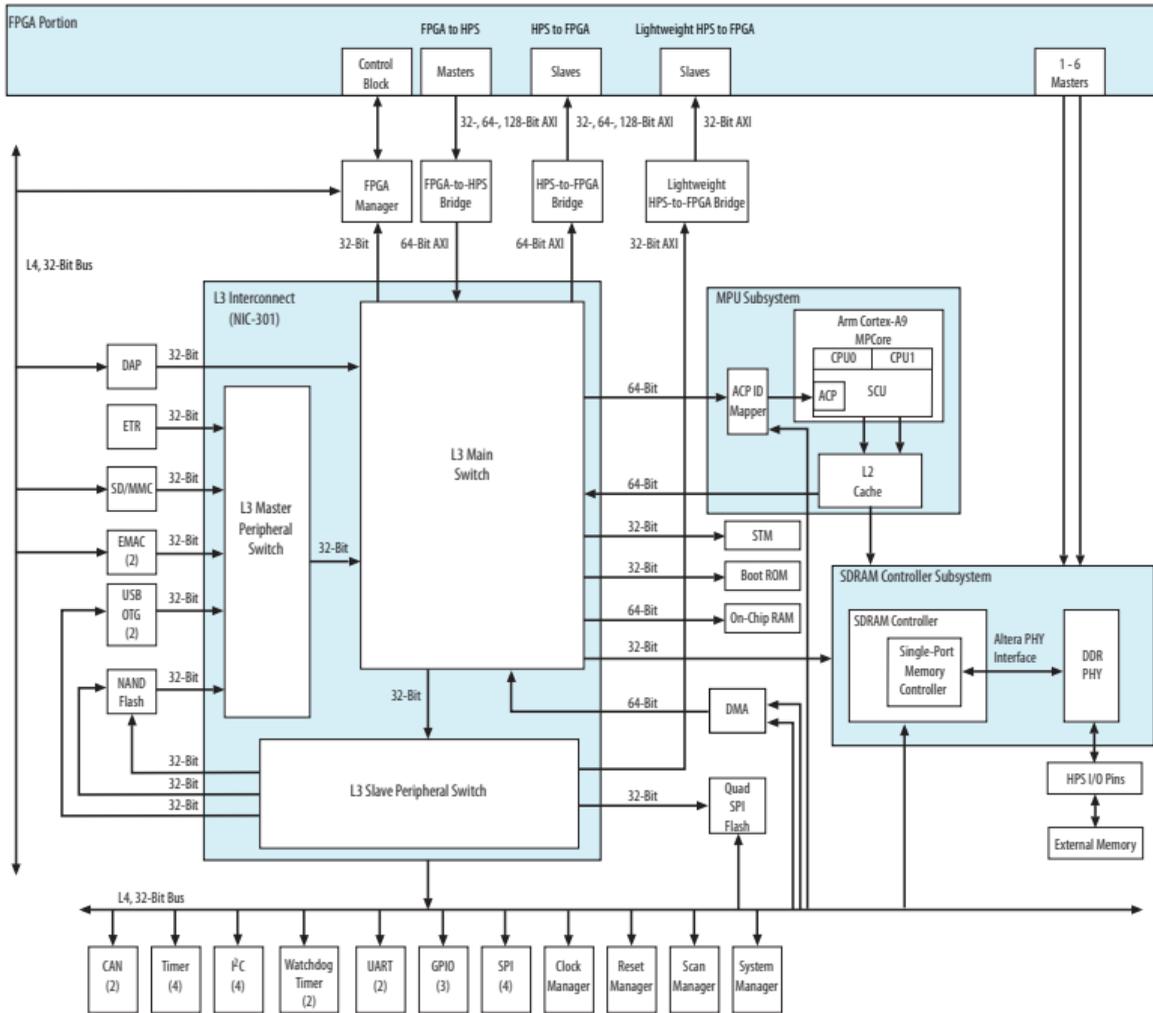
**Memory Controllers:** DDR3

**Clock and Reset signal generation:** PLLs

# Cyclone V SoC: FPGA layout



Source: Altera



# Cyclone V SoC: HPS Block Diagram

These are all hard IP cores

Source: Altera Cyclone V Hard Processor System Technical Reference Manual

# IP Integration with Quartus

# The IP Catalog in Quartus

## Formerly the "Megawizard"

The screenshot shows the Quartus Prime Lite Edition interface. The IP Catalog window is open, displaying a list of IP blocks. The 'IP Catalog' menu item is highlighted in the Tools menu. The IP Catalog window shows the following structure:

- Installed IP
  - Project Directory
    - No Selection Available
  - Library
    - Basic Functions
      - Arithmetic
      - Bridges and Adaptors
      - Clocks; PLLs and Resets
      - Configuration and Programming
      - I/O
      - Miscellaneous
      - On Chip Memory
      - Simulation; Debug and Verification
    - DSP
      - Error Detection and Correction
      - Filters
      - Floating Point
      - Signal Generation
      - Transforms
    - Interface Protocols
      - Audio & Video
      - Ethernet
      - JESD
      - PCI Express
      - Serial
      - Transceiver PHY
      - Transceiver PLL
    - Memory Interfaces and Controllers
      - Flash
      - Memory Interfaces with UniPHY
    - Processors and Peripherals
      - Co-Processors
      - Hard Processor Components
      - Peripherals
    - University Program
      - Audio & Video
      - Clock
      - Communications
      - Generic IO
      - Memory

At the bottom of the IP Catalog window, there are three tutorial video links:

- Tutorial Video: [20G Transceivers](#)
- Tutorial Video: [Quad Bus Architecture](#)
- Tutorial Video: [Streaming Data to DDR4](#)

At the bottom of the IP Catalog window, there are two checkboxes:

- Close page after project load
- Don't show this screen again

The Intel logo is visible in the bottom right corner of the IP Catalog window.

Selecting a  
floating-point  
add/sub IP core

The screenshot shows the IP Catalog window in Quartus Prime. The top bar indicates the device family is Cyclone V (E/GX/GT/SX/SE/ST). The main area displays a list of installed IP cores under the 'Library' > 'Basic Functions' > 'Arithmetic' category. The 'ALTFP\_ADD\_SUB' core is highlighted with a mouse cursor. A 'Save IP Variation' dialog box is open in the foreground, showing the file name 'vn/classes/2025/4840-spring/labs/lab1/fpaddsub' and the file type set to 'Verilog'.

Home X

New Project Wizard Open Project

Compare Editions Buy Software Documentation Training Support What's New

IP Catalog

Device Family Cyclone V (E/GX/GT/SX/SE/ST)

Installed IP

- Project Directory  
No Selection Available
- Library
  - Basic Functions
    - Arithmetic
      - ALTFP\_ADD\_SUB
      - ALTFP\_ABS
      - ALTFP\_ATAN
      - ALTFP\_COMPARE
      - ALTFP\_CONVERT
      - ALTFP\_DIV
      - ALTFP\_EXP
      - ALTFP\_INV
      - ALTFP\_INV\_SQRT
      - ALTFP\_LOG
      - ALTFP\_MULT
      - ALTFP\_SINCOS
      - ALTFP\_SQRT
      - ALTMEMMULT
      - ALTMULT\_COMPLEX
      - ALTSQRT
      - FP\_ACC\_CUSTOM Intel FPGA
      - FP\_FUNCTIONS Intel FPGA I
      - LPM\_ADD\_SUB
      - LPM\_COMPARE
      - LPM\_COUNTER
      - LPM\_DIVIDE
      - LPM\_MULT
      - Multiply Adder Intel FPGA IP
      - PARALLEL\_ADD

Save IP Variation

IP variation file name:  
vn/classes/2025/4840-spring/labs/lab1/fpaddsub

IP variation file type:  
 VHDL  
 Verilog

OK Cancel

Bridges and Adaptors



## ALTFP\_ADD\_SUB

About

Documentation

1 Parameter  
Settings

2 EDA

3 Summary

General

Optional Input/Exception Ports

Optimization

## fpaddsub

dataa[31..0] result[31..0]  
datab[31..0]  
add\_sub  
clock  
Clock Cycles: 14  
Single Precision  
Exponent Width: 8  
Mantissa Width: 23  
Optimization: Speed

Resource Usage

...

Currently selected device family: Cyclone V

 Match project/default

What is the floating point format?

- Single precision (32 bits)  
 Double precision (64 bits)  
 Single extended precision (43 bits to 64 bits)

How wide should the 'dataa' input, 'datab' input, and 'result' output buses be? 32 bits

How wide should the exponent field be? 8 bits

Mantissa width =  
(data input width) - (exponent field width) - 1 23 bits

What is the output latency in clock cycles? 14

Which operating mode do you want for the adder/subtractor?

- Addition only  
 Subtraction only  
 Create an 'add\_sub' input port to do both

Cancel

&lt; Back

Next &gt;

Finish

Setting its  
parameters

## Resulting fpaddsub.v

```
module fpaddsub ( add_sub, clock, dataa, datab, result);
  input          add_sub, clock;
  input  [31:0]  dataa, datab;
  output [31:0]  result;

  wire [31:0] sub_wire0;
  wire [31:0] result = sub_wire0[31:0];

  altfp_add_sub  altfp_add_sub_component (.add_sub (add_sub),
                                          .clock (clock),
                                          .dataa (dataa),
                                          .datab (datab),
                                          .result (sub_wire0));

  defparam altfp_add_sub_component.denormal_support = "NO",
           altfp_add_sub_component.direction = "VARIABLE",
           altfp_add_sub_component.optimize = "SPEED",
           altfp_add_sub_component.pipeline = 14,
           altfp_add_sub_component.reduced_functionality = "NO",
           altfp_add_sub_component.width_exp = 8,
           altfp_add_sub_component.width_man = 23;
endmodule
```

# Megawizard IP Cores

*Core-specific interfaces on each*

**Arithmetic:** +, -, ×, ÷, Multiply-Accumulate, ECC

**Floating Point:** +, -, ×, ÷

**Gate Functions:** Shift Registers, Decoders, Multiplexers

**I/O Functions:** PLL, temp sensor, remote update, high speed transceivers

**Memory:** Single/Dual-port RAMs, Single/Dual-clock FIFOs, Shift registers

**DSP:** FFT, ECC, FIR, etc.

**Video:** large suite

*Some megafunctions are only available on certain FPGAs*

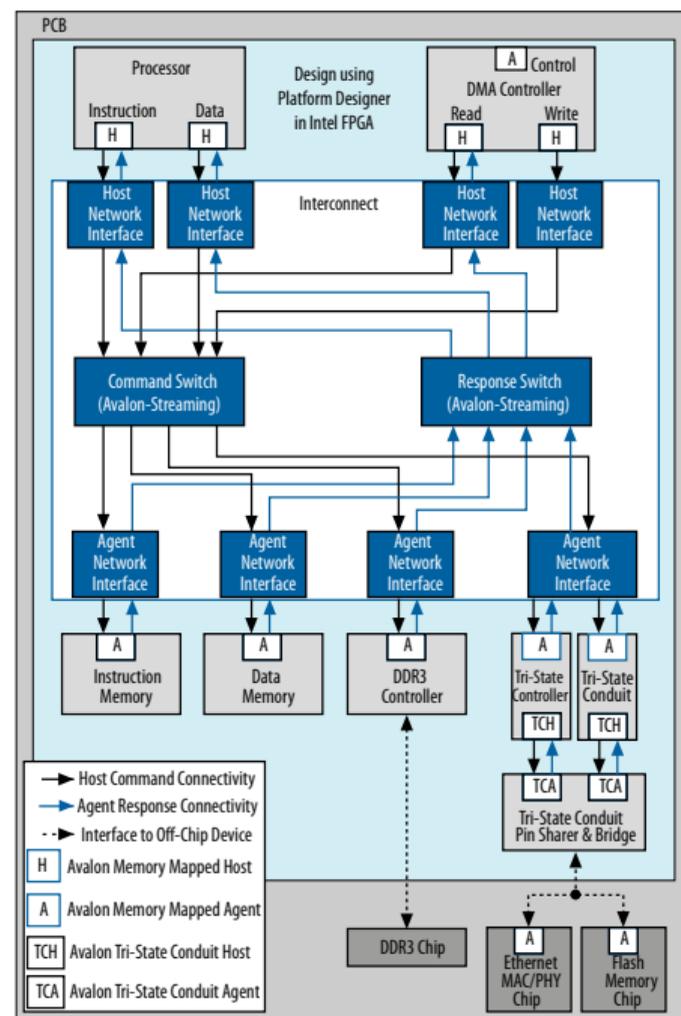
# IP Integration with Platform Designer

# Altera Platform Designer

Generates the interconnect logic for connecting a mix of IP Cores with **Avalon/AXI/APB/ACE** interfaces

You specify the components and their connections and Platform Designer generates the Verilog for it all

Formerly "Qsys"



# Platform Designer

Platform Designer - soc\_system.qsys (/mnt/sedwards/svn/classes/2025/4840-spring/labs/lab3-hw/soc\_system.qsys)

File Edit System Generate View Tools Help

IP Catalog System Contents Address Map Interconnect Requirements

System: soc\_system Path: clk\_0

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>		<b>clk_0</b> clk_in clk_in_reset clk clk_reset	Clock Source Clock Input Reset Input Clock Output Reset Output	clk reset <i>Double-click to</i> <i>Double-click to</i>	<i>exported</i> clk_0			
<input checked="" type="checkbox"/>		<b>hps_0</b> h2f_user1_clock memory hps_io h2f_reset h2f_axi_clock h2f_axi_master f2h_axi_clock f2h_axi_slave h2f_lw_axi_clock h2f_lw_axi_master f2h_irq0 f2h_irq1	Arria V/Cyclone V Hard Proce... Clock Output Conduit Conduit Reset Output Clock Input AXI Master Clock Input AXI Slave Clock Input AXI Master Interrupt Receiver Interrupt Receiver	<i>Double-click to</i> <b>hps_ddr3</b> <b>hps</b> <i>Double-click to</i> <i>Double-click to</i> <i>Double-click to</i> <i>Double-click to</i> <i>Double-click to</i> <i>Double-click to</i> <i>Double-click to</i> <i>Double-click to</i>	hps_0_h2...    clk_0 [h2f_axi_... clk_0 [f2h_axi_... clk_0 [h2f_lw_a...			IRQ 0 IRQ 31

Hierarc Device Far

soc\_system [soc\_system.qsys]

- clk
- hps
- hps\_ddr3
- reset
- clk\_0
- hps\_0
- Connections

Current filter:

Messages

Type	Path	Message
Warning	2 Warnings	
Warning	soc_system.hps_0	"Configuration/HPS-to-FPGA user 0 clock frequency" (desired_cfg_clk_mhz) requested 100.0 MHz, but only achieve
Warning	soc_system.hps_0	1 or more output clock frequencies cannot be achieved precisely, consider revising desired output clock frequencies.
Info	2 Info Messages	

0 Errors, 2 Warnings

Generate HDL... Finish

# Bus Bridges

# Bus Bridges

A bus bridge connects two, often different, buses.

Enables multiple clock domains, different protocols (e.g., AXI ↔ Avalon), bus widths, etc.

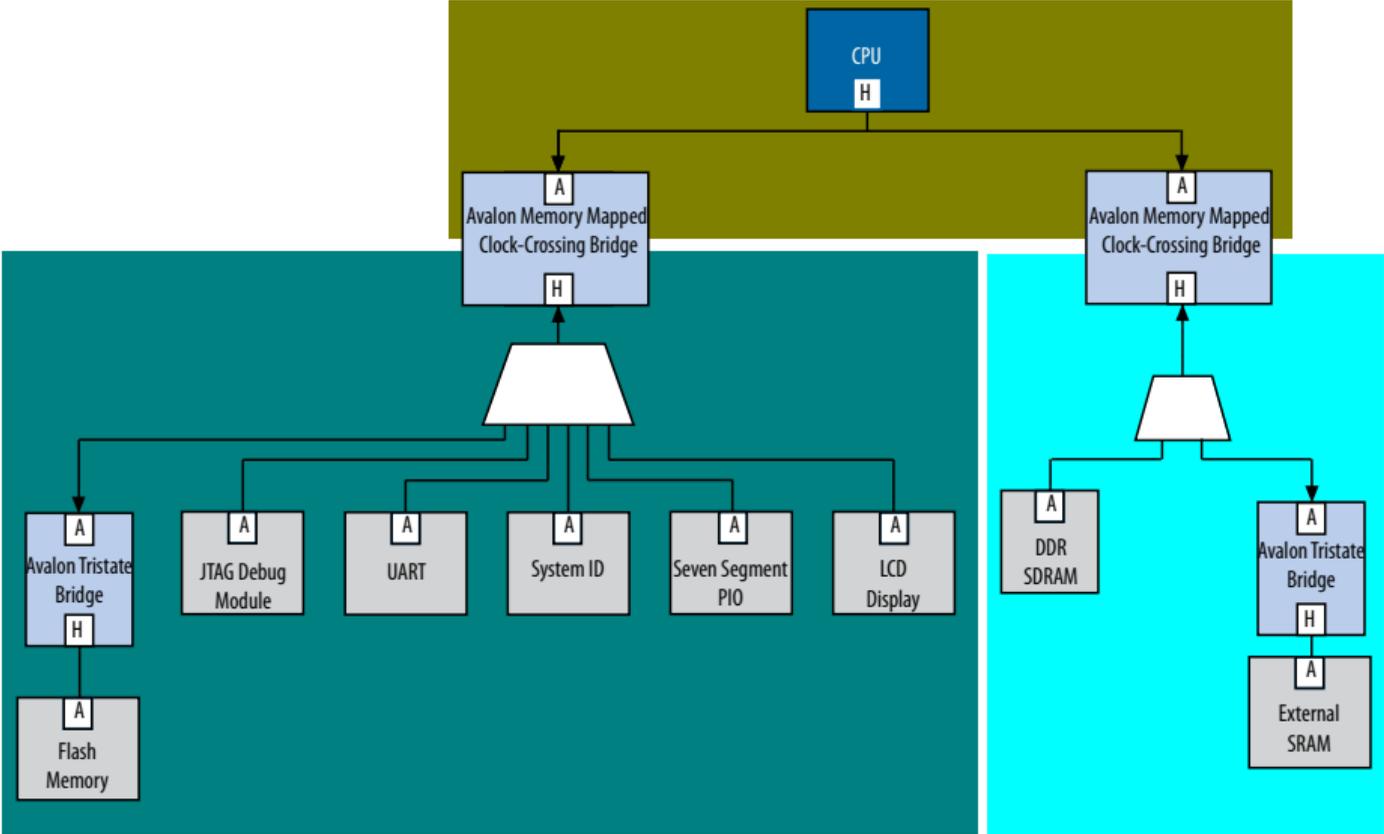
## **Example Bridge Types:**

SOC HPS ↔ FPGA Bridge

Avalon MM Clock Crossing Bridge

Avalon MM Pipeline Bridge

# Clock Crossing Bridge Example



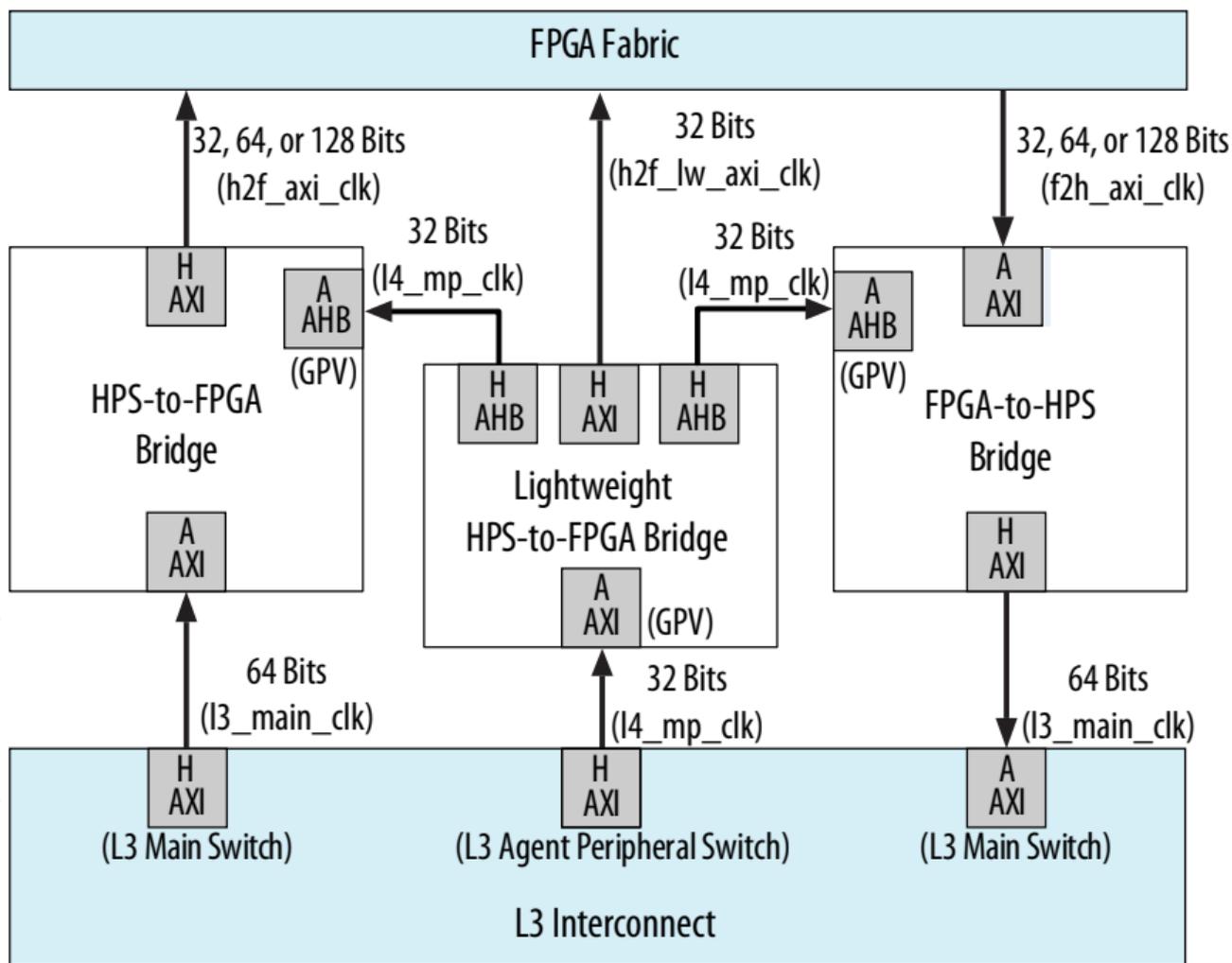
**H** Avalon Memory Mapped Host Port  
**A** Avalon Memory Mapped Agent Port

# Cyclone V HPS-FPGA Bridges

32-bit  
lightweight for  
configuration

32/64/128 high-  
performance  
FPGA agents

32/64/128 high-  
performance  
FPGA hosts



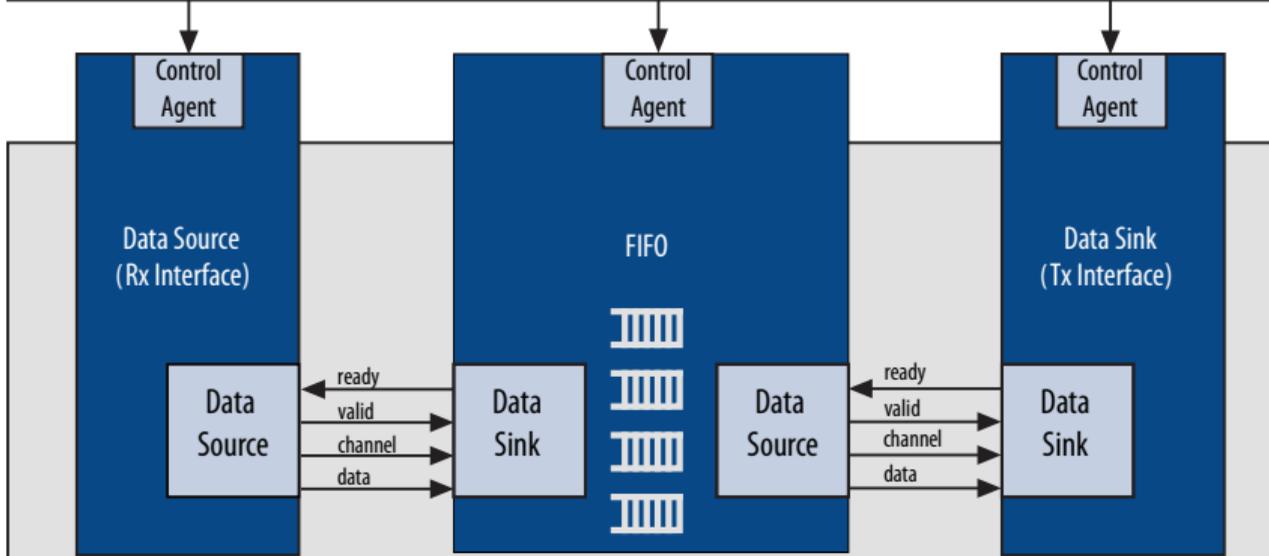
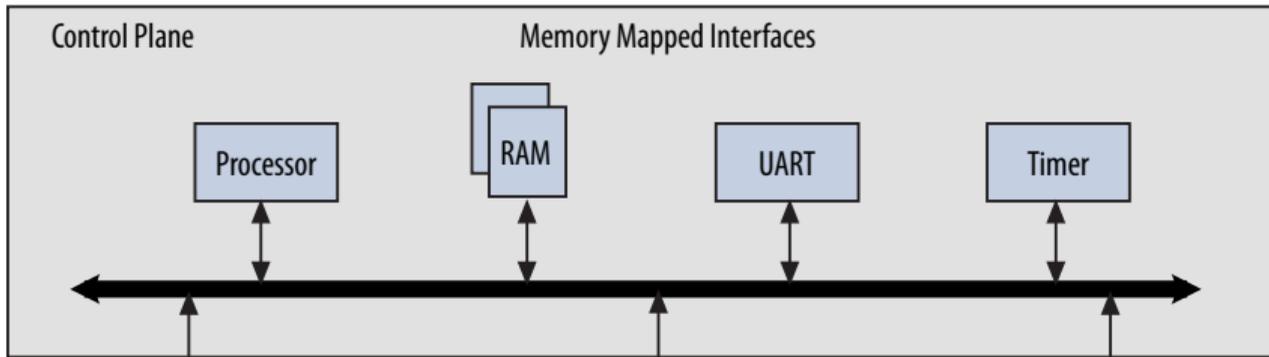
# Control and Data Planes

## Control vs. Data Planes

**Control Plane:** Memory mapped registers typically used for configuring devices, querying status, initiating transactions, etc (low bandwidth)

**Data Plane:** Streaming directed graphs for actually moving and processing large amounts of data (audio/video, network packets, etc); high bandwidth

A single IP core can have both MM and ST interfaces (including multiple of each).



Data Plane

Avalon Streaming Interface

Source: Altera Platform Designer User Guide

# References to Altera Documentation

## Cyclone V Device Handbook: Volume 1: Device Interfaces and Integration

<https://docs.altera.com/r/docs/683375/current/cyclone-v-device-handbook-volume-1-device-interfaces-and-integration/logic-array-blocks-and-adaptive-logic-modules-in-cyclone-v-devices>

## Cyclone V Hard Processor System Technical Reference Manual

<https://docs.altera.com/r/docs/683126/21.2/cyclone-v-hard-processor-system-technical-reference-manual/cyclone-v-hard-processor-system-technical-reference-manual-revision-history>

## Quartus Prime Standard Edition User Guide: Platform Designer

<https://docs.altera.com/r/docs/683364/18.1/intel-quartus-prime-standard-edition-user-guide-platform-designer/creating-a-system-with-platform-designer>