Nortsam

NumberOneRealTimeSpectrumAnalyzerMAX

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1. Project Overview

The purpose of this project was to create a 31-band Audio Spectrum Analyzer. A real time audio spectrum analyzer (sometimes called an RTA) is an invaluable tool for any audiophile. The ability to visualize the relative amplitude of discrete frequency ranges affords an objective measure by which to fine-tune a hi-fi audio system. Audio Spectrum Analyzers are also very common in commercial applications for the visualization of audio signals.

Nortsam uses the SpartanIIE FPGA on the XSB-300E Board with the on-board audio and video peripherals. The on-board audio input accepts an external analog stereo line-level signal through the 1/8" mini jack. The signal undergoes Analog-to-Digital conversion with the assistance of the on-board AK4565 (audio codec). A Fast Fourier Transform is applied in order to appropriately isolate independent ranges in the frequency domain. The results of the FFT are pipelined into a graphics visualization function and then sent to the video hardware to produce a proper visualization. The end result is a dynamic VGA bar graph style display.

The FPGA itself is used to implement the computations of the stereo FFT, and video frame buffer hardware. The display output consists of 31 discrete bands, each ranging 1/3 octave. Each band corresponds to a third octave segment on the range from 20 Hz to 20 KHz.

2. Project Design

2.1. The Hopeful

To achieve our goal, a suitable design plan was constructed. In our original Project Proposal, audio signal from the audio source is fed to the stereo-in port, where it is processed by the audio codec. Once processed, the sampled audio data is buffered by the FPGA and sent to the Fast Fourier Transform (FFT) for further processing. In the meantime, a second buffer is filling with new audio data to be processed by the FFT upon completion of the previous data.

The determination on how to process the audio required much background research. First, a simple Fast Fourier Transform (FFT) with 32 bins was thought to be sufficient. Unfortunately, since our desired bands are based on an exponential scale (the 1/3 octave scale), and FFT precision needs to be higher in order for the lower frequencies to be distinctive, it turned out that many more FFT bins would be needed. The implications are, even if a moderately large FFT were used, of size 512, each component of the FFT result (FFT bins), of which there are 256 due to mirroring in the frequency domain, would correspond to roughly 100 Hz, causing the first 7 frequency bands to be calculated from a single FFT result bin. Conversely, the final band would have about 40 bins associated with its' range.

To solve this problem, a staged approach was decided upon. Instead of calculating all the bands in one FFT, band segments could be calculated separately. It is known that the audio codec samples at the rate of 48 kHz. If a FFT of size 256 is used, the bottom 128 bins would be related to the positive frequency range of 0 to 24 kHz, or half the sampling rate. Knowing the center frequency for each of the bands, it was found that the accuracy of the FFT would only be suitable for approximately the top

12 bands. At the thirteenth band, less than one bin separates each band from the previous, resulting in increasing inaccuracy. This would be the cutoff point where a new FFT would begin, which contains only the nineteenth (1.25kHz band, thirteenth from top) band and below.

To reach the second FFT, two signal processing steps are needed. First, to avoid the effects of the higher frequencies, the samples would have to be filtered. The new sampling rate needs to be at least twice as high as the highest frequency sampled (Nyquist Sampling rate) to avoid aliasing. This would cause the frequency range of the new FFT to be from only 0 to 3 kHz. A second order Infinite Impulse Response Filter was designed for this purpose. Secondly, the samples would have to be downsampled, or decimated, after the filter to achieve the 3 kHz range. This translates into a 16x down-sample of the incoming samples at 48 kHz. For a 256 bin FFT, 4096 samples would be needed.

The range from 0 to 3 kHz only gives suitable accuracy down until about the 125 Hz center frequency, at about 12 Hz per bin. Although this leaves the 8 lower bands still inaccurate, any additional down-sampling would increase the number of samples needed to unacceptable limits. For example, to have more than one bin separating 20 Hz from 25 Hz, 128x downsample is needed, which mean 32768 samples are needed. At this rate it would take close to a second for there to be enough data to even begin calculating the audio spectrum.

Once all the necessary bins are calculated, a suitable average will be made for each band according to the appropriate bins, and the results will be displayed on the screen. For the display, previous lab setups will help in achieving the correct timing to display images.

2.2. The Actual

As can be found in many cases, the boundary between the theoretical and the attainable can be difficult to cross. Many design choices gave way to more practical and attainable goals. Our preliminary design was composed largely of hardware blocks which would do the majority of the signal processing, leaving the software end solely for the visualization aspects. Our design plan quickly changed when we realized the magnitude and complexity of work needed in such an elaborate hardware design. As an alternative, we chose to perform the majority of the control aspects in signal processing with the Microblaze processor, using hardware only for the most computationally expensive tasks. The software approach yielded to a much simpler interface with the SRAM, so those design aspects were avoided in hardware. Additionally, the software helped to keep track of the large sample buffers, and to group the resulting data.

Unfortunately, one of the more disappointing gaps between the optimistic and actual was the modular decomposition of the FFT. Even though all the necessary operations were decided upon for the filter and down-sampling, the task of getting a working FFT outweighed the further design option of using a filtering process. To compensate for the loss in accuracy, an FFT of size 2048 is used. Even so, lower bars have less accuracy. Even given additional time, the implementation of the filter would have been difficult, since the project was rapidly approaching its' limits: time constraint limit and the memory area limit.

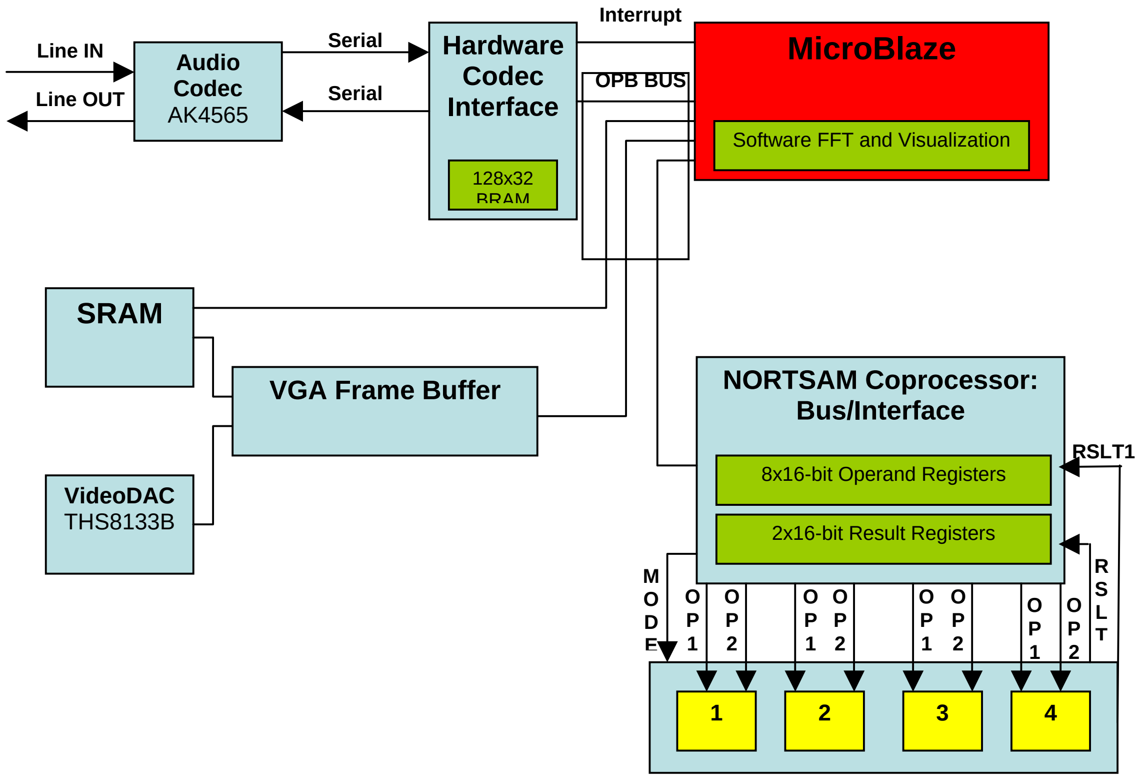
With the 2048 size FFT, there was still slight overlap between the lower frequency bands. Since the lower bars relate to such few bins, and in two cases the same bins, in the final result we changed the corresponding frequency ranges for the lower bands from the logarithmic scale in order to ensure distinctness in the visualization. The following table summarize the frequency ranges for the corresponding bin number:

Band	Corresponding FFT Bin(s)	Frequency Range (Hz)
0	0	0
1	1	0-23
2	2	23-70
3	3	70-93
4	4	93-117
5	6	117-140
6	7	140-164
7	8	164-187
8	9	187-210
9	10	210-234
10	11	234-257
11	12-13	257-304
12	14-16	304-375
13	17-20	375-468
14	21-25	468-585
15	26-31	585-726
16	32-39	726-914
17	40-49	914-1148
18	50-61	1148-1429
19	62-77	1429-1804
20	78-97	1804-2273
21	98-122	2273-2859
22	123-153	2895-3585
23	154-194	3585-4546
24	195-244	4546-5718
25	245-306	5718-7171
26	307-387	7171-9070
27	388-487	9070-11414
28	488-612	11414-14344
29	613-773	14344-18117
30	774-973	18177-22805

For every 2048 samples collected, 1216 samples are dropped while waiting for a free buffer from the FFT.

3. Design Components

3.1. Hardware Block Diagram



3.2. Hardware Description

a. Audio Codec Interface

The codec interface hardware generates three clock signals: master (12.5MHz), serial (1.5625MHz), and frame (48.828kHz). The AK4565 codec chip outputs a serial bitstream of sample data, synchronized to these clocks. The sample bitsteam is fed bit-by-bit into a BRAM module. Once 64 stereo samples have been collected (16 bits per sample-channel), the interface generates an Interrupt signal and swaps BRAM buffers to continue collecting samples.

The interface is memory-mapped to base address 0xFEFE0000 on the OPB bus. When a write is performed from software (in support of audio output), the interface prefetches the incoming sample at the corresponding address. A 32-bit value is returned upon the next read to the interface's address space, representing one stereo amplitude sample at $\Delta t=(1/48.828khz)$.

The interface was implemented in VHDL by Christian Soviani, with minor modifications made by us to scale input data and configure the output as a 'thru' jack.

b. Nortsam Coprocessor

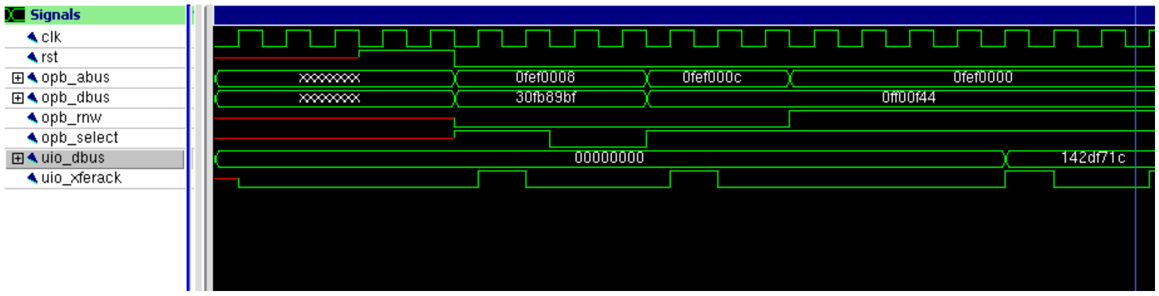
The Nortsam Coprocessor could also be known as the DSP Workhorse. The upper level module controls the interface aspects of communication through the OPB with the software level, as well as latching the appropriate values according to the function need, for further calculations in the sub-modules. The second level down controls the handshaking needed to interface with the computational units, as well as formatting the data appropriately for the upper level to receive. Once the calculations have been made, the second level sends the results, along with a done signal.

Inside the second state, there are four identical special purpose functional units, which can be assigned one of two modes. The first mode is a fixed point multiply which multiplies a signed 16 bit vector, formatted in any particular matter, and another signed 16 bit vector, with all 16 bits to the right of the binary point. The returned result is a 16 bit vector, with the same format as the first input. This function is especially important when data inside the FFT must be multiplies by a fixed coefficient which ranges from -1 to 1. The second mode takes two 16 bit signed vectors, with the same binary point, and returns a 16 bit signed value which represents their multiple. The binary point lies at whichever point that is twice as much over on the right as it is in the input format. This mode is important for the magnitude calculation necessary at the end of the butterfly output in the FFT. Although the output is signed, a 16 bit unsigned output is returned when calculating the magnitude. In both these modes, some precision is lost, since a potential 31 bit result is packed into 16 bits, but the overall loss is not significant enough to effect the values later on, since all the most significant bits are kept.

One important function the middle state handles is retrieving the result from these four sub-modules, and formatting the result appropriately. For the magnitude calculation this is fairly simple, since the module need only take two of the output and send them as output, with the first result being the real part of the magnitude calculation, and the second result being the imaginary part of the calculation. The actually summing of these results is handled in software, where saturation is additionally considered. For the data and coefficient multiplies, the job of this module is a bit more complex, effectively performing a complex multiply. The result of the real calculation is sent on result A, and the imaginary is sent on result B.

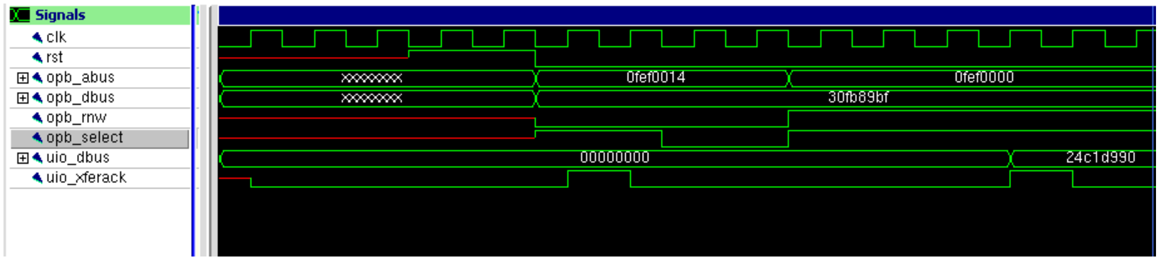
The communication scheme of the Coprocessor with the Microblaze follows the standard OPB protocol with perfecting of the results. This means that once data is written to the Coprocessor, it latches the return data even before the Microblaze requests it. This avoids some delay inherent in the reading data process, allowing the result to be returned in fewer clock cycles.

When the first mode is needed, the OPB_ABus upper bits correspond to the upper bit mask of the Coprocessor (0x0FEF), and the lower eight bits have the address 0x08. Since two 32 bit writes are needed to have enough data for a complex multiply, the Coprocessor has to wait for an additional write by the Microblaze to address 0x0c before it allows the computations to take place. This order in written addresses is fixed. If 0x0c is written first, the submodule will just use the previous value written on 0x08, so the software must keep to this ordered convention. Once both addresses are written, the submodules compute the result, and send a ready signal to the upper module to let it know to latch the result. Once the Microblaze request a read to the base address, the module passes the result on the UIO_DBus, regardless of the lower bits of the address sent by the Microblaze. Below is a sample timing diagram of the communication process across the OPB.



As can be seen, the result is latched to the output only seven cycles after the second write is acknowledged. In previous versions of the multiplier, only four cycles were needed, but due to timing delay constraints, the pipeline had to be widened. Even with the additional cycles needed to communicate between the software and hardware interfaces, this is a vast improvement of the alternative, where the multiplies would be performed in software.

The second mode follows many of the same conventions as the first mode. The one main difference is only one write is needed to begin computations. As long as the first write is to an address with the bottom eight bits of 0x14, the second mode will run. The result is prefetch, and latched to the UIO_DBus once a read is requested of the appropriate base address, regardless of the lower bits of the address. The timing diagram is below.



The amount of time taken for computation is seven cycles, which is the same as mode one. This is because mode one and mode two share the same functional units and data path in order to reduce area.

3.3. *Software Description*

a. The FFT

The Fast Fourier Transform (FFT) is a Discrete Fourier Transform (DFT) algorithm which reduces the number of computations needed for N points from N^2 to N(*Log*N). The idea behind the FFT is the *divide and conquer* approach, to break up the original N point sample into two N/2 sequences. A series of smaller problems is easier to solve than one large one. The normal DFT requires $(N-1)^2$ complex multiplications and N(N-1) complex additions as opposed to the FFT's approach of breaking it down into a series of 2 point samples which only require 1 multiplication and 2 additions and the recombination of the points which is minimal.[1]

The format of the FFT written for the MicroBlaze comes from Numerical Recipes in C[2], with some changes to make it better suited for a join software/hardware interface. After loading the 2048 audio samples from the audio codec into an array of 4096 (to represent real and imaginary values) the array is passed to the FFT function for computation. The FFT modifies the array during computation, ultimately returning the same array propagated with the correct real and imaginary results.

One of the major changes made from the traditional C FFT was moving all the multiplications to hardware, resulting in fewer writes and reads (two writes and one read) for complex multiplies. The other major change was pre-computing the coefficients used during the FFT calculation. Calculating the coefficients and storing them in memory prevented avoided the costly repetitive computations made in the original FFT.

b. Magnitude Calculation

Once the FFT propagates the array with the real and imaginary frequency representation of the original signal, the magnitude must be computed for each resulting bin. For this, the software writes a 32 bit value, which contains the real and imaginary values, to the hardware, which then calculates the square of each value and returns them after a 32 bit read is made. The software then adds these values together to get the square of the magnitude, accounting for any saturation that

[1] http://www.spd.eee.strath.ac.uk/~interact/fourier/fft/fftideas.html#whyFFT
[2] Numerical Recipes in C: The Art Of Scientific Computing, Cambridge University Press., 1992

might occur by having the result being greater than 16 bits.

c. Visualization

Due to the nature of the octave scale, the higher frequency bands correspond to more FFT bins than the lower frequency bands. The NORTSAM product has an array of the corresponding FFT bins for each frequency band. The max value for each FFT bin is used for the band's magnitude display to the screen. For the lower frequency bands, where there is only one FFT bin corresponding to the magnitude, the one bin was used as the magnitude.

As mentioned in the magnitude section above, the result returned from the magnitude function is a 32 bit result of the summed squared values of the real and imaginary parts of the FFT results. To bypass using a computationally complex square root calculation, the square root was compensated for in the visualization.

There are 31 frequency bands according to our design specs. Each band can has 182 vertical points of precision corresponding to max value of 33124. There is a constant array storing 0 to 33124 (182 squared). A binary search was implemented to find the best approximation within this array for the square root of the number searched for. The resultant index in the squared array is the approximate magnitude of the queried value.

The magnitude, bin number, and stereo component (left or right) are all passed to the drawBar method, drawing the bar to the screen. The method uses the above listed parameters to calculate the VGA memory location to write to. The color of each component of the bar is calculated on the distance away from the 0 bar, providing the white to red color effect.

A history is kept for each of the frequency bars to smooth the visualization. This method can be commented out to demonstrate the jerky and instantaneous response of the FFT to the audio input. With a linear decrement in bars, the display is more visually enjoyable and similar to competing commercial products.

In combination with the history for each bar, a max was computed for aesthetics. The placement of this bar was calculated in a similar manner to the magnitude bar.

4. <u>Benchmarks</u>

-With hardware, with stereo visualization, 2 FFT's of size 2048 – 500 iterations

First Trial	-	38.7099838sec
Second Trial	-	38.6399570sec
Average	-	77ms per iteration = 12.92 iterations per second

-Stereo FFTs without video, in hardware, with interrupts – 500 iterations

First	-	26.99987
Second	-	27.00011
Average	-	54ms per iteration = 18.5 iterations per second

-Stereo FFTs without video, in hardware, with interrupts disabled – 500 iterations

First	-	26.009817
Second	-	25.999864
Average	-	52ms per iteration = 19.2 iterations per second

5. Work Distribution

5.1. Joshua Mackler

a. **Fixed Point Multiplier in Hardware**

b. **Magnitude Calculator in Hardware**

c. **Coefficient Generation for FFT**

5.2. Tecuan Flores

a. **Implementation of initial FFT in software**

b. **Visualization Graphics**

5.3. Philip Coakley

a. **Audio input with Audio Codec**

b. **Hardware/Software bus interfaces**

c. **Final implementation of FFT with Hardware interaction**

6. Future Advice

As with any project, it is important to start planning the project early and set up a timeline of deliverables and milestones. Once again, we learned this the hard way ☺. Project planning is extremely important as implementation time is directly dependent on the thoroughness of the planning.

It is also important to distribute the work amongst the team members. Delegation of responsibilities early in the project life reduces dead time and duplication of work. Nortsam can attribute its success to the efficient distribution of the work that was later compiled to construct the final project.

7. VHDL Code

7.1. NORTSAM Coprocessor

a. Nortsam Bus Interface - *opb_xsb300_nortsam.vhd*

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;

--library UNISIM;
--use UNISIM.VComponents.all;

entity opb_xsb300_nortsam is
  generic (
    C_OPB_AWIDTH    : integer := 32;
    C_OPB_DWIDTH    : integer := 32;
    C_BASEADDR      : std_logic_vector(31 downto 0) := X"0FEF_0000";
    C_HIGHADDR      : std_logic_vector(31 downto 0) := X"0FEF_FFFF"
    );

    Port (
      OPB_Clk : in std_logic;
      OPB_Rst : in std_logic;
      OPB_ABus : in std_logic_vector (31 downto 0);
      OPB_BE : in std_logic_vector (3 downto 0);
      OPB_DBus : in std_logic_vector (31 downto 0);
      OPB_RNW : in std_logic;
      OPB_select : in std_logic;
      OPB_seqAddr : in std_logic;

      UIO_DBus : out std_logic_vector (31 downto 0);
      UIO_errAck : out std_logic;
      UIO_retry : out std_logic;
      UIO_toutSup : out std_logic;
      UIO_xferAck : out std_logic;
      Interrupt : out std_logic
      );
end opb_xsb300_nortsam;

architecture Behavioral of opb_xsb300_nortsam is

component nortsam_coprocessor
  port      (
    CLK : in std_logic;
    RST : in std_logic;
    done : out std_logic;
    interrupt : out std_logic;
    rdy : in std_logic;
    mode : in std_logic_vector(1 downto 0);
    rA, rB, rC, rD, rE, rF, rG, rH : in std_logic_vector(15 downto 0);
    resultA, resultB : out std_logic_vector(15 downto 0)
    );
end component;
```

```
signal cs,cs_1, xfer, xfer_1, xfer_2 : std_logic;

signal rnw : std_logic;
signal addr : std_logic_vector (15 downto 0);
signal wdata : std_logic_vector (31 downto 0);

signal rdata : std_logic_vector (31 downto 0);
signal opb_ad_ce : std_logic;

signal we : std_logic;

signal rA, rB, rC, rD, rE, rF, rG, rH : std_logic_vector(15 downto 0);
signal resA, resB : std_logic_vector(15 downto 0);
signal res_rdy : std_logic;
signal res_rdy_1 : std_logic := '0';
signal rdy : std_logic := '0';
signal mode : std_logic_vector(1 downto 0) := "00";
begin

process(OPB_Rst, OPB_Clk)
begin

-- register adresses, data write, rnw
   if OPB_Rst = '1' then
          addr <=  X"0000";
          wdata <= X"0000_0000";
          rnw <= '0';
      elsif OPB_Clk'event and OPB_Clk ='1' then
          if opb_ad_ce = '1' then
                         wdata <= OPB_DBus;
                         addr <= OPB_ABus(15 downto 0);
                                 rnw <= OPB_RNW;
                   end if;
      end if;

-- register data read
   if OPB_Rst = '1' then
                  rdata <= X"0000_0000";
      elsif OPB_Clk'event and OPB_Clk ='1' then
                   if res_rdy  = '1' then
                           rdata(31 downto 16) <= resA;
                           rdata(15 downto 0) <= resB;
                        end if;

      end if;

end process;

-- very important
-- TO DO
-- when writing, the read data can corrupt the DBus
UIO_DBus <= rdata when (xfer or xfer_1 or xfer_2) = '1' and rnw = '1'
else X"0000_0000";

cs <= OPB_Select when OPB_ABus(31 downto 16)=X"0FEF" else '0';
```

```
-- combinational logic for BRAM
we <= (xfer or xfer_1) and not rnw;


opb_ad_ce <= not xfer;

mode <= "01" when OPB_ABus(7 downto 0) = X"14" else "00" when
OPB_ABus(7 downto 0) = X"08" or OPB_ABus(7 downto 0) = X"0C";

-- the 1st ff -- FDR
process(OPB_Clk)
begin
      if OPB_Clk'event and OPB_Clk ='1' then

          if (xfer or xfer_1) = '1' then xfer <='0';
                elsif OPB_RNW = '0' then
                  xfer <= cs;
                else
                  xfer <= res_rdy and cs;
                end if;

      end if;
end process;

process (OPB_Rst, OPB_Clk)
begin
      if OPB_Rst = '1' then
                 xfer_1 <= '0';
                 xfer_2 <= '0';
                 cs_1 <= '0';
        elsif OPB_Clk'event and OPB_Clk ='1' then
             xfer_1 <= xfer;
             xfer_2 <= xfer_1;
                 cs_1 <= cs;
        end if;
end process;

-- write to registers
process (OPB_Rst, OPB_Clk)
begin
  if OPB_Rst = '1' then
    rA <= "0000000000000000";
    rB <= "0000000000000000";
    rC <= "0000000000000000";
    rD <= "0000000000000000";
    rE <= "0000000000000000";
    rF <= "0000000000000000";
    rG <= "0000000000000000";
    rH <= "0000000000000000";
  elsif OPB_Clk'event and OPB_Clk='1' then
    if rdy = '1' then
      rdy <= '0';
    end if;
    if (xfer and we) = '1' then

      case addr(7 downto 0) is
        when X"08" =>
```

```
          -- FFT: writing Jr & Ji
          rA <= wdata(31 downto 16);
          rE <= wdata(31 downto 16);
          rC <= wdata(15 downto 0);
          rG <= wdata(15 downto 0);
         -- mode <= "00";
        when X"0C" =>
          -- FFT: writing Cr & Ci
          rB <= wdata(31 downto 16);
          rH <= wdata(31 downto 16);
          rD <= wdata(15 downto 0);
          rF <= wdata(15 downto 0);
          rdy <= '1';
        when X"14" =>
          rA <= wdata(31 downto 16);
          rB <= wdata(31 downto 16);
          rC <= wdata(15 downto 0);
          rD <= wdata(15 downto 0);
          rdy <= '1';
          -- mode <= "01";
        when others => null;
      end case;
    end if;
  end if;
end process;

--rdy <= all4 when mode = "00" else '1' when mode = "01" else '0';

-- tie unused to ground
UIO_errAck <= '0';
UIO_retry <= '0';
UIO_toutSup <= '0';
UIO_xferAck <= xfer;

nortsam : nortsam_coprocessor port map(
      CLK => OPB_Clk,
        RST => OPB_Rst,
        mode => mode,
      interrupt => interrupt,
        rdy => rdy,
        rA => rA,
        rB => rB,
        rC => rC,
        rD => rD,
        rE => rE,
        rF => rF,
        rG => rG,
        rH => rH,

        resultA => resA,
        resultB => resB,
        done => res_rdy
);

end Behavioral;
```

b. Nortsam Coprocessor – nortsam_coprocessor.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

--library UNISIM;
--use UNISIM.VComponents.all;


entity nortsam_coprocessor is
  port      (
    CLK : in std_logic;
    RST : in std_logic;

    interrupt : out std_logic;
    rdy : in std_logic;
    mode : in std_logic_vector(1 downto 0);
    rA, rB, rC, rD, rE, rF, rG, rH : in std_logic_vector(15 downto 0);
    resultA, resultB : out std_logic_vector(15 downto 0);

    done : out std_logic

    );
end nortsam_coprocessor;


architecture Behavioral of nortsam_coprocessor is
component fixed_16x16_multi is
 port (
    data    : in  std_logic_vector(15 downto 0);
    coeff   : in  std_logic_vector(15 downto 0);
    rdy     : out std_logic;
    product : out std_logic_vector(15 downto 0);
    clk     : in std_logic;
    rst     : in std_logic;
    mode    : in std_logic_vector(1 downto 0));
end component;


signal resA, resB, resC, resD : std_logic_vector(15 downto 0);
signal done1 :std_logic := '0';
signal done2 :std_logic := '0';
signal done3 :std_logic := '0';
signal done4 :std_logic := '0';
signal not_mag : std_logic;
signal reel, im : std_logic_vector(15 downto 0);
signal re_rdy : std_logic := '0';
signal im_rdy : std_logic := '0';
begin

mul1 : fixed_16x16_multi port map(
  clk => CLK,
  data => rA,
  coeff => rB,
  rdy => done1,
  product => resA,
  rst => rdy,
  mode => mode
  );

mul2 : fixed_16x16_multi port map(
  clk => CLK,
  data => rC,
  coeff => rD,
  rdy => done2,
  product => resB,
  rst => rdy,
  mode => mode
  );


mul3 : fixed_16x16_multi port map(
  clk => CLK,
  data => rE,
  coeff => rF,
  rdy => done3,
  product => resC,
  rst => not_mag,
  mode => mode
  );

mul4 : fixed_16x16_multi port map(
  clk => CLK,
  data => rG,
  coeff => rH,
  rdy => done4,
  product => resD,
  rst => not_mag,
  mode => mode
  );



-- generate the 3 clocks: master, serial, frame

 process(CLK, RST)
 begin
   if clk'event and clk='1' then
     if rdy = '1' then
       im_rdy <= '0';
       re_rdy <= '0';
     else
       if (done1 and done2) = '1' and mode = "00" then
         reel <= resA - resB;
         re_rdy <= '1';
       elsif (done1 = '1' and mode ="01") then
         reel <= resA;
         re_rdy <= '1';
       end if;
       if (done3 and done4) = '1' and mode = "00" then
         im <= resC + resD;
         im_rdy <= '1';
       elsif (done2='1' and mode ="01") then
         im <= resB;
         im_rdy <= '1';
       end if;
     end if;
   end if;
 end process;

not_mag <= rdy when mode = "00" else '0';

interrupt <= '0';

resultA <= reel;
resultB <= im;

done <= im_rdy and re_rdy;

end Behavioral;
```

c. 16-bit Fixed Point Multiplier Module – *fixed_16x16_multi.vhd*

```
----------------------------------------------------------------------
--------
-- Fixed Point Multiplier
--
-- 16 bit data contains 9 bits to left of decimal and 7 to the right
-- 16 bit coeff contains all 16 bits to right of decimal
-- output has fixed point same as data
--
-- Josh Mackler
--
----------------------------------------------------------------------
--------



library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity fixed_16x16_multi is
  port (
    data    : in  std_logic_vector(15 downto 0);
    coeff   : in  std_logic_vector(15 downto 0);
    rdy     : out std_logic;
    product : out std_logic_vector(15 downto 0);
    clk     : in std_logic;
    rst     : in std_logic;
    mode    : in std_logic_vector(1 downto 0));

end fixed_16x16_multi;

architecture archy of fixed_16x16_multi is

  signal tmp : std_logic_vector(15 downto 0);  -- shift amt of data
  signal multip : std_logic_vector(15 downto 0) := X"0000";
  signal inter1 : std_logic_vector(15 downto 0);
  signal inter2 : std_logic_vector(15 downto 0);
  signal inter3 : std_logic_vector(15 downto 0);
  signal inter4 : std_logic_vector(15 downto 0);
  signal inter5 : std_logic_vector(15 downto 0);
  signal inter6 : std_logic_vector(15 downto 0);
  signal inter7 : std_logic_vector(15 downto 0);
  signal inter8 : std_logic_vector(15 downto 0);
  signal inter9 : std_logic_vector(15 downto 0);
  signal inter10 : std_logic_vector(15 downto 0);
  signal inter11 : std_logic_vector(15 downto 0);
  signal inter12 : std_logic_vector(15 downto 0);
  signal inter13 : std_logic_vector(15 downto 0);
  signal inter14 : std_logic_vector(15 downto 0);
  signal inter15 : std_logic_vector(15 downto 0);
  signal second1, second2, second3, second4, second5 :
std_logic_vector(15 downto 0);
  signal res1 : std_logic_vector(15 downto 0);
  signal res2 : std_logic_vector(15 downto 0);
  signal res3 : std_logic_vector(15 downto 0);
  signal res4 : std_logic_vector(15 downto 0);
  signal res5 : std_logic_vector(15 downto 0);
  signal res6 : std_logic_vector(15 downto 0);
  signal res7 : std_logic_vector(15 downto 0);
  signal twos_coeff : std_logic_vector(15 downto 0);
 -- signal fm_count : std_logic_vector(0 to 3) := "0000";
  signal mul_pipe : std_logic_vector(1 downto 0);
  signal negative : std_logic := '0';
  signal neg1 : std_logic := '0';
  signal neg2 : std_logic := '0';
  signal go : std_logic := '0';
  signal tmp2 : std_logic_vector(15 downto 0);
  signal ready : std_logic := '0';
begin  -- archy


   inter1 <= '0' & tmp(15 downto 1) when twos_coeff(14)='1' and
mode="00" else
             "0000000" & tmp(15 downto 7) when twos_coeff(7)='1' and
mode="01" else X"0000";

   inter2 <= "00" & tmp(15 downto 2) when twos_coeff(13)='1' and
mode="00" else
              "000000" & tmp(15 downto 7) & '0' when twos_coeff(8)='1'
             and mode = "01" else X"0000";

   inter3 <= "000" & tmp(15 downto 3) when twos_coeff(12)='1' and
mode="00" else
              "00000" & tmp(15 downto 7) & "00" when twos_coeff(9)='1'
             and mode = "01" else X"0000";

   inter4 <= "0000" &  tmp(15 downto 4) when twos_coeff(11)='1' and
mode="00" else
              "0000" & tmp(15 downto 7) & "000" when twos_coeff(10)='1'
and mode="01"
             else X"0000";

   inter5 <=  "00000" & tmp(15 downto 5) when twos_coeff(10)='1' and
mode="00" else
               "000" & tmp(15 downto 7) & "0000" when
twos_coeff(11)='1' and mode="01"
              else X"0000";

   inter6 <=  "000000" & tmp(15 downto 6) when twos_coeff(9)='1' and
mode="00" else
              "00" & tmp(15 downto 7) & "00000" when twos_coeff(12)='1'
and mode="01"
              else X"0000";

   inter7 <=  "0000000" & tmp(15 downto 7) when twos_coeff(8)='1' and
mode="00" else
```

```
               "0" & tmp(15 downto 7) & "000000" when
twos_coeff(13)='1' and mode="01"
              else X"0000";

  inter8 <=  "00000000" & tmp(15 downto 8) when twos_coeff(7)='1' and
mode="00" else
              tmp(15 downto 7) & "0000000" when twos_coeff(14)='1' and
mode="01"
             else X"0000";
   inter9 <=  "000000000" & tmp(15 downto 9) when twos_coeff(6)='1' and
mode="00" else X"0000";
   inter10 <=  "0000000000" & tmp(15 downto 10) when twos_coeff(5)='1'
and mode="00" else X"0000";
   inter11 <=  "00000000000" & tmp(15 downto 11) when twos_coeff(4)='1'
and mode="00" else X"0000";
   inter12 <=  "000000000000" & tmp(15 downto 12) when
twos_coeff(3)='1' and mode="00" else X"0000";
   inter13 <=  "0000000000000" & tmp(15 downto 13) when
twos_coeff(2)='1' and mode="00" else X"0000";
   inter14 <=  "00000000000000" & tmp(15 downto 14) when
twos_coeff(1)='1' and mode="00" else X"0000";
   inter15 <=  "000000000000000" & tmp(15) when twos_coeff(0)='1' and
mode="00" else X"0000";

  process (clk, rst)
  begin  -- process
    if clk'event and clk='1' then
      if rst = '1' then
        if data(15) = '1' then
          tmp <= not(data) + 1;
          neg1 <= '1';
        else tmp <= data;
             neg1 <= '0';
        end if;
        if coeff(15) = '1' then
          neg2 <= '1';
          twos_coeff <= not(coeff) + 1;
        else
          twos_coeff <= coeff;
          neg2 <= '0';
        end if;
        multip <= X"0000";
        mul_pipe <= "00";
        ready <= '0';
        go <= '1';
      else
        if go = '1' then
          if mul_pipe = "00" then
            res1 <= inter1 + inter2;
            res2 <= inter3 + inter4;
            res3 <= inter5 + inter6;
            res4 <= inter7 + inter8;

           res5 <= inter9 + inter10;
            res6 <= inter11 + inter12;
            res7 <= inter13 + inter14;
            mul_pipe <= "01";
          elsif mul_pipe = "01" then       -- second clock
            second1 <= res1 + res2 + res3 + res4;
            second2 <= res5 + res6 + res7 + inter15;
            mul_pipe <= "11";
          elsif mul_pipe = "11" then       -- third clock
              if negative = '1' then product <= not(second1 + second2)
+ 1;
            else
              product <= second1 + second2;
            end if;
            go <= '0';
              ready <= '1';
          end if;
        end if;


      end if;
    end if;
  end process;

   rdy <= ready;
   negative <= neg1 xor neg2;
end archy;
```

7.2. AK4565 Audio Codec Interface

a. Bus Interface – opb_xsb300_ak4565.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;


library UNISIM;

use UNISIM.VComponents.all;


entity opb_xsb300_ak4565 is
  generic (
    C_OPB_AWIDTH    : integer := 32;
    C_OPB_DWIDTH    : integer := 32;
    C_BASEADDR      : std_logic_vector(31 downto 0) := X"FEFE_0000";
    C_HIGHADDR      : std_logic_vector(31 downto 0) := X"FEFE_FFFF"
    );

    Port (  OPB_Clk : in std_logic;
                      OPB_Rst : in std_logic;
                      OPB_ABus : in std_logic_vector (31 downto 0);
                      OPB_BE : in std_logic_vector (3 downto 0);
                      OPB_DBus : in std_logic_vector (31 downto 0);
                      OPB_RNW : in std_logic;
                      OPB_select : in std_logic;
                      OPB_seqAddr : in std_logic;

                      UIO_DBus : out std_logic_vector (31 downto 0);
                      UIO_errAck : out std_logic;
                      UIO_retry : out std_logic;
                      UIO_toutSup : out std_logic;
                      UIO_xferAck : out std_logic;


                      Interrupt : out std_logic;


            AU_CSN_N : out std_logic;
            AU_BCLK : out std_logic;
            AU_MCLK : out std_logic;
            AU_LRCK : out std_logic;
            AU_SDTI : out std_logic;
            AU_SDTO0 : in std_logic
                     );
end opb_xsb300_ak4565;

architecture Behavioral of opb_xsb300_ak4565 is


component audio_ak4565 port   (
         CLK : in std_logic;

            RST : in std_logic;


            audio_bram_clk : out std_logic;

            audio_bram_addr_dac : out std_logic_vector(11 downto 0);

            audio_bram_addr_adc : out std_logic_vector(11 downto 0);


            audio_bram_dacdata : in std_logic;

            audio_bram_adcdata : out std_logic;


            interrupt : out std_logic;

            audio_fifohalf : out std_logic;


            AU_CSN_N : out std_logic;
      AU_BCLK : out std_logic;
      AU_MCLK : out std_logic;
      AU_LRCK : out std_logic;
      AU_SDTI : out std_logic;
      AU_SDTO0 : in std_logic
        );


end component;

signal cs, xfer, xfer_1, xfer_2 : std_logic;

signal rnw : std_logic;
signal addr : std_logic_vector (15 downto 0);
signal wdata : std_logic_vector (31 downto 0);


signal rdata : std_logic_vector (31 downto 0);
signal opb_ad_ce : std_logic;



signal we, a0, ce0, ce1 : std_logic;

signal bram_rdata, bram_wdata : std_logic_vector(15 downto 0); -- as
the CPU sees them

signal bram_rdata_rev, bram_wdata_rev : std_logic_vector(15 downto 0);
-- reversed !
```

```
signal bram_addr : std_logic_vector(7 downto 0);



signal audio_bram_clk : std_logic;

signal audio_bram_addr_dac, audio_bram_addr_adc : std_logic_vector(11
downto 0);

signal audio_bram_dacdata : std_logic;

signal audio_bram_adcdata : std_logic;

signal audio_bram_dacdata_v : std_logic_vector(0 downto 0);

signal audio_bram_adcdata_v : std_logic_vector(0 downto 0);



signal audio_fifohalf : std_logic;


begin

process(OPB_Rst, OPB_Clk)
begin

-- register adresses, data write, rnw
   if OPB_Rst = '1' then
          addr <=  X"0000";
          wdata <= X"0000_0000";
          rnw <= '0';
      elsif OPB_Clk'event and OPB_Clk ='1' then
          if opb_ad_ce = '1' then

                         wdata <= OPB_DBus;

                         addr <= OPB_ABus(15 downto 0);
             rnw <= OPB_RNW;

                   end if;
      end if;


-- register data read

   if OPB_Rst = '1' then

                  rdata <= X"0000_0000";
      elsif OPB_Clk'event and OPB_Clk ='1' then

                   if(ce0='1') then rdata(15 downto 0) <= bram_rdata;
end if;

                   if(ce1='1') then rdata(31 downto 16) <= bram_rdata;
end if;
      end if;
end process;


-- very important

-- TO DO

-- when writing, the read data can corrupe the DBus

      UIO_DBus <= rdata when xfer = '1' else X"0000_0000";




cs <= OPB_Select when OPB_ABus(31 downto 16)=X"FEFE" else '0';



-- the 1st ff -- FDR

process(OPB_Clk)

begin

      if OPB_Clk'event and OPB_Clk ='1' then

            if (xfer or xfer_1) = '1' then xfer <='0'; else xfer <= cs;
end if;

      end if;

end process;



process (OPB_Rst, OPB_Clk)

begin

      if OPB_Rst = '1' then
       xfer_1 <= '0';

             xfer_2 <= '0';
   elsif OPB_Clk'event and OPB_Clk ='1' then

             xfer_1 <= xfer;

             xfer_2 <= xfer_1 and not rnw;
      end if;
end process;

-- combinational logic for BRAM
we <= (xfer or xfer_1) and not rnw;
ce0 <= xfer_1 and not rnw;
```

```
ce1 <= xfer_2;
a0 <= xfer_1;
opb_ad_ce <= not xfer;

bram_addr <= (not audio_fifohalf) & addr(7 downto 2) & a0;
bram_wdata <= wdata(31 downto 16) when a0='0' else wdata(15 downto 0);

-- tie unused to ground
UIO_errAck <= '0';
UIO_retry <= '0';
UIO_toutSup <= '0';
UIO_xferAck <= xfer;


-- instantiate the BRAMS
process (bram_rdata_rev) begin
        bram_rdata(0) <= bram_rdata_rev(8);
        bram_rdata(1) <= bram_rdata_rev(7);
        bram_rdata(2) <= bram_rdata_rev(6);
        bram_rdata(3) <= bram_rdata_rev(5);
        bram_rdata(4) <= bram_rdata_rev(4);
        bram_rdata(5) <= bram_rdata_rev(3);
        bram_rdata(6) <= bram_rdata_rev(2);
        bram_rdata(7) <= bram_rdata_rev(1);
        bram_rdata(8) <= bram_rdata_rev(0);
        -- sign extend
        bram_rdata(9) <= bram_rdata_rev(0);
        bram_rdata(10) <= bram_rdata_rev(0);
        bram_rdata(11) <= bram_rdata_rev(0);
        bram_rdata(12) <= bram_rdata_rev(0);
        bram_rdata(13) <= bram_rdata_rev(0);
        bram_rdata(14) <= bram_rdata_rev(0);
        bram_rdata(15) <= bram_rdata_rev(0);
--    for i in 6 to 15 loop
--          bram_rdata(i)<=bram_rdata_rev(21-i);
--    end loop;
end process;

process(bram_wdata) begin
      for i in 0 to 15 loop
            bram_wdata_rev(i)<=bram_wdata(15-i);
      end loop;
end process;

audio_bram_dacdata <= audio_bram_dacdata_v(0);
dac_bram : RAMB4_S1_S16 port map (
              DIA    => "0" ,
        ENA    => '1',
              WEA    => '0',
        RSTA   => '0',
              CLKA   => audio_bram_clk,
              ADDRA  => audio_bram_addr_dac,
              DOA    => audio_bram_dacdata_v,

              DIB    => bram_wdata_rev,
        ENB    => '1',
        WEB    => we,
              RSTB   => '0',
        CLKB   => OPB_Clk,
        ADDRB  => bram_addr,
        DOB    => open
);

audio_bram_adcdata_v(0) <= audio_bram_adcdata ;
adc_bram : RAMB4_S1_S16 port map (
              DIA    => audio_bram_adcdata_v,
        ENA    => '1',
              WEA    => '1',
        RSTA   => '0',
              CLKA   => audio_bram_clk,
              ADDRA  => audio_bram_addr_adc,
              DOA    => open,

              DIB    => X"0000",
        ENB    => '1',
        WEB    => '0',
              RSTB   => '0',
        CLKB   => OPB_Clk,
        ADDRB  => bram_addr,
        DOB    => bram_rdata_rev
);


-- the sound stuff



audio : audio_ak4565 port map(



      CLK => OPB_Clk,

   RST => OPB_Rst,



      audio_bram_clk => audio_bram_clk,

      audio_bram_addr_dac => audio_bram_addr_dac,

      audio_bram_addr_adc => audio_bram_addr_adc,

      audio_bram_dacdata =>   audio_bram_dacdata,

      audio_bram_adcdata => audio_bram_adcdata,


      interrupt => interrupt,

      audio_fifohalf => audio_fifohalf,
      AU_CSN_N => AU_CSN_N,
   AU_BCLK => AU_BCLK,
   AU_MCLK => AU_MCLK,
   AU_LRCK => AU_LRCK,
   AU_SDTI => AU_SDTI,
   AU_SDTO0 => AU_SDTO0

);


end Behavioral;
```

b. Codec Interface Module – audio_ak4565.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


library UNISIM;

use UNISIM.VComponents.all;



entity audio_ak4565 is



port  (

         CLK : in std_logic;

            RST : in std_logic;


            audio_bram_clk : out std_logic;

            audio_bram_addr_dac : out std_logic_vector(11 downto 0);

            audio_bram_addr_adc : out std_logic_vector(11 downto 0);


            audio_bram_dacdata : in std_logic;

            audio_bram_adcdata : out std_logic;
            interrupt : out std_logic;

            audio_fifohalf : out std_logic;



            AU_CSN_N : out std_logic;
      AU_BCLK : out std_logic;
      AU_MCLK : out std_logic;
      AU_LRCK : out std_logic;
      AU_SDTI : out std_logic;
      AU_SDTO0 : in std_logic
        );
end audio_ak4565;





architecture Behavioral of audio_ak4565 is



component RAMB4_S1_S16
--
  generic (
       INIT_00 : bit_vector :=
X"0000000000000000000000000000000000000000000000000000000000000000";
       INIT_01 : bit_vector :=
X"0000000000000000000000000000000000000000000000000000000000000000";
       INIT_02 : bit_vector :=
X"0000000000000000000000000000000000000000000000000000000000000000";
       INIT_03 : bit_vector :=
X"0000000000000000000000000000000000000000000000000000000000000000"

             );
--
  port (DIA    : in STD_LOGIC_VECTOR (0 downto 0);
        DIB    : in STD_LOGIC_VECTOR (15 downto 0);
        ENA    : in STD_logic;
        ENB    : in STD_logic;
        WEA    : in STD_logic;
        WEB    : in STD_logic;
        RSTA   : in STD_logic;
        RSTB   : in STD_logic;
        CLKA   : in STD_logic;
        CLKB   : in STD_logic;
        ADDRA  : in STD_LOGIC_VECTOR (11 downto 0);
        ADDRB  : in STD_LOGIC_VECTOR (7 downto 0);
        DOA    : out STD_LOGIC_VECTOR (0 downto 0);
        DOB    : out STD_LOGIC_VECTOR (15 downto 0));
end component;



signal clkcnt : std_logic_vector(4 downto 0);
signal audiocnt_dac, audiocnt_adc : std_logic_vector(11 downto 0);


signal audio_clk : std_logic;

signal lrck : std_logic;


begin


AU_CSN_N <= '1'; -- no chip select as we don't write the ctrl regs


-- generate the 3 clocks: master, serial, frame


process(CLK, RST)

begin

      if rst = '1' then

            clkcnt <= "00000";

      elsif clk'event and clk='1' then

            clkcnt <= clkcnt + 1;

      end if;

end process;

AU_MCLK <= clkcnt(1); -- master clock, 12.5 MHz

audio_clk <= clkcnt(4); -- this is the serial clock, 1.5625 Mhz

AU_BCLK <= not audio_clk; -- dont't ask but read AK4565 specs


process(audio_clk, RST)

begin

      if rst = '1' then

      audiocnt_dac <= "000000000000";

      audiocnt_adc <= "111111111111";
      lrck <= '0';

      elsif audio_clk'event and audio_clk='1' then

            audiocnt_dac <= audiocnt_dac + 1;

            audiocnt_adc <= audiocnt_adc + 1;

            lrck <= not audiocnt_dac(4);

      end if;

end process;

AU_LRCK <= lrck; -- audio clock, 48.828 kHz


interrupt <= not audiocnt_dac(10);

audio_fifohalf <= audiocnt_dac(11);


audio_bram_addr_dac <= audiocnt_dac;

audio_bram_addr_adc <= audiocnt_adc;

audio_bram_clk <= audio_clk;


--AU_SDTI <= audio_bram_dacdata;

AU_SDTI <= AU_SDTO0;

audio_bram_adcdata <= AU_SDTO0;


end architecture;
```

8. <u>C Code</u>

8.1. main.c

```
/***  FFT size is defined by the following preprocessor
defines/includes:
 *  main.c:
 *     #define FFT_SIZE
 *     #define BUFFER_SHIFT_OFFSET [=log2(FFT_SIZE)]
 *  isr.c:
```

```
 *     #define FFT_SIZE
 *  fft.c:
 *     #define FFT_SIZE
 *     #include "coeff(FFT_SIZE).c"
 *     Xuint16 nonswaps[] - must correspond to correct fft size
 *  graphics.c:
 *     Xuint16 correspond[] - must to bin correlations for correct fft
size
 ***/

#include "xbasic_types.h"
#include "xio.h"

#include "xintc_l.h"
#include "xuartlite_l.h"


#define W 640
#define H 480
#define VGA_START 0x00800000
#define AUDIO_START 0xFEFE0000
#define RED 0xE0
#define GREEN 0x1C
#define BLUE 0x03

#define FFT_SIZE 2048
#define BUFFER_SHIFT_OFFSET 11  // must =log2(FFT_SIZE), used for
double buffer

// defined in isr.c
extern void audio_intr_handler(void *callback);
extern volatile Xuint16 bufInUse[];
extern volatile Xuint16 bufReady[];
//extern Xuint32 droppedPackets, grabbedPackets, midFrameDrops;

Xuint32 audioBuffer[ FFT_SIZE*2 ];
Xuint32 audioBufferRIGHT[ FFT_SIZE ];
Xint16 *startLPtr, *startRPtr;

/*
 * setup_interrupts: Initialize the interrupt sources and handlers
 */
void setup_interrupts()
{
  /*
   * Reset the interrupt controller peripheral
   */

  /* Disable the interrupt signal */
  XIntc_mMasterDisable(XPAR_INTC_SINGLE_BASEADDR);
  /* Disable all interrupt sources */
  XIntc_mEnableIntr(XPAR_INTC_SINGLE_BASEADDR,0);
  /* Acknowledge all possible interrupt sources
     to make sure none are pending */
  XIntc_mAckIntr(XPAR_INTC_SINGLE_BASEADDR, 0xffffffff);

  /*
```

```
   * Install the codec interrupt handler
   */
  XIntc_InterruptVectorTable[XPAR_INTC_AK4565_INTERRUPT_INTR].Handler =
    audio_intr_handler;

  // enable interrupt sources
  /* Enable CPU interrupts */
  microblaze_enable_interrupts();
  /* Enable interrupts from the interrupt controller */
  XIntc_mMasterEnable(XPAR_INTC_SINGLE_BASEADDR);
  /* Tell the interrupt controller to accept interrupts from the codec
*/
  XIntc_mEnableIntr(XPAR_INTC_SINGLE_BASEADDR,
XPAR_AK4565_INTERRUPT_MASK);
}



int main()
{
  Xuint16 i, j, k, z;
  Xint32 x;

  print("[number one realtime spectrum analyzer max].\n\r");

  // Enable the instruction cache: makes the code run 6 times faster
  microblaze_enable_icache();

  setup_interrupts();

  //  clear screen
  for(x=0 ; x<H*W ; x++)
    XIo_Out8(VGA_START + x, 0);

  // this never changes, define outside loop.
  startRPtr = (Xint16*)(audioBufferRIGHT) - 1;

  i=0;
  for ( ;; ) {
    // ******************************
    // double buffer logistics
    while (bufReady[i] == 0)
      print("."); // need this delay, a busy-wait loop prevents isr
context switch?!
    bufInUse[(i+1) % 2] = 0;
    bufInUse[i] = 1;
    // ******************************


    // fudge starting pointers to account for FFT starting
    //  with index 1.
    startLPtr = (Xint16*)(&(audioBuffer[ (i<<BUFFER_SHIFT_OFFSET) ])) -
1;

    bitReverseAndLRSeparate( startLPtr, startRPtr );
    // after this point:
```

```
    //   audioBuffer[] holds bit-rearranged LEFT samples,
MSB=real/LSB=imag
    //   audioBufferRIGHT[] holds bit-rearranged RIGHT samples,
MSB=real/LSB=imag

    doFFT( startLPtr );
    doFFT( startRPtr );

    visualize( &(audioBuffer[ (i<<BUFFER_SHIFT_OFFSET) ]), 0 );
    visualize( audioBufferRIGHT, 1 );

    if (i==0) i++;
    else
      i=0;
  }

  return 0;
}
```

8.2. isr.c

```
#include "xbasic_types.h"
#include "xio.h"
#include "xparameters.h"
#include "xuartlite_l.h"

extern Xuint32 audioBuffer[];
extern Xuint32 audioBufferRIGHT[];
Xint32 bufPos = 0;
Xuint16 volatile bufInUse[] = {0, 0};
Xuint16 volatile bufReady[] = {0, 0};

// define: packet = set of 64 samples; frame= set of FFT_SIZE samples

/*
Xuint32 droppedPackets=0;
Xuint32 grabbedPackets=0;
Xuint32 midFrameDrops=0;
*/

#define FFT_SIZE 2048

/*
 * Interrupt service routine for the AK4565 CODEC
 */

void audio_intr_handler( void *callback ) {
  Xint16 i;

  // if the FFT isn't done yet, drop these samples.
  if (bufPos < FFT_SIZE) {
    if (bufInUse[0] == 1) {
      /*
      droppedPackets++;
      if (bufPos != 0)
      midFrameDrops++;
      */
      return;
    }
  }
  else if (bufInUse[1] == 1) {

    //    droppedPackets++;
    if (bufPos != FFT_SIZE)
      //      midFrameDrops++;
    return;
  }

  for (i=0; i < 64; i++) {
    XIo_Out32( XPAR_AK4565_BASEADDR + (i<<2), 0 );
    audioBuffer[bufPos++] = (XIo_In32( XPAR_AK4565_BASEADDR )); //
0xLLLLRRRR
  }

  if (bufPos == FFT_SIZE) {
    bufReady[0] = 1;
    bufReady[1] = 0;
  }
  else if (bufPos >= (FFT_SIZE * 2)) { // multiply here OK -- should
optimize to constant value
    bufReady[1] = 1;
    bufReady[0] = 0;
    bufPos = 0;
  }

  //  grabbedPackets++;
}
```

8.3. fft.c

```
#include "xbasic_types.h"
#include "xio.h"
#include "coeff2048.c"  // coefficients must be calculated for FFT size

#define FFT_SIZE 2048

extern Xuint32 coeff[];


/***********************************************************************
******/
// nonswaps[] identifies indices that do not get affected during
bitswapping.
//            index 0 holds the total # values in array


/*
const Xuint16 nonswaps256[] =
   { 17,
     1,   49,  73,  121, 133, 181, 205, 253, 259, 307, 331, 379,
     391, 439, 463, 511, 513 };
```

```
const Xuint16 nonswaps1024[] =
{ 33,
  1, 97, 145, 241, 265, 361, 409, 505, 517, 613, 661, 757, 781, 877,
925, 1021,
  1027, 1123, 1171, 1267, 1291, 1387, 1435, 1531, 1543, 1639, 1687,
1783,
  1807, 1903, 1951, 2047, 2049 };
*/

const Xuint16 nonswaps[] =
{ 65,
  1,    65,   161,  225,  273,  337,  433,  497,  521,  585,  681,
745,  793,
  857,  953,  1017, 1029, 1093, 1189, 1253, 1301, 1365, 1461, 1525,
1549, 1613,
  1709, 1773, 1821, 1885, 1981, 2045, 2051, 2115, 2211, 2275, 2323,
2387, 2483,
  2547, 2571, 2635, 2731, 2795, 2843, 2907, 3003, 3067, 3079, 3143,
3239, 3303,
  3351, 3415, 3511, 3575, 3599, 3663, 3759, 3823, 3871, 3935, 4031,
4095, 4097 };
/**********************************************************************
******/


/**
 * takes buffer data in dataL, in form 0xLLLLRRRR
 * separates L and R data and performs bit reversal of indices
 * returns two arrays, each ready to be FFT-ized
 * ---note: as with the FFT algorithm, this function will never access
idx[0]
 * fills all imaginary (even) indices with 0x0000.
 */
void bitReverseAndLRSeparate( Xint16 *dataL, Xint16 *dataR ) {
  int i, j, n, m;
  Xint16 tempL, tempR;

  n = FFT_SIZE << 1;
  j = 1;

  for ( i=1; i < n; i+=2 ) {
    if ( j > i ) {

      tempL = dataL[j];
      tempR = dataL[j+1];

      dataL[j] = dataL[i];
      dataR[j] = dataL[i+1];

      dataL[i] = tempL;
      dataR[i] = tempR;

      dataL[i+1] = 0x0000;
      dataL[j+1] = 0x0000;
      dataR[i+1] = 0x0000;
      dataR[j+1] = 0x0000;
    }

    m = FFT_SIZE;
    while ( (m >= 2) && (j > m) ) {
      j -= m;
      m >>= 1;
    }

    j += m;
  }

  // separate L and R for the indices that don't get bitreversed
  for (i=1; i < nonswaps[0]; i++) {
    dataR[ nonswaps[i] ] = dataL[ nonswaps[i]+1 ];

    dataL[ nonswaps[i]+1 ] = 0x0000;
    dataR[ nonswaps[i]+1 ] = 0x0000;
  }
}


// takes an array of size (FFT_SIZE * 2), of 16-bit values
// this function WILL NEVER access array index 0 (very important-no seg
faults)
void doFFT( Xint16 *data ) {
  //  int istep, mmax, j, i, m, n, coeff_ofs, z;
  Xint32 istep, mmax, j, i, m, n, coeff_ofs, z;
  Xint32 itr = 0;

  Xint16 *tempRI;
  Xuint32 temp;
  Xuint32* temp32;

  coeff_ofs = 0;

  n = FFT_SIZE << 1;
  mmax = 2;

  while ( n > mmax ) { // this, the outer loop, gets executed
log2(FFT_SIZE) times.
    istep = mmax << 1;

    for ( m=1; m<mmax; m+=2 ) {
      for ( i=m; i<=n; i+=istep ) {
      j = i + mmax;

      itr++;
      // And now, the guts of the whole project, the butterfly
operation:
      // (aka Danielson-Lanczos formula)

      temp32 = (Xuint32*)(&(data[j]));
      // write real and imag values of J to multiplier
      XIo_Out32( 0x0FEF0008, *temp32 );
      // write coefficients to multiplier
      XIo_Out32( 0x0FEF000C, coeff[ coeff_ofs ] );
      temp = XIo_In32( 0x0FEF0000 );

      tempRI = (Xint16*)(&temp);

      data[j] = data[i] - tempRI[0];
      data[j+1] = data[i+1] - (tempRI[1]);
      data[i] += tempRI[0];
      data[i+1] += tempRI[1];
      }
      coeff_ofs++;
    }
    mmax = istep;
  }
}
```

8.4. graphics.c

```
#include "xbasic_types.h"
#include "xio.h"

#include "xintc_l.h"
#include "xuartlite_l.h"

#define W 640
#define H 480
#define VGA_START 0x00800000
#define X_START 40
#define Y_START 240

#define RED 0xE0
#define GREEN 0x1C
#define BLUE 0x03
#define WHITE RED | GREEN | BLUE
#define BLACK 0x00

#define MAX_PIX 200

#define TRUE 1
#define FALSE 0

/*******************************************************************/
//correspond2048:

/*  [0]   [1]   [2]   [3]   [4]   [5]   [6]   [7]   [8]   [9]*/

Xuint16 correspond[] = {
     0,    1,    2,    3,    4,    5,    6,    7,    8,    9,
    10,   11,   13,   16,   20,   25,   31,   39,   49,   61,
    77,   97,  122,  153,  194,  244,  306,  387,  487,  612,
   773,  973};
/*******************************************************************/


static Xuint16 logScale[] = {
 0, 1, 4, 9, 16, 25, 36, 49, 64, 81, 100, 121, 144, 169, 196, 225, 256,
289, 324, 361, 400, 441, 484, 529, 576, 625, 676, 729, 784, 841, 900,
961, 1024, 1089, 1156, 1225, 1296, 1369, 1444, 1521, 1600, 1681, 1764,
1849, 1936, 2025, 2116, 2209, 2304, 2401, 2500, 2601, 2704, 2809, 2916,
3025, 3136, 3249, 3364, 3481, 3600, 3721, 3844, 3969, 4096, 4225, 4356,
4489, 4624, 4761, 4900, 5041, 5184, 5329, 5476, 5625, 5776, 5929, 6084,
6241, 6400, 6561, 6724, 6889, 7056, 7225, 7396, 7569, 7744, 7921, 8100,
8281, 8464, 8649, 8836, 9025, 9216, 9409, 9604, 9801, 10000, 10201,
10404, 10609, 10816, 11025, 11236, 11449, 11664, 11881, 12100, 12321,
12544, 12769, 12996, 13225, 13456, 13689, 13924, 14161, 14400, 14641,
14884, 15129, 15376, 15625, 15876, 16129, 16384, 16641, 16900, 17161,
17424, 17689, 17956, 18225, 18496, 18769, 19044, 19321, 19600, 19881,
20164, 20449, 20736, 21025, 21316, 21609, 21904, 22201, 22500, 22801,
23104, 23409, 23716, 24025, 24336, 24649, 24964, 25281, 25600, 25921,
26244, 26569, 26896, 27225, 27556, 27889, 28224, 28561, 28900, 29241,
29584, 29929, 30276, 30625, 30976, 31329, 31684, 32041, 32400, 32761
};

Xuint16 history[] = {
  0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
  0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
  0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };

Xuint16 barHistory[] = {
  0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
  0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
    0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
  0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 };

/* Method for drawing the Magnitude bar for each frequency band */
void drawBar(Xuint16 bin, int mag,  unsigned char direction) {
  Xuint32 vgaMem;
  Xint32 i;
  Xuint16 color= 0xffff, middle=0x49;
  Xint32 offset =0;
  unsigned char higher=0;
  unsigned int fourPixel = 0; //0xFF; //f0ffff;

  if (direction ==1)
    offset =30+bin;
  else
    offset = bin;

  /* Zero Out Noise */
  if (mag < 15) mag = 0;

  /* Update History if mag is higher */
  if(((history[offset]-6) < mag)) {
    //history[direction][bin] =
    barHistory[((offset))] = mag;
    history[(offset)] = mag;
    higher =1;
  } else {
    if((history[(offset)]) >6)
      history[(offset)]-= 6;  // comment this line and uncomment next
line
```

```
      //history[offset] = mag;  //    to disable slowed decay of bars
      else
        history[(offset)] =0;
      mag = history[(offset)];
    }

    /* draw black above color so screen refreshes */
    for (i=mag; i < MAX_PIX; i++) {
      if (direction)
        vgaMem = VGA_START + bin*16 + X_START + (Y_START - i-2)*640;
      else
        vgaMem = VGA_START + bin*16 + X_START + (Y_START + i+2)*640;

      XIo_Out32(vgaMem, 0x0);
      XIo_Out32(vgaMem+4, 0x0);
    }

    /* Print Middle Spacer Bar */
    for(i=0; i < 32; i++){

      fourPixel = (middle<<24);
      fourPixel = fourPixel | (middle<<16);
      fourPixel = fourPixel | (middle<<8);
      fourPixel = fourPixel | middle;

      /* Draw 3 pixel thick bar to separate Left and Right Results */
      vgaMem = VGA_START + (bin<<4) + X_START + (Y_START -1)*640 + i;
      XIo_Out32(vgaMem, fourPixel);
      XIo_Out32(vgaMem+4, fourPixel);

      vgaMem = VGA_START + (bin<<4) + X_START + (Y_START)*640 + i;
      XIo_Out32(vgaMem, fourPixel);
      XIo_Out32(vgaMem+4, fourPixel);

      vgaMem = VGA_START + (bin<<4) + X_START + (Y_START+1)*640 + i;
      XIo_Out32(vgaMem, fourPixel);
      XIo_Out32(vgaMem+4, fourPixel);
    }

    // If the Bar is Magnitude is smaller than History //
      if ( (higher==0) && (mag-6) > 0 ) {

        for (i=0 ; i < (mag-6); i++) {

        if (direction)
          vgaMem = VGA_START + (bin<<4) + X_START + (Y_START - i -
  2)*640;
        else
          vgaMem = VGA_START + (bin<<4) + X_START + (Y_START + i +
  2)*640;

        // If higher than 160, print RED //
        if(i > 160) {
          color = 224;
        }
        else { // ELSE, get color based on Magnitude //
          if((i&0x000000FF) == 4)
            color = 252;
          else if ((i&0x001f) == 16)
            color-=4;
        }

        // Set Color and Print Bar //
        fourPixel = (color<<24);
        fourPixel = fourPixel | (color<<16);
        fourPixel = fourPixel | (color<<8);
        fourPixel = fourPixel | color;
        XIo_Out32(vgaMem, fourPixel);
        XIo_Out32(vgaMem+4, fourPixel);
        }

      } else  if (higher == 1) {

        for (i=0; i < mag; i++) {

        if (direction)
          vgaMem = VGA_START + (bin<<4) + X_START + (Y_START - i -
  2)*640;
        else
          vgaMem = VGA_START + (bin<<4) + X_START + (Y_START + i +
  2)*640;
        /* If higher than 160, print RED */
        if(i > 160) {
          color = 224;
        }
        else { /* ELSE, get color based on Magnitude */
          if((i&0x000000FF) == 4)
            color = 252;
          else if ((i&0x001f) == 16)
            color-=4;
        }

        /* Set Color and Print Bar */
        fourPixel = (color<<24);
        fourPixel = fourPixel | (color<<16);
        fourPixel = fourPixel | (color<<8);
        fourPixel = fourPixel | color;
        XIo_Out32(vgaMem, fourPixel);
        XIo_Out32(vgaMem+4, fourPixel);
        }
      }

      mag = barHistory[(offset)];

      if ( (mag > 3 ) && (higher ==0) ){
        mag -= 3;
        barHistory[(offset)] = mag;

        if ( direction ==0 )
        vgaMem = VGA_START + (bin<<4) + X_START + (Y_START + mag )*640;
        else
        vgaMem = VGA_START + (bin<<4) + X_START + (Y_START - mag )*640;
      fourPixel = (middle<<24);
      fourPixel = fourPixel | (middle<<16);
      fourPixel = fourPixel | (middle<<8);
      fourPixel = fourPixel | middle;

      XIo_Out32(vgaMem, fourPixel);
      XIo_Out32(vgaMem+4, fourPixel);
      }
}

Xuint16 calcMagnitude( Xuint32 data ) {
  Xint16 *tempRI;
  Xuint32 result;
  short high = 182, low = 0, middle;
  unsigned char less = 0;
  short temp;

  // calculate magnitudes of buckets corresponding to positive
frequencies
  // hw address 0x0fef_0014 squares real and imag.

  XIo_Out32( 0x0FEF0014, data );
  result = XIo_In32( 0x0FEF0000 );

  tempRI = (Xuint16*)(&result);
  result = (Xuint32)(tempRI[0]) + (Xuint32)(tempRI[1]);

  // saturate, don't overflow
  if (result > 32767)
    result = 32750;

  while( low <= high )
    {
      middle = ( low  + high ) / 2;
      if( result == logScale[  middle ] ) //match
      return middle;
      else if( result < logScale[ middle ] ) {
      high = middle - 1;     //search low end of array
      less =1;
      }
      else {
      low = middle + 1;      //search high end of array
      less = 0;
      }
    }
  if(less == 0) {
    if (middle > 180)
      return 180;
    else
      return middle;
  }
  else
    return middle-1;
}
```

```
void visualize( const Xuint32* fftData, const unsigned char direction )
{
  Xint32 i;
  Xint32 currBin, endBin;
  Xuint16 secondHighest;
  Xuint16 tempo;
  Xuint16 binMagnitude;

  // figure out which bin magnitudes pair up with which bands

  /*[0]   [1]   [2]   [3]   [4]   [5]   [6]   [7]   [8]   [9]
     0,  0/1,    1,  1/2,    2,  2/3,    3,    4,    5,    7,
     8,   10,   13,   16,   20,   25,   31,   39,   49,   61,
    77,   97,  122,  153,  194,  244,  306,  387,  487,  612,
   773, [973] */

  // fill upper bands (bin resolution >= 1) with peak from range
  for (i=0; i<31; i++) {
    binMagnitude = 0;
    secondHighest = 0;
    endBin = correspond[i+1];

    for (currBin = correspond[i]; currBin < endBin; currBin++) {
      tempo = calcMagnitude( fftData[currBin] );
      if (tempo > secondHighest) {
      if (tempo >= binMagnitude) {
        secondHighest = binMagnitude;
        binMagnitude = tempo;
      }
      else {
        secondHighest = tempo;
      }
      }
    }

    if (i < 15)
      drawBar(i, binMagnitude, direction);
    else
      drawBar(i, secondHighest, direction);
  }

}
```

8.5. coeff2048.c

```
[font size reduced]
static                  0x30fb7640,             0x00007ffb,             0x70e13c53,             0xe70b7d7f,
Xuint32                 0x00007ffe,             0xe7097d85,             0x6a6c4719,             0xdadd7a72,
coeff[] = {             0xcf05763f,             0xcf07763c,             0x62f0512f,             0xcf0b7637,
0x7FFF0000,             0xa5805a80,             0xb8e76a68,             0x5a805a7d,             0xc3b270d8,
0x7FFF0000,             0x89c230fa,             0xa5835a7d,             0x513162ec,             0xb8ed6a63,
0x00007FFF,             0x7FFF0000,             0x95994718,             0x471a6a67,             0xaed862e8,
0x7FFF0000,             0x7d8a18f8,             0x89c630f8,             0x3c5470db,             0xa58b5a79,
0x5a825a82,             0x764130fa,             0x827e18f6,             0x30f97639,             0x9d1d512b,
0x00007fff,             0x6a6d471b,             0x7FFF0000,             0x25267a74,             0x95a34715,
0xa57f5a81,             0x5a825a80,             0x7f620c8b,             0x18f77d81,             0x8f2f3c50,
0x7FFF0000,             0x471c6a6b,             0x7d8a18f7,             0x0c8b7f58,             0x89d130f6,
0x764130fb,             0x30fb763e,             0x7a7c2526,             0x00007ff5,             0x85972524,
0x5a825a81,             0x18f87d86,             0x764030f9,             0xf3767f57,             0x828a18f6,
0x80b30c8b,        0x763c30f2,        0xa381581c,        0x68974993,        0xfb517f98,
0x7FFF0000,        0x74ff33d5,        0xa15f55d0,        0x67ad4ada,        0xf9c17f86,
0x7fd80647,        0x73b036b0,        0x9f4c5376,        0x66bf4c1e,        0xf8317f6f,
0x7f610c8a,        0x724f3982,        0x9d485110,        0x65cd4d5f,        0xf6a17f54,
0x7e9c12c6,        0x70dc3c4b,        0x9b534e9d,        0x64d74e9d,        0xf5127f34,
0x7d8918f6,        0x6f583f0b,        0x996d4c1e,        0x63de4fd8,        0xf3837f0f,
0x7c281f17,        0x6dc341c1,        0x97974993,        0x62e15110,        0xf1f57ee5,
0x7a7b2524,        0x6c1d446d,        0x95d146fd,        0x61e05245,        0xf0677eb6,
0x78822b1b,        0x6a66470e,        0x941c445c,        0x60db5376,        0xeeda7e82,
0x763f30f7,        0x689f49a4,        0x927741b0,        0x5fd254a4,        0xed4d7e49,
0x73b336b5,        0x66c84c2f,        0x90e33efa,        0x5ec655cf,        0xebc17e0b,
0x70e03c51,        0x64e14eae,        0x8f603c3b,        0x5db656f7,        0xea367dc8,
0x6dc741c8,        0x62ea5121,        0x8def3972,        0x5ca2581b,        0xe8ac7d81,
0x6a6a4716,        0x60e45388,        0x8c8f36a0,        0x5b8b593c,        0xe7237d35,
0x66cc4c38,        0x5ecf55e2,        0x8b4133c6,        0x5a705a59,        0xe59b7ce4,
0x62ee512b,        0x5cac582f,        0x8a0530e4,        0x59525b73,        0xe4147c8e,
0x5ed355ec,        0x5a7a5a6e,        0x88db2dfb,        0x58305c89,        0xe28e7c33,
0x5a7e5a78,        0x583a5c9f,        0x87c42b0a,        0x570b5d9c,        0xe1097bd4,
0x55f15ecc,        0x55ed5ec2,        0x86bf2813,        0x55e35eab,        0xdf857b70,
0x512f62e6,        0x539360d6,        0x85cd2516,        0x54b75fb6,        0xde027b07,
0x4c3b66c3,        0x512c62db,        0x84ee2213,        0x538860be,        0xdc817a99,
0x47186a60,        0x4eb864d1,        0x84221f0b,        0x525661c2,        0xdb017a27,
0x41c96dbc,        0x4c3866b7,        0x83691bfe,        0x512162c2,        0xd98279b0,
0x3c5270d4,        0x49ac688d,        0x82c318ed,        0x4fe963be,        0xd8057934,
0x36b673a6,        0x47156a53,        0x823115d8,        0x4eae64b7,        0xd68a78b4,
0x30f87631,        0x44736c09,        0x81b212bf,        0x4d7065ac,        0xd510782f,
0x2b1c7873,        0x41c66dae,        0x81460fa4,        0x4c2f669d,        0xd39877a5,
0x25257a6b,        0x3f0f6f42,        0x80ee0c86,        0x4aeb678a,        0xd2217717,
0x1f177c17,        0x3c4f70c5,        0x80aa0966,        0x49a46873,        0xd0ac7684,
0x18f67d77,        0x39857237,        0x80790645,        0x485a6958,        0xcf3975ed,
0x12c67e89,        0x36b37397,        0x805c0323,        0x470d6a39,        0xcdc87551,
0x0c8a7f4d,        0x33d874e5,        0x7FFF0000,        0x45bd6b16,        0xcc5974b0,
0x06477fc3,        0x30f57621,        0x7ffd0192,        0x446b6bef,        0xcaec740b,
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0xb3736458,       0x9f3b50b6,       0x8fe33914,       0x862a1e9f,       0x829002a9,
0xb325641b,       0x9efc5069,       0x8fb738bb,       0x86131e3f,       0x828f0246,
0xb2d763de,       0x9ebd501c,       0x8f8b3862,       0x85fc1ddf,       0x828e01e3,
0xb28963a1,       0x9e7f4fcf,       0x8f5f3809,       0x85e51d7f,       0x828d0180,
0xb23b6364,       0x9e414f82,       0x8f3437b0,       0x85ce1d1f,       0x828c011d,
0xb1ee6326,       0x9e034f35,       0x8f093757,       0x85b81cbe,       0x828c00ba,
0xb1a162e8,       0x9dc54ee7,       0x8ede36fe,       0x85a21c5d,       0x828c0057};
```

9. Other Files

9.1. system.mhs

```
# Parameters
PARAMETER VERSION = 2.0.0

# Global Ports

PORT PB_A = PB_A, DIR = OUT, VEC = [19:0]
PORT PB_D = PB_D, DIR = INOUT, VEC = [15:0]
PORT PB_LB_N = PB_LB_N, DIR = OUT
PORT PB_UB_N = PB_UB_N, DIR = OUT
PORT PB_WE_N = PB_WE_N, DIR = OUT
PORT PB_OE_N = PB_OE_N, DIR = OUT
PORT RAM_CE_N = RAM_CE_N, DIR = OUT
PORT VIDOUT_CLK = VIDOUT_CLK, DIR = OUT
PORT VIDOUT_HSYNC_N = VIDOUT_HSYNC_N, DIR = OUT
PORT VIDOUT_VSYNC_N = VIDOUT_VSYNC_N, DIR = OUT
PORT VIDOUT_BLANK_N = VIDOUT_BLANK_N, DIR = OUT
PORT VIDOUT_RCR = VIDOUT_RCR, DIR = OUT, VEC = [9:0]
PORT VIDOUT_GY = VIDOUT_GY, DIR = OUT, VEC = [9:0]
PORT VIDOUT_BCB = VIDOUT_BCB, DIR = OUT, VEC = [9:0]
PORT FPGA_CLK1 = FPGA_CLK1, DIR = IN
PORT RS232_TD = RS232_TD, DIR=OUT
PORT RS232_RD = RS232_RD, DIR=IN
PORT AU_CSN_N =  AU_CSN_N, DIR=OUT
PORT AU_BCLK =  AU_BCLK, DIR=OUT
PORT AU_MCLK = AU_MCLK, DIR=OUT
PORT AU_LRCK = AU_LRCK, DIR=OUT
PORT AU_SDTI = AU_SDTI, DIR=OUT
PORT AU_SDTO0 = AU_SDTO0, DIR=IN

# Sub Components


BEGIN microblaze
 PARAMETER INSTANCE = mymicroblaze
 PARAMETER HW_VER = 2.00.a
 PARAMETER C_USE_BARREL = 1
 PARAMETER C_USE_ICACHE = 1
 PARAMETER C_ADDR_TAG_BITS = 6
 PARAMETER C_CACHE_BYTE_SIZE = 2048
 PARAMETER C_ICACHE_BASEADDR = 0x00860000
 PARAMETER C_ICACHE_HIGHADDR = 0x0087FFFF
 PORT Clk = sys_clk
 PORT Reset = fpga_reset
 PORT Interrupt = intr
 BUS_INTERFACE DLMB = d_lmb
 BUS_INTERFACE ILMB = i_lmb
 BUS_INTERFACE DOPB = myopb_bus
 BUS_INTERFACE IOPB = myopb_bus
END

BEGIN opb_intc
```

```
 PARAMETER INSTANCE = intc
 PARAMETER HW_VER = 1.00.c
 PARAMETER C_BASEADDR = 0xFEFF0000
 PARAMETER C_HIGHADDR = 0xFEFF00FF
 PORT OPB_Clk = sys_clk
 PORT Intr =  uart_intr & audio_intr
 PORT Irq =   intr
 BUS_INTERFACE SOPB = myopb_bus
END

BEGIN bram_block
 PARAMETER INSTANCE = bram
 PARAMETER HW_VER = 1.00.a
 BUS_INTERFACE PORTA = conn_0
 BUS_INTERFACE PORTB = conn_1
END

BEGIN opb_xsb300
 PARAMETER INSTANCE = xsb300
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_BASEADDR = 0x00800000
 PARAMETER C_HIGHADDR = 0x00FFFFFF
 PORT PB_A = PB_A
 PORT PB_D = PB_D
 PORT PB_LB_N = PB_LB_N
 PORT PB_UB_N = PB_UB_N
 PORT PB_WE_N = PB_WE_N
 PORT PB_OE_N = PB_OE_N
 PORT RAM_CE_N = RAM_CE_N
 PORT OPB_Clk = sys_clk
 PORT pixel_clock = pixel_clock
 PORT VIDOUT_CLK = VIDOUT_CLK
 PORT VIDOUT_HSYNC_N = VIDOUT_HSYNC_N
 PORT VIDOUT_VSYNC_N = VIDOUT_VSYNC_N
 PORT VIDOUT_BLANK_N = VIDOUT_BLANK_N
 PORT VIDOUT_RCR = VIDOUT_RCR
 PORT VIDOUT_GY = VIDOUT_GY
 PORT VIDOUT_BCB = VIDOUT_BCB
 BUS_INTERFACE SOPB = myopb_bus
END

BEGIN opb_xsb300_ak4565
 PARAMETER INSTANCE = ak4565
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_BASEADDR = 0xFEFE0000
 PARAMETER C_HIGHADDR = 0xFEFEFFFF

 PORT OPB_Clk = sys_clk
 PORT Interrupt = audio_intr
 PORT AU_CSN_N =  AU_CSN_N
 PORT AU_BCLK =  AU_BCLK
 PORT AU_MCLK = AU_MCLK
 PORT AU_LRCK = AU_LRCK
 PORT AU_SDTI = AU_SDTI
 PORT AU_SDTO0 = AU_SDTO0

 BUS_INTERFACE SOPB = myopb_bus
```

```
END

BEGIN opb_xsb300_nortsam
 PARAMETER INSTANCE = nortsam
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_BASEADDR = 0x0FEF0000
 PARAMETER C_HIGHADDR = 0x0FEFFFFF

 PORT OPB_Clk = sys_clk
 PORT Interrupt = nortsam_intr

 BUS_INTERFACE SOPB = myopb_bus
END

BEGIN clkgen
 PARAMETER INSTANCE = clkgen_0
 PARAMETER HW_VER = 1.00.a
 PORT FPGA_CLK1 = FPGA_CLK1
 PORT sys_clk = sys_clk
 PORT pixel_clock = pixel_clock
 PORT fpga_reset = fpga_reset
END

BEGIN lmb_lmb_bram_if_cntlr
 PARAMETER INSTANCE = lmb_lmb_bram_if_cntlr_0
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_BASEADDR = 0x00000000
 PARAMETER C_HIGHADDR = 0x00000FFF
 BUS_INTERFACE DLMB = d_lmb
 BUS_INTERFACE ILMB = i_lmb
 BUS_INTERFACE PORTA = conn_0
 BUS_INTERFACE PORTB = conn_1
END

BEGIN opb_uartlite
 PARAMETER INSTANCE = myuart
 PARAMETER HW_VER = 1.00.b
 PARAMETER C_CLK_FREQ = 50_000_000
 PARAMETER C_USE_PARITY = 0
 PARAMETER C_BASEADDR = 0xFEFF0100
 PARAMETER C_HIGHADDR = 0xFEFF01FF
 PORT OPB_Clk = sys_clk
 PORT Interrupt = uart_intr
 BUS_INTERFACE SOPB = myopb_bus
 PORT RX=RS232_RD
 PORT TX=RS232_TD
END

BEGIN opb_v20
 PARAMETER INSTANCE = myopb_bus
 PARAMETER HW_VER = 1.10.a
 PARAMETER C_DYNAM_PRIORITY = 0
 PARAMETER C_REG_GRANTS = 0
 PARAMETER C_PARK = 0
 PARAMETER C_PROC_INTRFCE = 0
 PARAMETER C_DEV_BLK_ID = 0
 PARAMETER C_DEV_MIR_ENABLE = 0
 PARAMETER C_BASEADDR = 0x0fff1000
 PARAMETER C_HIGHADDR = 0x0fff10ff
 PORT SYS_Rst = fpga_reset
 PORT OPB_Clk = sys_clk
END

BEGIN lmb_v10
 PARAMETER INSTANCE = d_lmb
 PARAMETER HW_VER = 1.00.a
 PORT LMB_Clk = sys_clk
 PORT SYS_Rst = fpga_reset
END

BEGIN lmb_v10
 PARAMETER INSTANCE = i_lmb
 PARAMETER HW_VER = 1.00.a
 PORT LMB_Clk = sys_clk
 PORT SYS_Rst = fpga_reset
END
```