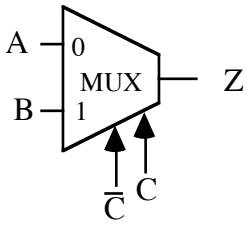
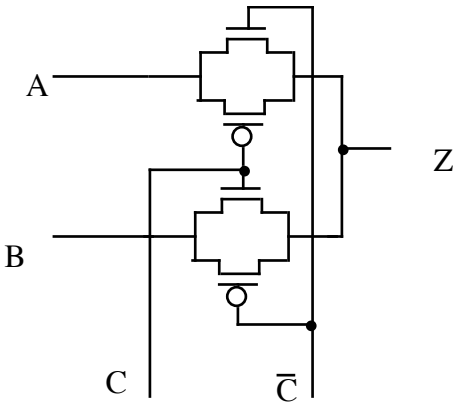
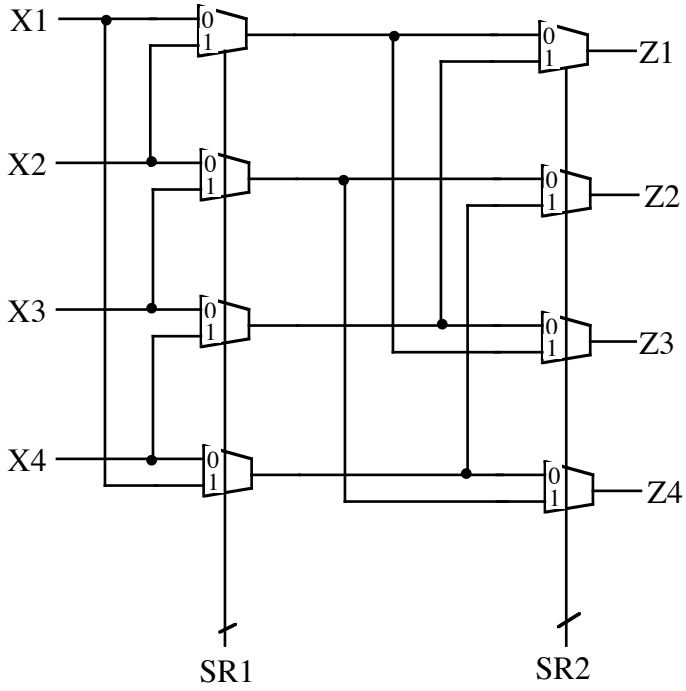
CS W4825 HW #8 Solutions

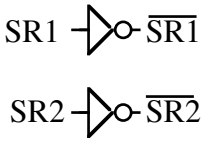
1. Design a 4-bit logarithmic shifter that shifts right rotary (i.e. the rightmost bit is shifted in to the left end, etc.). Use transmission gates. Number the elements, starting at the left end, as 4, 3, 2, 1.

Use as components the following 2-1MUX which has two complementary control inputs.



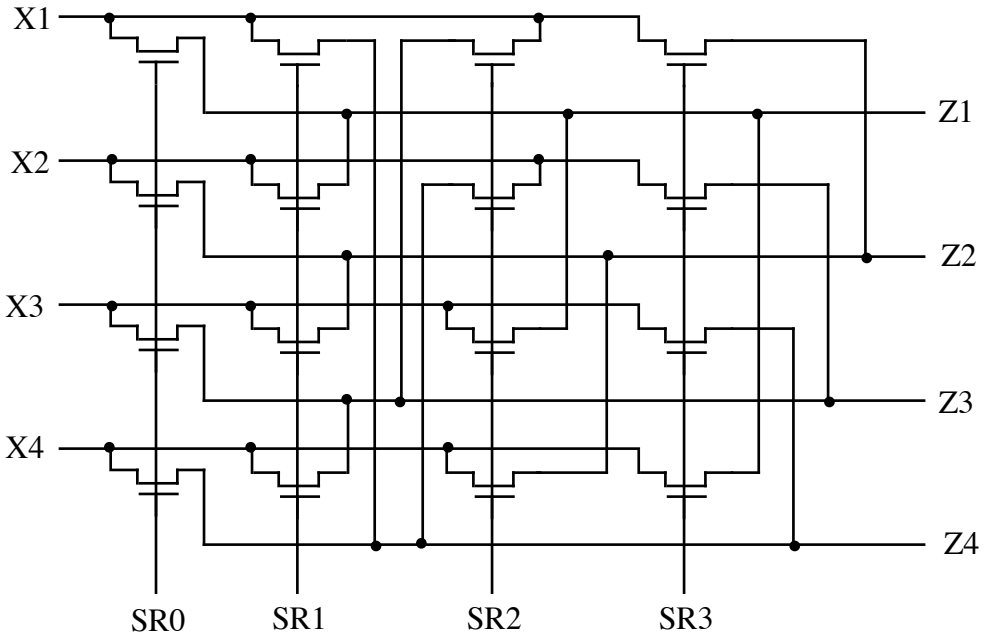






2. Repeat the previous problem, but now use a barrel shifter with single transistors as switches.

An effort was made here to make the array as regular as possible.,

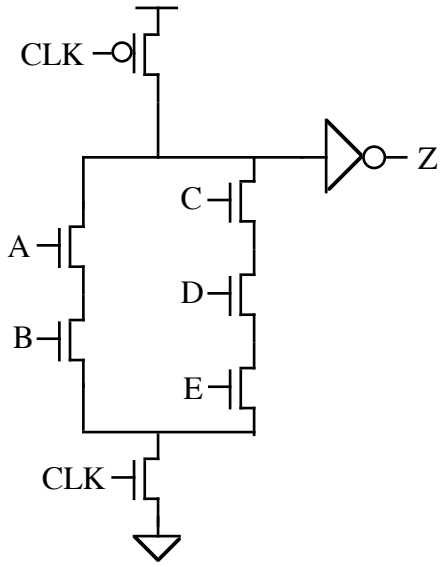


3. Assuming the use of single-transistors as switches, how many switching transistors are needed for a 64-bit rotary right shift logarithmic shifter? How many for a 64-bit barrel shifter? What happens to these numbers for arithmetic right shifters? What if we change to shift right logical operations?

For logarithmic shifters, for each stage, each of the n outputs must be fed thru one of two unique transistors, depending on whether that stage is fed by a 0 or 1 signal. In general, there are logn (base 2) stages. So the total number of switching transistors is 2nlogn. This is true for rotary, arithmetic, and logical shifts. For n=64, we thus have 2x64x6=768 transistors for each type of logarithmic shifter.

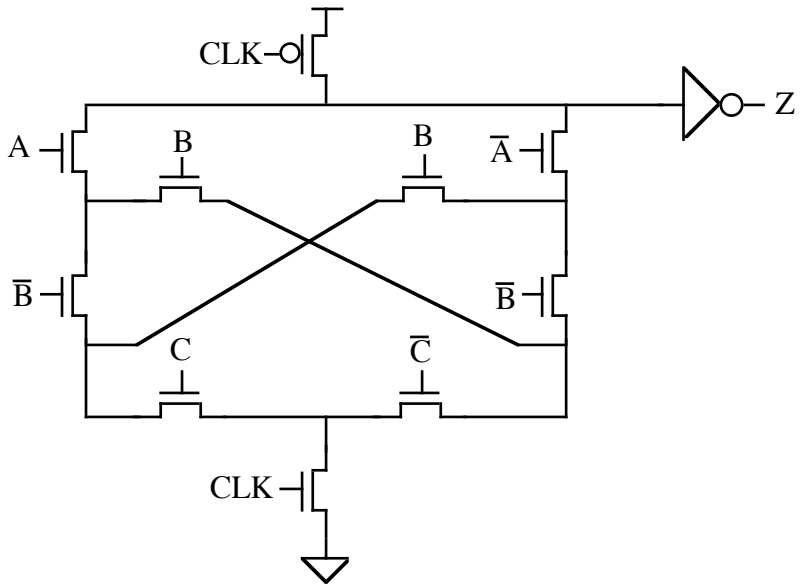
For the rotary barrel shifter, assuming one transistor switches, we need n^2 transistors for an n-bit register, so if n=64 we need 4096 transistors. Note that , for all types of barrel shifter, each output signal must be fed from a unique transistor for each shift amount. So the total number of transistors is n^2 for all three types of barrel shifter.

4. Draw a single domino logic gate that realizes the function described by Z=AB+CDE.

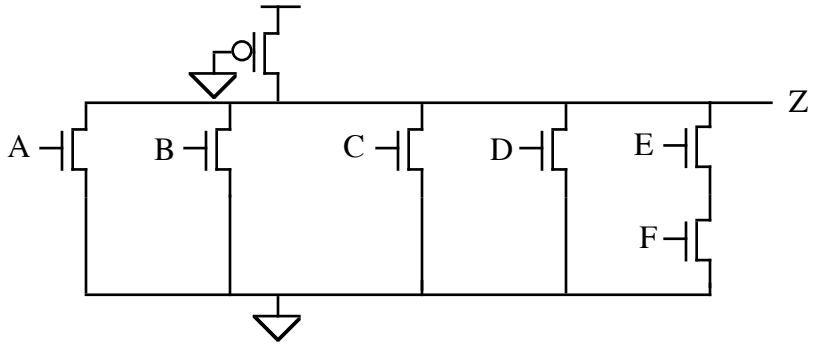


5. Draw an efficient domino logic circuit realizing $\overline{A \oplus B \oplus C}$, assuming double-rail inputs are available. Hint: if you don't restrict yourself to series-parallel circuits, 12 transistors are sufficient, including the inverter, the precharge transistor, and the evaluation transistor.

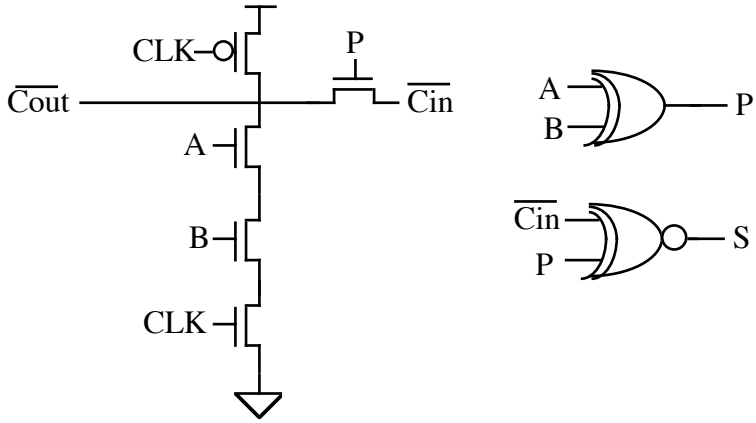
In the ckt below, the right branch of the pulldown ckt is the even parity side, and the left branch is the odd parity side. In order to get the correct output, we need to reach the bottom on the right side. Notice that the side is changed thru uncomplemented literals.



6. Draw a circuit for a complex pseudo-NMOS gate realizing $Z=\overline{A+B+C+D+EF}$



7. Draw a circuit for the dynamic version of a Manchester carry chain adder stage valid when the carry input is the complement of the true carry. This is the kind of stage needed when we intersperse inverters in the carry chain.



Note that the above gate for S (sometimes called an XNOR) can be realized using the same ckts used to generate the XOR but with the complemented input signal switched with its complement. Check this out.

8. In the design of the double-clocked latch, discussed in class, replace the two MUX's and
one of the inverters with a single complex CMOS gate.