

HW #8

1. Design a 4-bit logarithmic shifter that shifts right rotary (i.e. the rightmost bit is shifted in to the left end, etc.). Use transmission gates. Number the elements, starting at the left end, as 4, 3, 2, 1.
2. Repeat the previous problem, but now use a barrel shifter with single transistors as switches.
3. Assuming the use of single-transistors as switches, how many switching transistors are needed for a 64-bit rotary right shift logarithmic shifter? How many for a 64-bit barrel shifter? What happens to these numbers for arithmetic right shifters? What if we change to shift right logical operations?
4. Draw a single domino logic gate that realizes the function described by $Z=AB+CDE$.
5. Draw an efficient domino logic circuit realizing $\overline{A\oplus B\oplus C}$, assuming double-rail inputs are available. Hint: if you don't restrict yourself to series-parallel circuits, 12 transistors are sufficient, including the inverter, the precharge transistor, and the evaluation transistor.
6. Draw a circuit for a complex pseudo-NMOS gate realizing $Z=\overline{A+B+C+D+EF}$
7. Draw a circuit for the dynamic version of a Manchester carry chain adder stage valid when the carry input is the complement of the true carry. This is the kind of stage needed when we intersperse inverters in the carry chain.
8. In the design of the double-clocked latch, discussed in class, replace the two mux's and one of the inverters with a single complex CMOS gate.