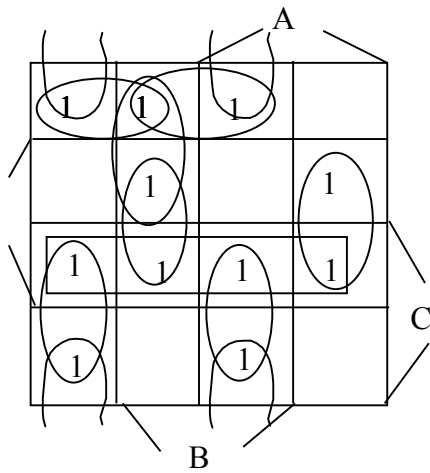
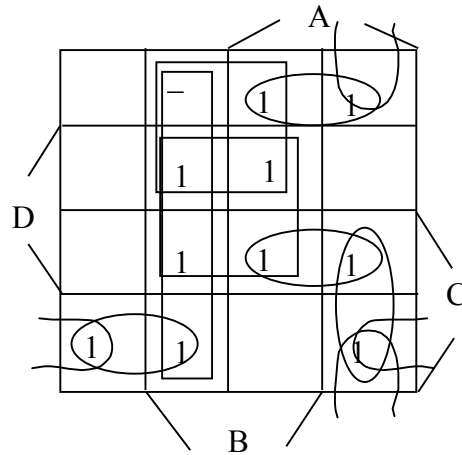


6.23. See K-maps below, where every adjacent pair of 1-points is covered by a selected prime implicant cube. The corresponding logic expressions follow.



(a)



(b)

(a) $Z = A'B'D' + A'B'C + A'C'D' + A'BC' + A'BD + BC'D' + CD + ABD' + ABC + AB'D$

(b) $Z = A'CD' + B'CD' + AB' + BC' + BD + AC'D' + ACD + AB'D' + AB'C$

6.25. There is an essential hazard starting in state 1-11, with C changing, and another starting in 3-10 with C changing

6.26. For the transition starting with $Q=0$ and CD changing from 11 to 01, a delay in the C-input to the second latch might cause Q to change to 1 (because the second latch will remain sensitive to its D-input, which will change when the first latch changes state as a result of its C-input changing to 1). The same delay might cause similar malfunction when $Q=1$, $D=0$, and C changes from 1 to 0.

6.29. The circuit is described by the tables of Fig. 6.32. There are essential hazards for transitions from 4-01 and 7-00, in both cases when X_1 is turned on. Consider first the transition from 4-01. Trouble occurs if the direct effect of the X_1 -change does not reach Y_3 until *after* the change in y_2 caused by the X_1 -change reaches Y_3 . In that event, y_3 will also change, leading the system to the wrong state. A large stray delay in the X_1 input to the NOR-gate generating Y_3 will cause this situation to occur.

For the transition from 7-00, the situation is reversed in that y_3 is supposed to change as a direct result of the X_1 -change, and a malfunction will occur if the change in y_3 reaches Y_2 before the signal from X_1 . Thus the malfunction can be made to occur by a large delay at the X_1 -input to the gate producing Y_2 .

In the 4-01 case, the path from X1 to Y3 via y2 passes thru just 2 gates, whereas in the 7-00 case, the trouble-producing path from X1 thru y3 to Y2 passes thru 4 gates. Thus the likelihood of trouble is significantly greater for the 4-01 case. Placing a sufficiently large delay element at the output of the gate generating Y2, or in the path from y2 to the input to the gate generating Y3 ensures against the occurrence of this particular malfunction.