

Curriculum Vitae

Personal Information

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Research Interests

My main research interests are in the asynchronous circuits, synthesis of asynchronous systems from high-level languages, optimizations for asynchronous systems, and interfacing of mixed-timing domains in system-on-a-chip design. An important trend in VLSI design is to build chips that contain multiple timing domains, both synchronous and asynchronous. My research attempts to facilitate this type of systems by proposing methods for fast and reliable communication between domains, and methods to optimize asynchronous domains synthesized from high-level description languages. These methods enable the integration of asynchronous domains, as well as synchronous domains each with a separate clock, in such chips with substantial improvements in performance.

Education

Fall 1997- Current Graduate Student, PhD Program of the Computer Science Department, Columbia University, New York, NY. Expected graduation date: May 2003.
1995-1996 Graduate Student, MSc Program, Department of Electrical Engineering, Politehnica University of Bucharest, Romania. Area of specialization: VLSI Design.
1990-1995 Student, Department of Electrical Engineering, Politehnica University of Bucharest, Romania. Degree: Bachelor of Science.

Publications

1. Tiberiu Chelcea, Steven M. Nowick, Andrew Bardsley, Doug Edwards, "Resynthesis and Peephole Transformations for the Optimization of Large-Scale Asynchronous Systems", submitted to the *IEEE Transactions on Computer Aided Design*.
2. Tiberiu Chelcea, Steven M. Nowick, "Resynthesis and peephole transformations for the optimization of large-scale asynchronous systems", *Proceedings of the 39th Design Automation Conference (DAC'02)*, 2002, Pp. 405-410.
3. Tiberiu Chelcea, Andrew Bardsley, Doug Edwards, Steven M. Nowick, "A Burst-Mode Oriented Back-End for the Balsa Synthesis System", *Proceedings of the Design, Automation and Test in Europe Conference (DATE'02)*, 2002, Pp. 330-337.

Overview: The above three papers discuss a novel optimizing back-end for the Balsa asynchronous synthesis system. The proposed back-end incorporates a new component modeling language, called CH, and several resynthesis and peephole optimizations. Furthermore, several low-level component synthesis CAD packages (such as Minimalist, Petrify) can be plugged into the new back-end to synthesize the modules. The speed improvements obtained on several examples range up to 54% over the basic Balsa implementations.

4. Tiberiu Chelcea, Steven M. Nowick, "Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols", *Proceedings of the 38th Design Automation Conference (DAC'01)*, 2001, Pp. 21-26.
5. Tiberiu Chelcea, Steven M. Nowick, "Low-Latency Asynchronous FIFO's Using Token Rings", *Proceedings of the Sixth International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'00)*, 2000, Pp. 210-220.
6. Tiberiu Chelcea, Steven M. Nowick, "A Low-Latency FIFO for Mixed-Clock Systems", *Proceedings of the IEEE Computer Society Workshop on VLSI (IWLSI'00)*, 2000, Pp. 119-126.

Overview: The above three papers introduce several low-latency, high-throughput FIFO's that can interface any combination of synchronous and asynchronous domains. Their design is highly modular: new FIFO types can be obtained by simply mixing pre-defined synchronous and asynchronous interfaces. The FIFO designs are also adapted to work as relay stations, interfacing latency-insensitive domains. The FIFO designs work at up to 500MHz in 0.6 μ technology, with a latency of 1-6 ns.

7. Tiberiu Chelcea, "Fast Pointers for Geometric Objects in Finite-Element Method", *Proceedings of RJJSAEM'96*, Sept. 1996.
8. Tiberiu Chelcea, Ioan Daniel, "A Hierarchy of Classes for the Finite Element Method", *Proceedings of the IEEE Conference on Electromagnetic Field Computation (IEEE-CEFC'96)*, March 1996.

Overview: The above two papers discuss the implementation of a tool for electromagnetic field computation using object-oriented programming techniques.

Patents

- "A Low-Latency FIFO for Mixed-Clock Systems", provisional application filed 2001 (pending).
- "Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols", provisional application filed 2001 (pending).
- "Low-Latency Asynchronous FIFO's Using Token Rings", provisional application filed 2001 (pending).

Experience	<ul style="list-style-type: none"> • Amulet Group, University of Manchester, UK. Academic Visitor, Summer 2000. Research on an optimizing back-end for the Balsa synthesis system, developed in the Amulet Group. The research lead to a paper at DATE'02. • Cogency Technology, Toronto, Canada. Summer Intern, 1999. Participated in the development of a proprietary synthesis system for asynchronous systems. • Young&Rubicam/MediaPro, Bucharest, Romania. 1993 - 1994. Part-time position. Duties: poll data analysis, database design and administration.
Teaching Experience	<ul style="list-style-type: none"> • Teaching Assistant for 4 courses: "Computer Organization", "Computer Architecture", "Digital Logic", "Computer-Aided Design of Digital Systems". Gave about 10 lectures in the above classes, contributed problems and provided solutions. • Instructor for the ACID-WG Summer School on Asynchronous Circuit Design, Grenoble, France, July 2002. Presented an intensive tutorial on Burst-Mode design with the Minimalist package. • Taught "Introduction to VLSI Design" laboratory, Fall 1996 semester, Department of Electrical Engineering, Politehnica University of Bucharest.
Technology Transfer	<ul style="list-style-type: none"> • Participated in the development of the MINIMALIST CAD package for the synthesis of asynchronous controllers from Burst-Mode machines. The software has been downloaded in 85 locations in 20 countries. • Participated in the development of a synthesis CAD tool for asynchronous systems from Verilog HDL. The tool is used internally at Cogency Technology, Toronto, Canada.
Additional Professional Activities	<p>Refereed papers for Design Automation Conference (DAC), and the IEEE Transactions on VLSI.</p> <p>IEEE Student Member.</p> <p>Translation from English into Romanian of several psychology tests, published in different books and magazines.</p>
Awards and Honors	<p>Paul Michelman Award for community service in the Computer Science Department, Columbia University, 2002.</p> <p>Sun Student Fellowship to attend Async-2001, Salt Lake City, Utah. Award amount: \$500.</p> <p>National Programming Contest, Romania: 3rd prize in 1988.</p>
Visa Status	F-1 (Student) currently, 1-year Practical Training (EAD) upon completion of studies.
Interests	Peer advising, mentoring and counseling, badminton, soccer.