I. Circuit Synthesis from the Program Dependence Graph

```
every R do
  loop
    await A;
    emit B;
    present C then emit D end;
    pause end
  ||
  loop
    present B then emit C end;
    pause end
end
```

II. High-Level State Assignment

```
abort
  pause; emit e;
  pause; emit f
when b;
abort
  pause; emit g;
  pause; emit h;
  pause; emit i
when c;
abort
  pause; emit j;
  pause; emit k
when d
```

III. Don't-Care Extraction from Control-flow Information

```
present A then
  emit B
else
  emit C end;
present C then
  present B end
else
  present B then emit D end
```