Compiling Parallel Algorithms to Memory Systems

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$(\lambda x. ?) f = \text{FPGA}$
Functional Programs to FPGAs
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Moore’s Law: Lots of Cheap Transistors...

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year.”

Closer to every 24 months

Pollack’s Rule: ...Give Diminishing Returns for Processors

Single-core processor performance follows the square root of area.

It takes 4× the transistors to give 2× the performance.

Fred J. Pollack, MICRO 1999 keynote. Graph from Borkar, DAC 2007
Dally: Calculation is Cheap; Communication is Costly

“Chips are power limited and most power is spent moving data

Performance = Parallelism
Efficiency = Locality

Bill Dally’s 2009 DAC Keynote, *The End of Denial Architecture*
Parallelism for Performance and Locality for Efficiency

Dally: “Single-thread processors are in denial about these two facts”

We need different programming paradigms and different architectures on which to run them.
Bacon et al.’s Liquid Metal

Fig. 2. Block level diagram of DES and Lime code snippet

public static Unsigned64 DEScoder(KeySchedule keys, Unsigned64 text)
{
    Unsigned64 block = text.permute(IP.Permutation);

    Unsigned32 R = block.extractBits(sixtyfour.b0, sixtyfour.b31);
    Unsigned32 L = block.extractBits(sixtyfour.b32, sixtyfour.b63);

    for (sixteen round) {
        Unsigned32 F = Fiestel(keys, round, R);
        Unsigned32 X = F ^ L;
        L = R;
        R = X;
    }

    Unsigned64 LR = makeUnsigned64(R, L);

    return LR.permute(FP.Permutation);
}

JITting Lime (Java-like, side-effect-free, streaming) to FPGAs
Huang, Hormati, Bacon, and Rabbah, Liquid Metal, ECOOP 2008.
```c
int squares() {
    int i = 0,
        sum = 0;
    for (; i < 10; i++)
        sum += i * i;
    return sum;
}
```

**Figure 3:** C program and its representation comprising three hyperblocks; each hyperblock is shown as a numbered rectangle. The dotted lines represent predicate values. (This figure omits the token edges used for memory synchronization.)

**Figure 8:** Memory access network and implementation of the value and token forwarding network. The LOAD produces a data value consumed by the oval node. The STORE node may depend on the load (i.e., we have a token edge between the LOAD and the STORE, shown as a dashed line). The token travels to the root of the tree, which is a load-store queue (LSQ).

C to asynchronous logic, monolithic memory

Figure 1. In-place map schematic and implementation

Algol-like imperative language to handshake circuits
Ghica, Smith, and Singh. *Geometry of Synthesis IV, ICFP 2011*
Greaves and Singh’s Kiwi

```csharp
public static void SendDeviceID()
{
    int deviceID = 0x76;
    for (int i = 7; i > 0; i--)
    {
        scl = false;
        sda_out = (deviceID & 64) != 0;
        Kiwi.Pause(); // Set it i−th bit of the device ID
        scl = true; Kiwi.Pause(); // Pulse SCL
        scl = false; deviceID = deviceID << 1;
        Kiwi.Pause();
    }
}
```

C# with a concurrency library to FPGAs

Arvind, Hoe et al.’s Bluespec

**GCD Mod Rule**
\[ \text{Gcd}(a, b) \text{ if } (a \geq b) \land (b \neq 0) \rightarrow \text{Gcd}(a - b, b) \]

**GCD Flip Rule**
\[ \text{Gcd}(a, b) \text{ if } a < b \rightarrow \text{Gcd}(b, a) \]

*Figure 1.3* Circuit for computing \( \text{Gcd}(a, b) \) from Example 1.

Guarded commands and functions to synchronous logic

Hoe and Arvind, *Term Rewriting*, VLSI 1999
Sheeran et al.’s Lava

```
bfly :: CmplxArithmetic m
      => [CmplxSig] -> m [CmplxSig]
bfly [i1, i2] =
    do o1 <- csubtract (i1, i2)
       o2 <- cplus (i1, i2)
    return [o1, o2]

bflys :: CmplxArithmetic m
       => Int -> [CmplxSig] -> m [CmplxSig]
bflys n =
    riffle >>= raised n two bfly >>= unriffle
```

**Functional specifications of regular structures**

Kuper et al.’s CλaSH

\[
\text{fir} \left( \text{State} \left( xs, hs \right) \right) x = \left( \text{State} \left( \text{shiftInto} x \, xs, hs \right), (x \triangleright xs) \bullet hs \right)
\]

More operational Haskell specifications of regular structures

Baaij, Kooijman, Kuper, Boeijink, and Gerards. Cλash, DSD 2010
AutoESL (Xilinx, was Cong’s xPilot)

**SSDM (System-level Synthesis Data Model)**

- Hierarchical netlist of concurrent processes and communication channels

- Each leaf process contains a sequential program which is represented by an extended LLVM IR with hardware-specific semantics
  - Port / IO interfaces, bit-vector manipulations, cycle-level notations

SystemC input; classical high-level synthesis for processes

Jason Cong, presentation at ISARS 2005
Optimization of Parallel “Programs” Enables Chip Design

Sun’s UltraSPARC T2
The “Niagara 2”
8 cores; 64 threads
Built 2007, 1.6 GHz, 65 nm
Released open-source as the OpenSPARC T2
www.opensparc.net

454 000 lines of synthesizable Verilog → 503 000 000 transistors
A mix of Boolean logic and structure
The Lesson of Logic Synthesis: the Enabling Technology

How do you compile and optimize a digital logic circuit?

\[ f_1 = abcd + abce + a\overline{bcd} + a\overline{b\overline{c}d} + \overline{ac} + cdf + ab\overline{cde} + a\overline{b\overline{c}d}f \]
\[ f_2 = bdg + \overline{bd}fg + \overline{bd}g + b\overline{deg} \]

After Brayton et al.’s class on Multi-Level Logic Synthesis

\[ f_1 = c(x + \overline{a}) + a\overline{cx} \]
\[ f_2 = gx \]
\[ x = d(b + f) + \overline{d}(\overline{b} + e) \]
The Lesson of Logic Synthesis: the Enabling Technology

How do you compile and optimize a digital logic circuit?

Use a simple, formal model and automate it.

\[ f_1 = abcd + abce + \overline{abcd} + ab\overline{cd} + \overline{ac} + cd\overline{f} + ab\overline{cde} + ab\overline{cd}f \]
\[ f_2 = bdfg + \overline{bd}fg + \overline{bd}g + b\overline{d}eg \]

Minimize

\[ f_1 = bcd + bce + \overline{bd} + \overline{ac} + cd\overline{f} + ab\overline{cde} + ab\overline{cd}f \]
\[ f_2 = bdfg + dfg + \overline{bd}g + d\overline{e}g \]

Factor

\[ f_1 = c(b(d + e) + \overline{b}(\overline{d} + f) + \overline{a}) + a\overline{c}(b\overline{d}\overline{e} + \overline{bd}\overline{f}) \]
\[ f_2 = g(d(b + f) + \overline{d}(\overline{b} + e)) \]

Decompose

\[ f_1 = c(x + \overline{a}) + a\overline{cx} \]
\[ f_2 = gx \]
\[ x = d(b + f) + \overline{d}(\overline{b} + e) \]

After Brayton et al.’s class on Multi-Level Logic Synthesis
High-Level Synthesis: Adding Time Meant Scheduling

Figure 2: (a) VHDL description; (b) Separate control and data-flow graphs

Figure 3: (a) FSM for scheduled CFG in Figure 2(b), (b) Hardware implementation of FSM using one-hot encoding

Bergamaschi, Behavioral Network Graph, DAC 1999.
The High-Level Synthesis Lessons

Don’t Start From C

“The so-called high-level specifications in reality grew out of the need for simulation and were often little more than an input language to make a discrete event simulator reproduce a specific behavior.”


Don’t Forget Memory

Goldstein et al.’s Phoenix synthesized asychronous hardware from ANSI C. Required heroic work [CGO 2003] to recover any parallelism.
Our Approach

C et al.  
gcc et al.  
x86 et al.  

Future Languages  
Higher-level languages  
Future ISAs  
More hardware reality  
A Functional IR  
FPGAs
Our Approach

- C et al.
- gcc et al.
- x86 et al.

Future Languages

Future ISAs

Higher-level languages

More hardware reality

abstraction

time

today
Our Approach

- C et al.
- gcc et al.
- x86 et al.

Future Languages

Higher-level languages

A Functional IR

Future ISAs

More hardware reality

FPGAs
Why Functional Specifications?

- Referential transparency/side-effect freedom make formal reasoning about programs vastly easier.

- Inherently concurrent and race-free (Thank Church and Rosser). If you want races and deadlocks, you need to add constructs.

- Immutable data structures makes it vastly easier to reason about memory in the presence of concurrency.
Why FPGAs?

- We do not know the structure of future memory systems
  Homogeneous/Heterogeneous?
  Levels of Hierarchy?
  Communication Mechanisms?

- We do not know the architecture of future multi-cores
  Programmable in Assembly/C?
  Single- or multi-threaded?

Use FPGAs as a surrogate. Ultimately too flexible, but representative of the long-term solution.
A Modern High-End FPGA: Altera’s Stratix V

2500 dual-ported 2.5KB 600 MHz memory blocks; 6 Mb total
350 36-bit 500 MHz DSP blocks (MAC-oriented datapaths)
300000 6-input LUTs; 28 nm feature size
Let’s Talk Details
Let’s Talk Details
Let’s Talk Details
Our Starting Point: A Functional IR

Inspired by the Glasgow Haskell Compiler’s “Core” representation

\[ expr ::= name \ var^* \]

Function call

Includes primitive arithmetic operators and type constructors

Non-tail-recursive calls generally inlined to improve parallelism; Mycroft and Sharp’s [IWLS 2000] propose sharing policies

True recursion transformed to tail recursion with a stack
Our Starting Point: A Functional IR

Inspired by the Glasgow Haskell Compiler’s “Core” representation

\[
expr ::= \text{name } var^* \\
| \text{let } (var = expr)^+ \text{ in } expr
\]

- Function call
- Parallel evaluation

Parallelism and sequencing:

\[
\begin{align*}
\text{let } v_1 &= e_1 \\
v_2 &= e_2 \\
v_3 &= e_3 \text{ in } e
\end{align*}
\]

\[
\begin{align*}
e_1 \\
e_2 \\
e_3
\end{align*}
\]

\begin{align*}
\text{evaluated in parallel, then } e
\end{align*}
Our Starting Point: A Functional IR

Inspired by the Glasgow Haskell Compiler’s “Core” representation

\[
expr ::= \text{name } var^* \\
| \text{let } (var = expr)^+ \text{ in } expr \\
| \text{case } var \text{ of } (pat \to expr)^+ \\
\]

\[
pat ::= \text{literal} \\
| _ \\
| \text{Constr. } (var | \text{literal} | _)^* \\
\]

| Function call |
| Parallel evaluation |
| Multiway conditional |

| Exact match |
| Default |
| Match a tagged union |

Evaluate and return one of the expressions based on the pattern
Our Starting Point: A Functional IR

Inspired by the Glasgow Haskell Compiler’s “Core” representation

\[
expr ::= \text{name } var^* \\
| \text{let } (var = expr)^+ \text{ in } expr \\
| \text{case } var \text{ of } (pat -> expr)^+ \\
| var \\
| \text{literal }
\]

\[
pat ::= \text{literal} \\
| \_
| \text{Constr. } (var \mid \text{literal} \mid \_)^*
\]

- Function call
- Parallel evaluation
- Multiway conditional
- Variable reference
- Literal value
- Exact match
- Default
- Match a tagged union
The Type System: Tagged Unions

Types are primitive (Boolean, Integer, etc.) or tagged unions:

\[
\text{type ::= Type} \\
\quad \mid \text{Constr Type}\ast \mid \cdots \mid \text{Constr Type}\ast
\]

Named type/primitive
Tagged union

Subsume C structs, unions, and enums
Comparable power to C++ objects with virtual methods
Sometimes called “algebraic data types”: sums of products
The Type System: Tagged Unions

Types are primitive (Boolean, Integer, etc.) or tagged unions:

\[
\text{type ::= Type} \quad \text{Named type/primitive} \\
| \quad \text{Constr Type}^* \quad \cdots \quad \text{Constr Type}^* \quad \text{Tagged union}
\]

Examples:

\textbf{data} \hspace{0.1cm} \text{Intlist} = \text{Nil} \quad -- \text{Linked list of integers} \\
\hspace{0.5cm} | \hspace{0.5cm} \text{Cons Int Intlist}

\textbf{data} \hspace{0.1cm} \text{Bintree} = \text{Leaf Int} \quad -- \text{Binary tree w/ integer leaves} \\
\hspace{0.5cm} | \hspace{0.5cm} \text{Branch BinTree Bintree}

\textbf{data} \hspace{0.1cm} \text{Expr} = \text{Literal Int} \quad -- \text{Arithmetic expression} \\
\hspace{0.5cm} | \hspace{0.5cm} \text{Var String} \\
\hspace{0.8cm} | \hspace{0.8cm} \text{Binop Expr Op Expr}

\textbf{data} \hspace{0.1cm} \text{Op} = \text{Add} | \text{Sub} | \text{Mult} | \text{Div}
Syntax-Directed Translation of Expressions to Hardware

Combinational functions:

Sequential functions:
Translating Let and Case

Let makes all new variables available to its body.

Case invokes one of its sub-expressions, then synchronizes.
Representing Recursive Algebraic Data Types

Consider a list of integers:

\[
data \text{ Intlist} = \text{Nil} \mid \text{Cons Int Intlist}
\]

An obvious representation:

- Usual byte-alignment unnecessary & wasteful in hardware
- Naturally stored & managed in a custom integer-list memory
- Width of pointer can depend on integer-list memory size
Removing Recursion: Recursive Fibonacci Example

Starting point: a dumb way to compute Fibonacci numbers

\[
\begin{align*}
\text{fib} & \ 1 = 1 \\
\text{fib} & \ 2 = 1 \\
\text{fib} & \ n = \text{fib} \ (n-1) + \text{fib} \ (n-2)
\end{align*}
\]
Removing Recursion: Recursive Fibonacci

Reformatting

\[
\begin{align*}
\text{fib} \ 1 &= 1 \\
\text{fib} \ 2 &= 1 \\
\text{fib} \ n &= \text{fib} \ (n-1) + \\
&\quad \text{fib} \ (n-2)
\end{align*}
\]
Removing Recursion: Continuation-Passing Style

In continuation-passing style (the “and then?” transformation):

\[
\begin{align*}
\text{fib} 1 \ c &= c \ 1 \\
\text{fib} 2 \ c &= c \ 1 \\
\text{fib} n \ c &= \text{fib} (n-1) \\
& \quad (n1 \to \text{fib} (n-2)) \\
& \quad (n2 \to c \ (n1 + n2)) \\
\text{fib} n &= \text{fib} n \ (x \to x)
\end{align*}
\]

-- Calls made sequential

-- Intermediates named

-- Add scheduled last

-- Wrapper
Removing Recursion: Naming Functions

Naming functions; converting unbound variables to arguments:

\[
\begin{align*}
\text{fib1} \ 1 \ c &= c \ 1 \\
\text{fib1} \ 2 \ c &= c \ 1 \\
\text{fib1} \ n \ c &= \text{fib1} \ (n-1) \ (\text{fib2} \ n \ c) \quad \text{--- Unbound variables passed} \\
\text{fib2} \ n \ c \ n1 &= \text{fib1} \ (n-2) \ (\text{fib3} \ n1 \ c) \quad \text{--- Lambdas named} \\
\text{fib3} \ n1 \ c \ n2 &= c \ (n1 + n2) \\
\text{fib} \ n &= \text{fib1} \ n \ \text{fib0} \\
\text{fib0} \ n &= n \quad \text{--- Identity function named}
\end{align*}
\]
Removing Recursion: True Recursion to Tail Recursion

Introducing a stack; merging functions

\[
\begin{align*}
    f \, (Fib1 \ 1 \ c) & = f \, (\text{Cont} \ c \ 1) \quad \text{-- Single function} \\
    f \, (Fib1 \ 2 \ c) & = f \, (\text{Cont} \ c \ 1) \quad \text{-- Continuation the stack} \\
    f \, (Fib1 \ n \ c) & = f \, (Fib1 \ (n-1) \ (Fib2 \ n \ c)) \\
    f \, (\text{Cont} \ (Fib2 \ n \ c) \ n1) & = f \, (Fib1 \ (n-2) \ (Fib3 \ n1 \ c)) \\
    f \, (\text{Cont} \ (Fib3 \ n1 \ c) \ n2) & = f \, (\text{Cont} \ c \ (n1 + n2)) \\
    f \, (Fib \ n) & = f \, (Fib1 \ n \ Fib0) \\
    f \, (\text{Cont} \ Fib0 \ n) & = n
\end{align*}
\]

-- Continuations (references to the lambda expressions)

```
data Stack = Fib2 \ Int \ Stack -- fib2 n c
  \mid Fib3 \ Int \ Stack -- fib3 n1 c
  \mid Fib0                 -- identity function (bottom of stack)
```

-- Invoke a named function or a continuation

```
data Action = Fib \ Int       -- fib n (outside call)
  \mid Fib1 \ Int \ Stack -- fib1 n c (recursive call)
  \mid Cont \ Stack \ Int  -- c (...) (invoke continuation)
```
Fibonacci Datapath

\[
\begin{align*}
  f \ (\text{Fib1} \ 1 \ c) & = f \ (\text{Cont} \ c \ 1) \\
  f \ (\text{Fib1} \ 2 \ c) & = f \ (\text{Cont} \ c \ 1) \\
  f \ (\text{Fib1} \ n \ c) & = f \ (\text{Fib1} \ (n-1) \ (\text{Fib2} \ n \ c)) \\
  f \ (\text{Cont} \ (\text{Fib2} \ n \ c) \ n1) & = f \ (\text{Fib1} \ (n-2) \ (\text{Fib3} \ n1 \ c)) \\
  f \ (\text{Cont} \ (\text{Fib3} \ n1 \ c) \ n2) & = f \ (\text{Cont} \ c \ (n1 + n2)) \\
  f \ (\text{Fib} \ n) & = f \ (\text{Fib1} \ n \ \text{Fib0}) \\
  f \ (\text{Cont} \ \text{Fib0} \ n) & = n \\
\end{align*}
\]

**data** Stack = Fib2 Int Stack | Fib3 Int Stack | Fib0

**data** Action = Fib Int | Fib1 Int Stack | Cont Stack Int
Implementing the Stack in Hardware

This uses a list-like stack data type:

```
data Stack = Fib2 Int Stack
         \ | Fib3 Int Stack
         \ | Fib0
```

A naïve, but correct, way to implement it in hardware:

```
<table>
<thead>
<tr>
<th>00</th>
</tr>
</thead>
</table>
Fib0

<table>
<thead>
<tr>
<th>01</th>
<th>Integer</th>
<th>Pointer</th>
</tr>
</thead>
</table>
Fib2 Int Stack

<table>
<thead>
<tr>
<th>10</th>
<th>Integer</th>
<th>Pointer</th>
</tr>
</thead>
</table>
Fib3 Int Stack

Encoded return address

Function activation record
Specializing Data Types: Recovering a Classical Stack

\[ \text{Fib3 42 (Fib2 17 (Fib3 8 (Fib3 2 Fib0))))} \]
Specializing Data Types: Recovering a Classical Stack

$Fib3\ 42\ (Fib2\ 17\ (Fib3\ 8\ (Fib3\ 2\ Fib0)))$

The only “pop” operation discards the previous top-of-stack

$$f\ (\text{Cont}\ (Fib3\ n1\ c)\ n2) = f\ (\text{Cont}\ c\ (n1 + n2))$$

so this code will never generate a tree. Sequential memory allocation is safe.
Specializing Data Types: Recovering a Classical Stack

\[ \text{Fib3 42 (Fib2 17 (Fib3 8 (Fib2 2 Fib0)))} \]

<table>
<thead>
<tr>
<th>Level</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>10</td>
<td>42</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>01</td>
<td>17</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>10</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Sequential memory allocation makes “next” pointers predictable...
Specializing Data Types: Recovering a Classical Stack

$Fib3 42 \ (Fib2 17 \ (Fib3 8 \ (Fib2 2 \ Fib0)))$

...so there is no need to store them.

Constructor (Fib0) always returns 0.

Constructors (Fib2/3 \ n \ s) writes (Fib2/3 \ n) at \ s + 1 and returns \ s + 1.

Reading 0 returns Fib0; reading \ s \ returns (Fib2/3 \ n \ s - 1).
Specializing Data Types

Stacks are the tip of the iceberg

Synthesizing custom memory systems for specific types is a key goal of this project

Shape Analysis relevant here

This is a simple case; a simple, mathematical IR enables such clever optimizations.

Imagine trying to do this in C.
Unrolling Code for Better Parallelism

fib 0 = 0
fib 1 = 1
fib n = fib (n−1) + fib (n−2)

fib (n−1) and fib (n−2) are functionally independent.

Yet because they share fib, they are performed sequentially.
Unrolling Code for Better Parallelism

\[ \text{fib} \ 0 = 0 \]
\[ \text{fib} \ 1 = 1 \]
\[ \text{fib} \ n = \text{fib}' \ (n-1) + \text{fib}'' \ (n-2) \]

\[ \text{fib}' \ 0 = 0 \]
\[ \text{fib}' \ 1 = 1 \]
\[ \text{fib}' \ n = \text{fib}' \ (n-1) + \text{fib}' \ (n-2) \]

\[ \text{fib}'' \ 0 = 0 \]
\[ \text{fib}'' \ 1 = 1 \]
\[ \text{fib}'' \ n = \text{fib}'' \ (n-1) + \text{fib}'' \ (n-2) \]

By unrolling the recursion once, \( \text{fib}' \) and \( \text{fib}'' \) run in parallel.

A further improvement: balance the work done by \( \text{fib}' \) and \( \text{fib}'' \)
Unrolling Types for Better Locality

```
data Stack = Fib2 \ Int \ Stack
  | Fib3 \ Int \ Stack
  | Fib0
```

Each Stack object naturally represents a single activation record
Unrolling Types for Better Locality

\[
\text{data } Stack = \text{Fib2} \text{ Int Stack'} \\
\quad \mid \text{Fib3} \text{ Int Stack'} \\
\quad \mid \text{Fib0}
\]

\[
\text{data } Stack' = \text{Fib2} \text{ Int Stack''} \\
\quad \mid \text{Fib3} \text{ Int Stack''} \\
\quad \mid \text{Fib0}
\]

\[
\text{data } Stack'' = \text{Fib2} \text{ Int Stack'''} \\
\quad \mid \text{Fib3} \text{ Int Stack'''} \\
\quad \mid \text{Fib0}
\]

\[
\text{data } Stack''' = \text{Fib2} \text{ Int Stack} \\
\quad \mid \text{Fib3} \text{ Int Stack} \\
\quad \mid \text{Fib0}
\]

A similar unrolling amounts to packing records that can be processed in parallel.

Abstract data types enables this.

Imagine trying to do this safely in a C compiler.
Example: Huffman Decoder in Haskell

\textbf{data} \quad \texttt{HTree} = \texttt{Branch HTree HTree} \quad | \quad \texttt{Leaf Char}

\texttt{decode} :: \quad \texttt{HTree} \to \texttt{[Bool]} \to \texttt{[Char]} \quad -- \quad \text{Huffman tree & bitstream to symbols}

\texttt{decode table str} = \texttt{decoder table str}
\hspace{1cm} \textbf{where}
\begin{align*}
\texttt{decoder (Leaf s) \ i} &= s : (\texttt{decoder table i}) \quad -- \text{Identified symbol; start again} \\
\texttt{decoder _ []} &= [] \\
\texttt{decoder (Branch f _)} (\texttt{False:xs}) &= \texttt{decoder f xs} \quad -- \ 0: \text{follow left branch} \\
\texttt{decoder (Branch _ t)} (\texttt{True:xs}) &= \texttt{decoder t xs} \quad -- \ 1: \text{follow right branch}
\end{align*}

Three data types: Input bitstream, output character stream, and Huffman tree
Optimizations

- Split Memories
- Use Streams
- Unroll for locality
- Speculate

Diagram:
- Memory
- HTree
- Input
- Output
- In FIFO
- Out FIFO
- Mem
- HTree
- Mem
- Speculate
Target Applications

- “Data-parallel irregular applications [that] manipulate large pointer-based data structures like graphs”
  [Pingali et al.’s Galois project]

- Datatype accelerators
  Hash tables, Balanced trees, Heaps

- Application-domain accelerators
  Relational databases, Cryptography, Data compression

- Non-scientific computing: the stuff that’s hard for vector units and GPGPUs
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See his keynote tomorrow

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