



# So What About Variability...

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# A Looming Problem

- ◆ Integrated circuit manufacturing variability has been increasing with process scaling.
- ◆ Within-die variability causes a decrease in circuit performance that is not recoverable by binning.
- ◆ Lack of models and analysis tools causes excessive conservatism in the design process and therefore reduces potential performance.

# Variability Sources

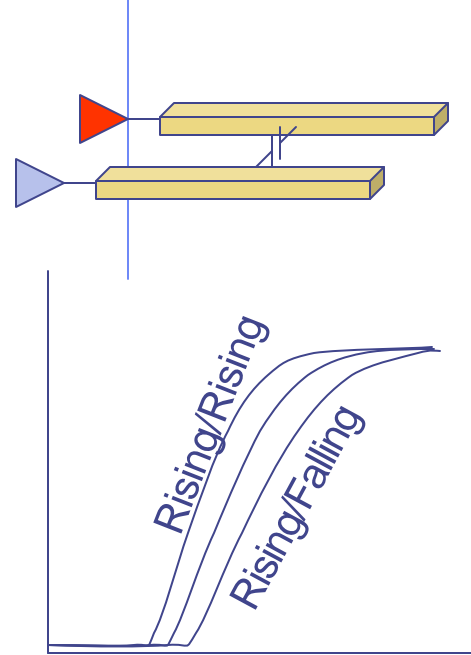
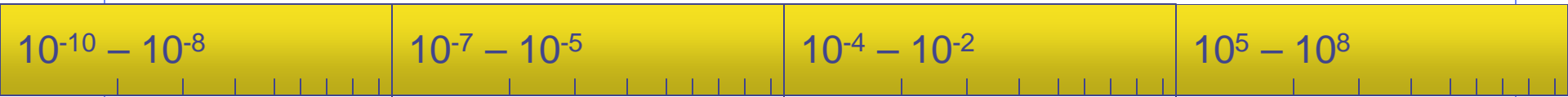
## Physical:

- ◆ Changes in characteristics of devices and wires.
- ◆ Caused by IC manufacturing process & wear-out.
- ◆ Time scale:  $10^8$ sec (months).

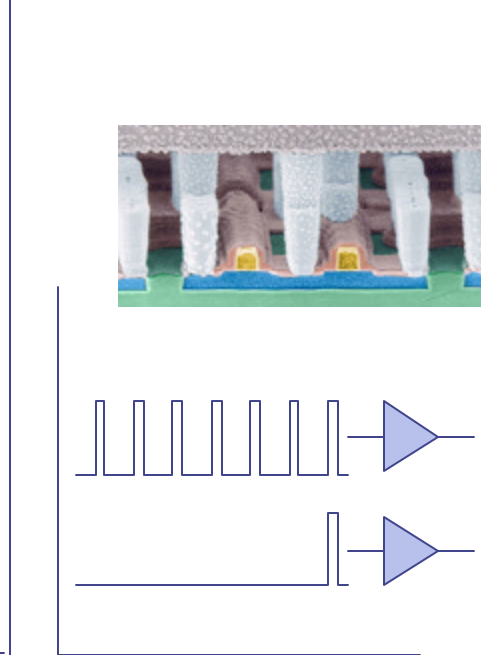
## Environmental:

- ◆ Changes in  $V_{DD}$ , Temperature, local coupling.
- ◆ Caused by the specifics of the design implementation.
- ◆ Time scale:  $10^{-6}$  to  $10^{-10}$ sec (clock tick).
  
- ◆ Roughly equal... Delay can change as much as 2X.

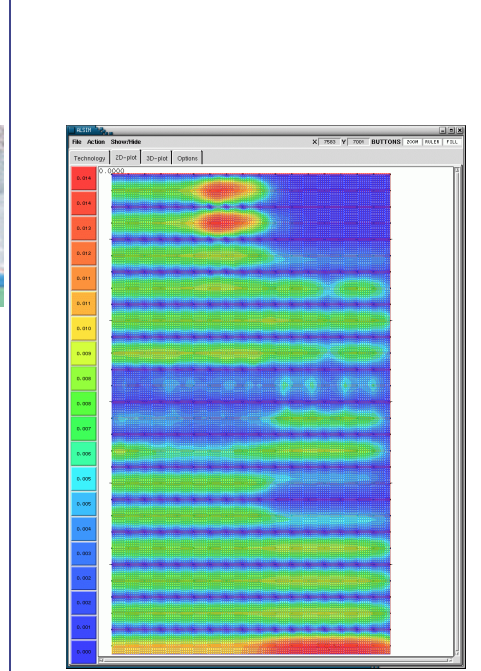
# Variability Time Scales



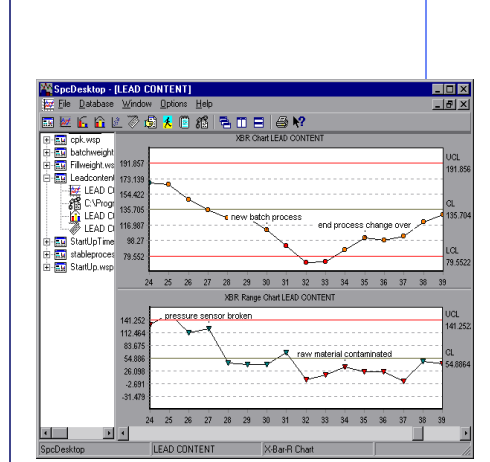
Signal Coupling



SOI Body History  
 $V_{DD}$ /Package Noise



Temperature

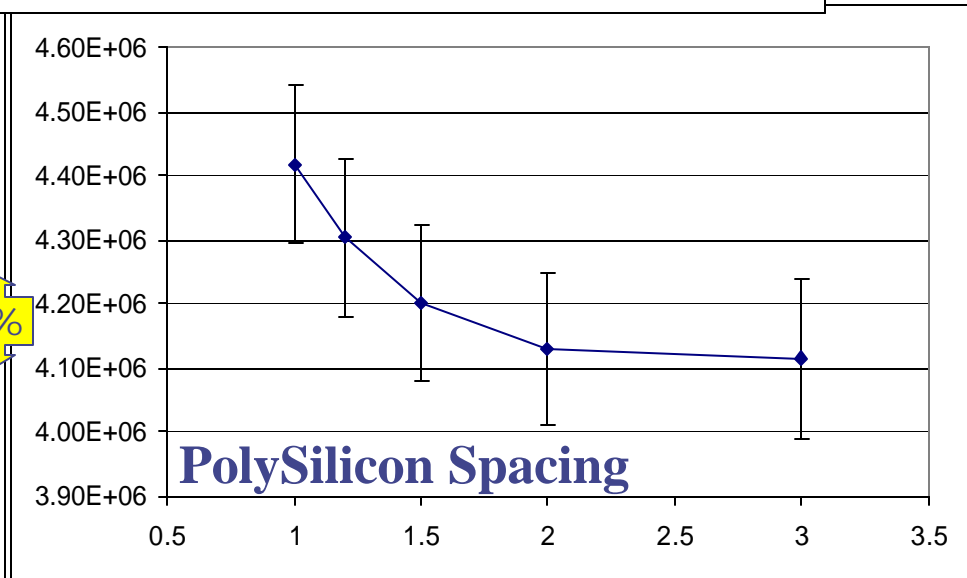
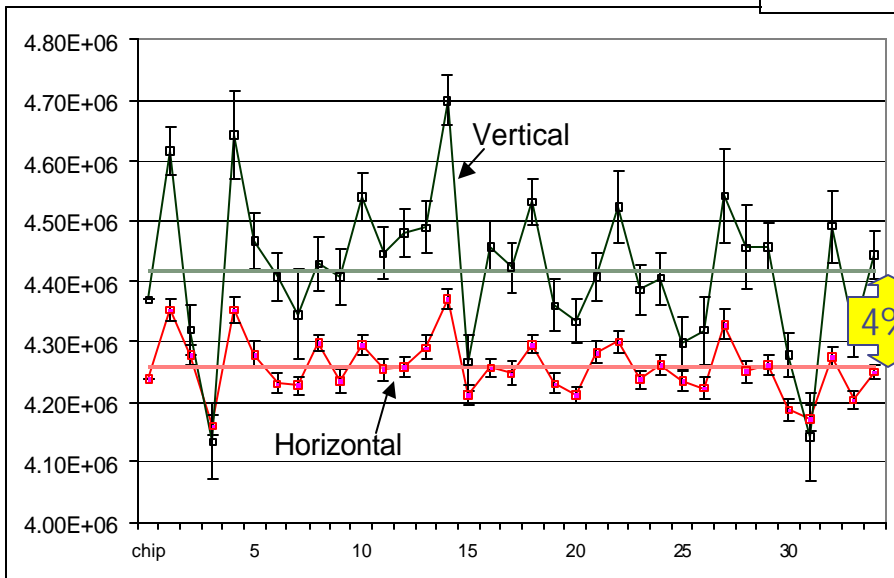
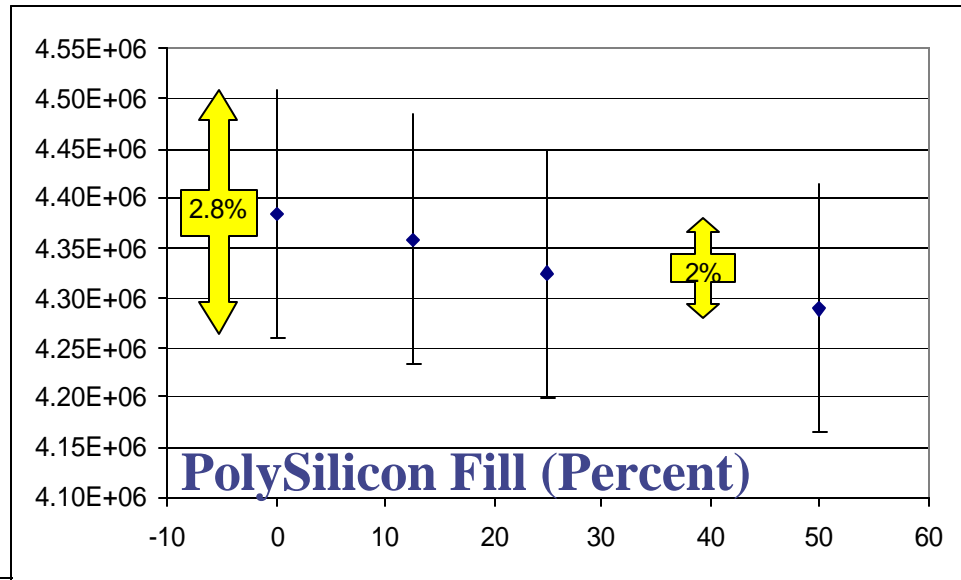


Process Line

# Modeling of Variability

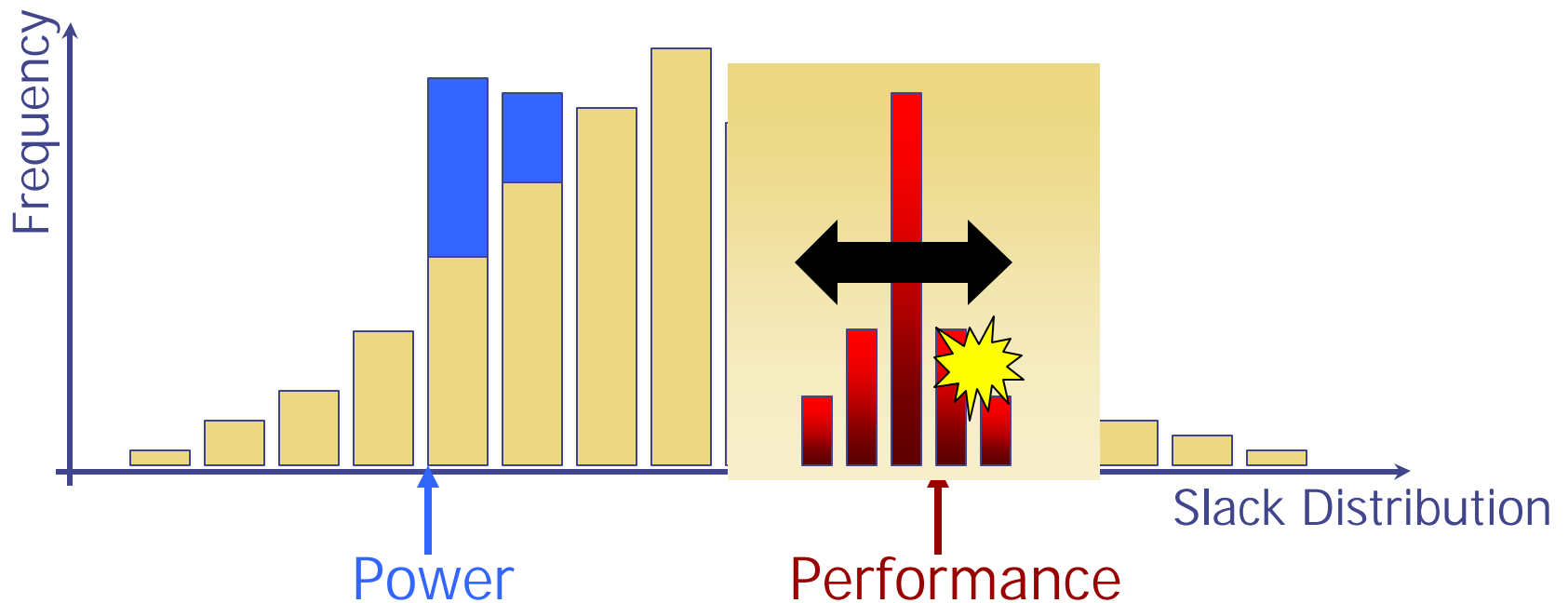
- ◆ Pre-PD vs. Post-PD are very different.
- ◆ Example: floor-plan location and power estimates can provide precise  $V_{DD}$  and T allowing potential correction.
- ◆ Pre-PD can only dealt with using worst-case analysis!

# Magnitude... Systematic Effects



# Design Factors

- ◆ Power and leakage constraints are driving designers to decrease overall path delay variability.
- ◆ This decrease results in more susceptibility to variability-induced timing fluctuations.



# Specific Questions/Answers

- ◆ Where should timing robustness be stressed?
  - At the technology mapping level and below.
- ◆ Is variability really a problem?
  - Duh...
- ◆ How much tolerance is needed?
  - 30%
- ◆ How well do current techniques do?
  - OK for die-to-die, badly for within-die.
- ◆ What phenomena do we need to consider?
  - Physical and Environmental impact on delay.