CSEE 4840 Room EQ Correction

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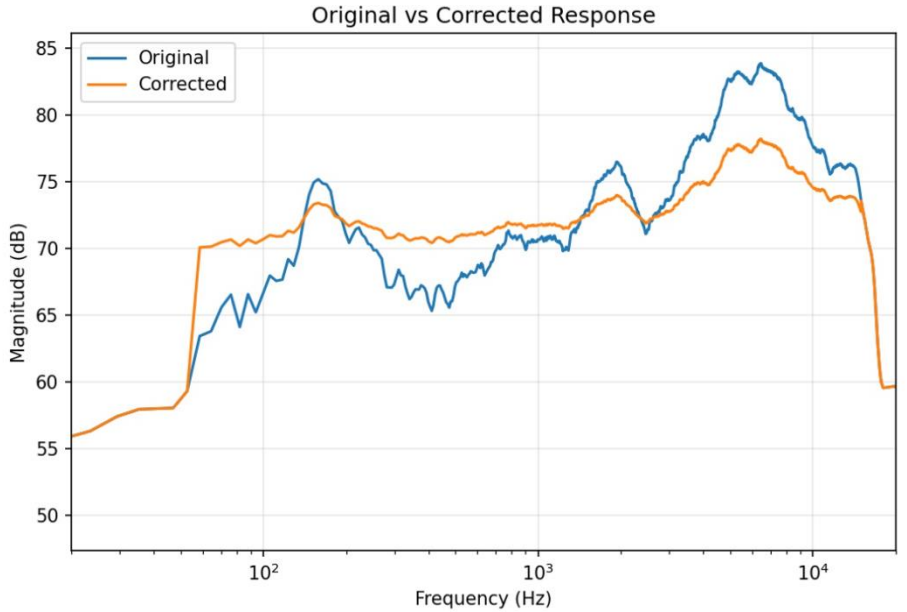
The Problem

- **Every room colors the sound inside it**, affecting the listening experience…
  - Specific frequencies are canceled while others are boosted.
  - Speaker placement alters the stereo image, creating poor soundstage.
  - Too much absorptive materials can make audio sound dull.
- **Our Goal**
  - Use the DE1-SoC to:
    - Measure a room's frequency response.
    - Generate a compensating FIR filter.
    - Output filter taps for downstream use.



Project Overview

Play log sine sweep
60 Hz – 20 kHz

→

Capture room response
via microphone

→

FPGA converts to
frequency domain

↓

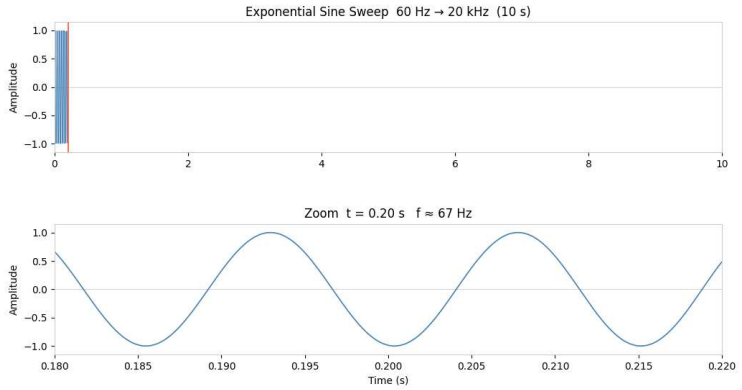
Compute correction
curve in software

←

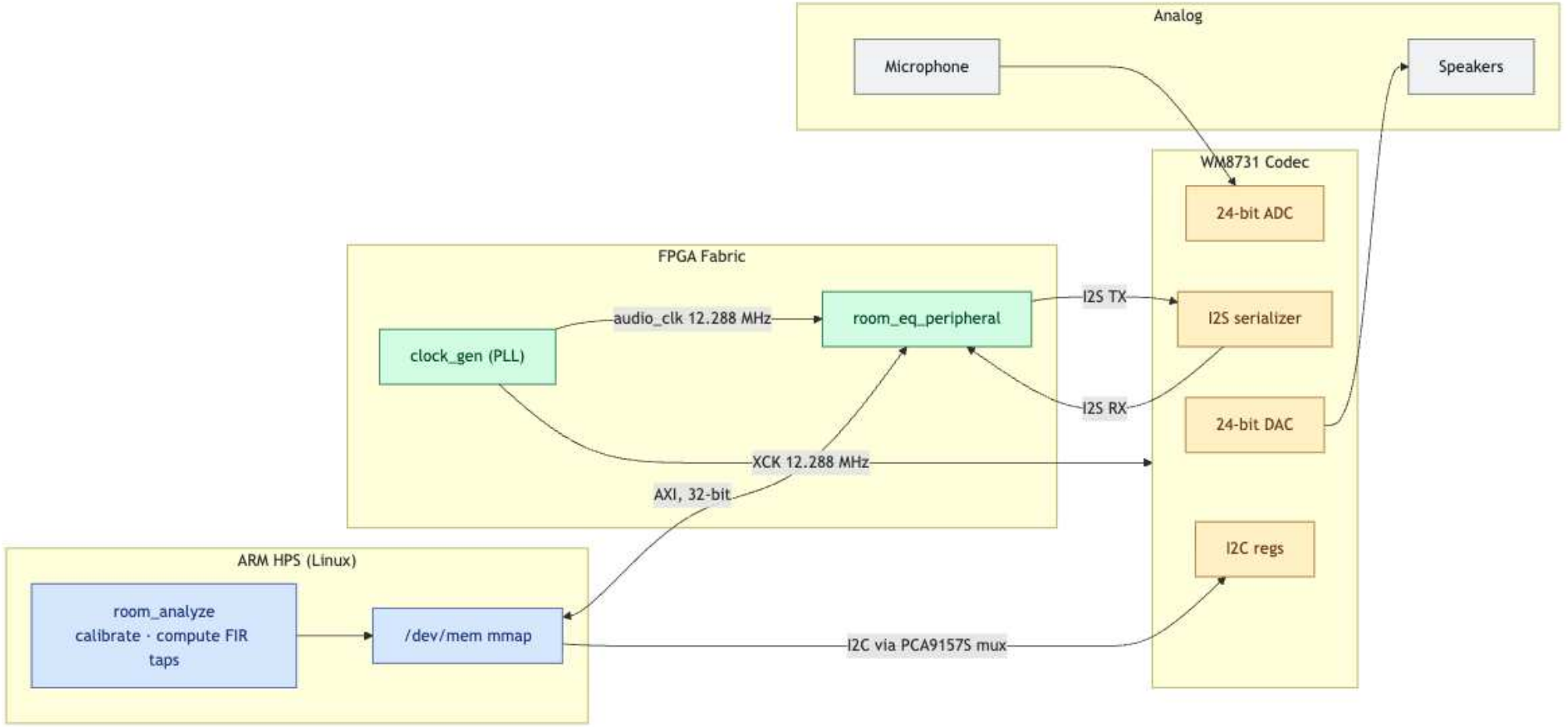
Generate FIR filter
coefficients

←

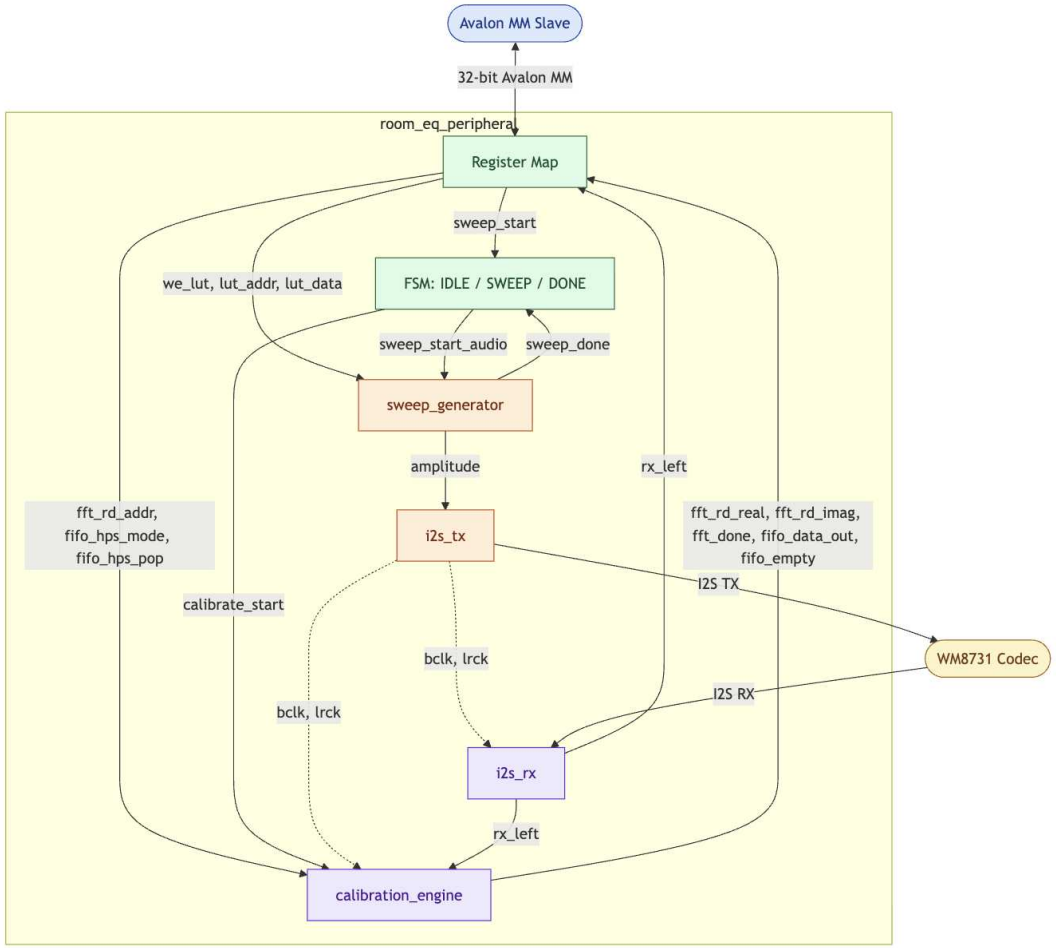
Export tap coeffs
to CSV file

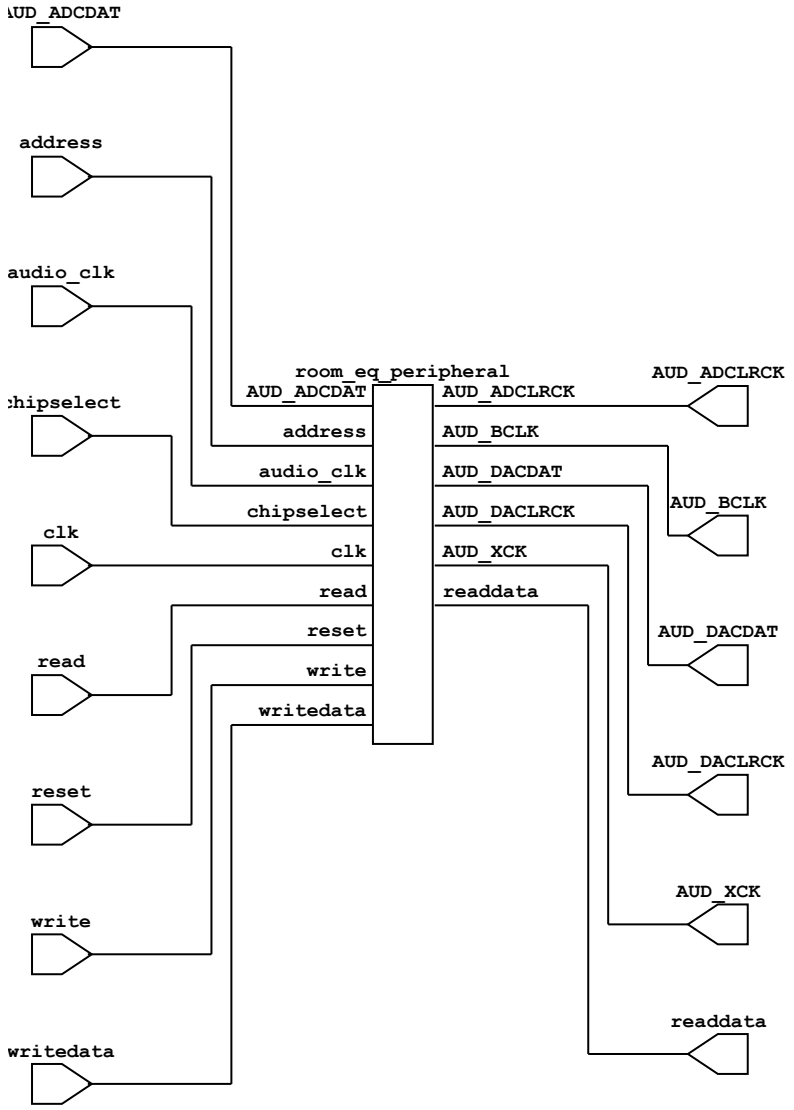


System Architecture



Room EQ Peripheral

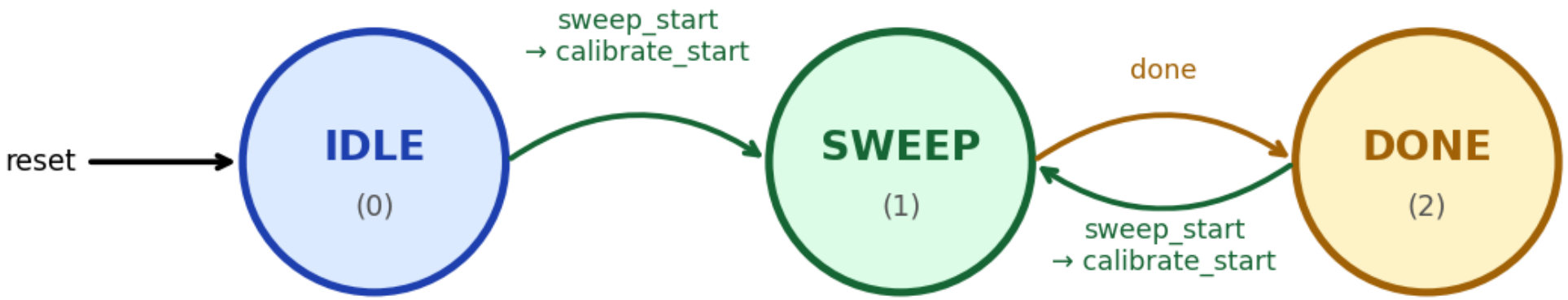




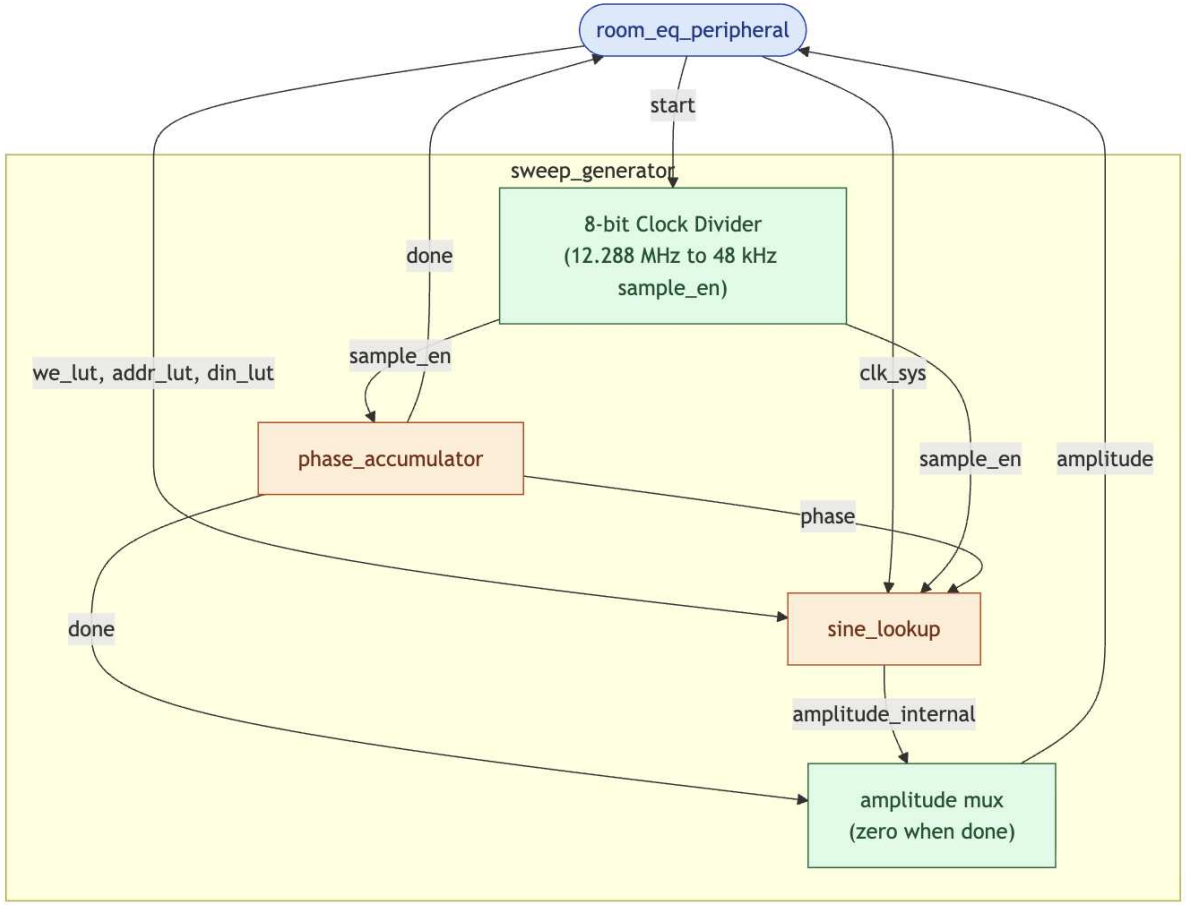
Room EQ Peripheral Register Map

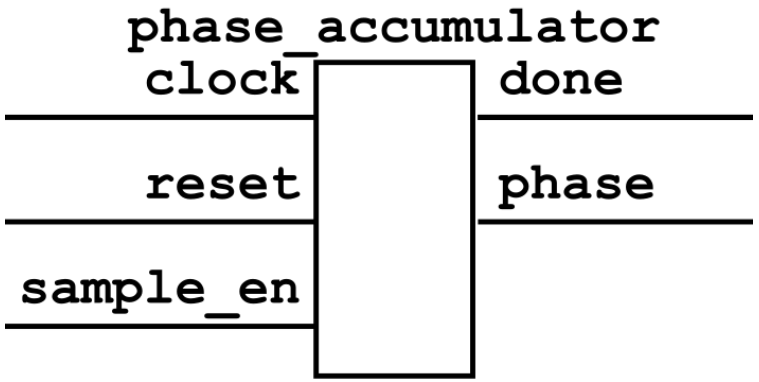
Offset	Bits	Access	Name	Description
0	[0]	W	CTRL	sweep_start
0	[1]	R/W	CTRL	fifo_hps_mode
1	[3:0]	R	STATUS	FSM state
1	[4]	R	STATUS	fft_done
1	[5]	R	STATUS	fifo_empty
3	[31:0]	R	VERSION	Hardware version
4	[9:0]	W	LUT_ADDR	Write address for sine LUT initialization
5	[23:0]	W	LUT_DATA	Write data for sine LUT
6	[12:0]	R/W	FFT_ADDR	Read address into FFT result RAM
7	[23:0]	R	FFT_RDATA	Real part of FFT bin at FFT_ADDR
8	[23:0]	R	FFT_IDATA	Imaginary part of FFT bin at FFT_ADDR
9	[23:0]	R	ADC_LEFT	Latest left-channel sample from I2S RX
10	[23:0]	R	FIFO_RDATA	Pop-on-read from sample FIFO

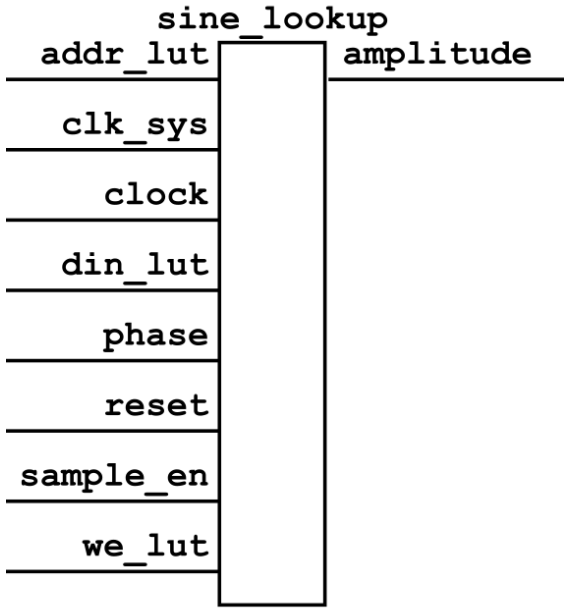
Room EQ Peripheral FSM



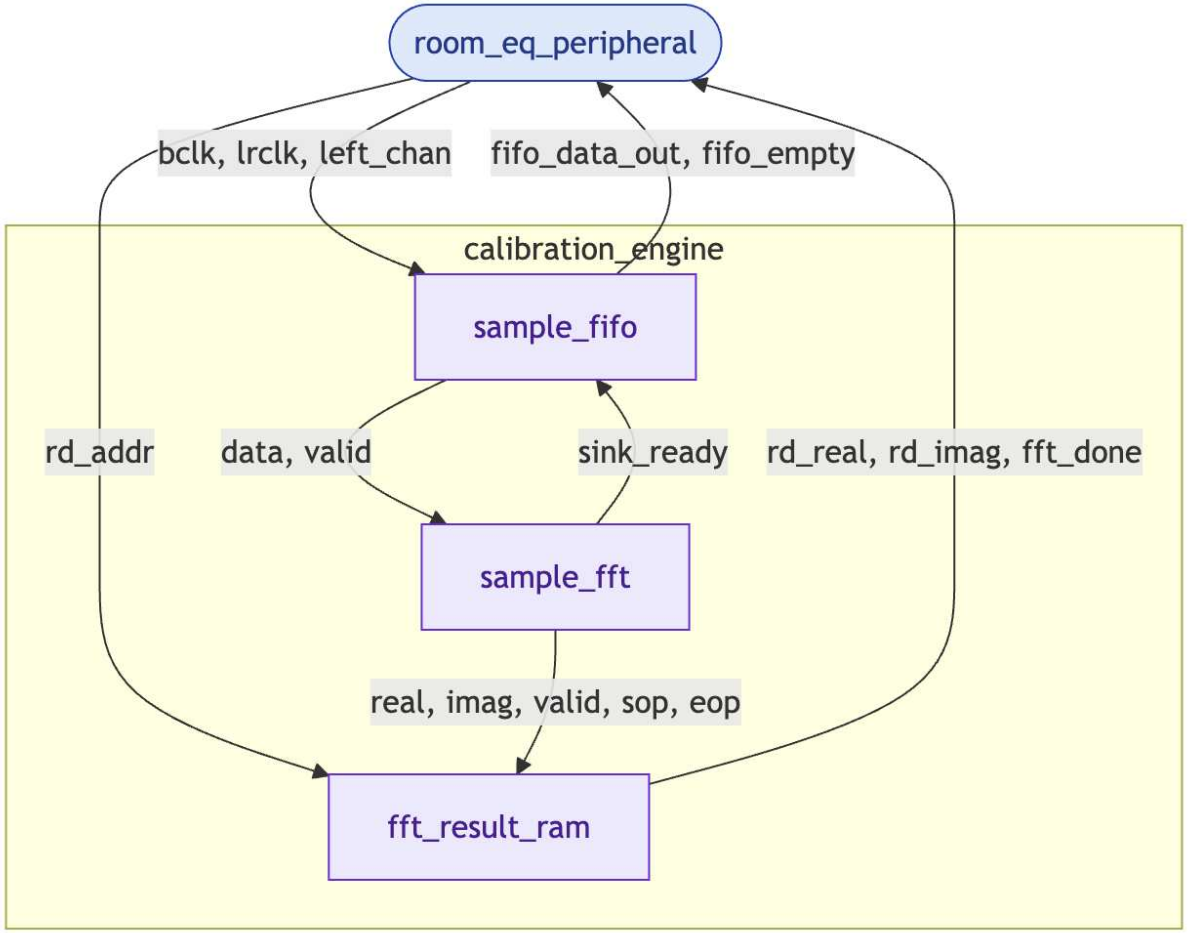
Sweep Generator



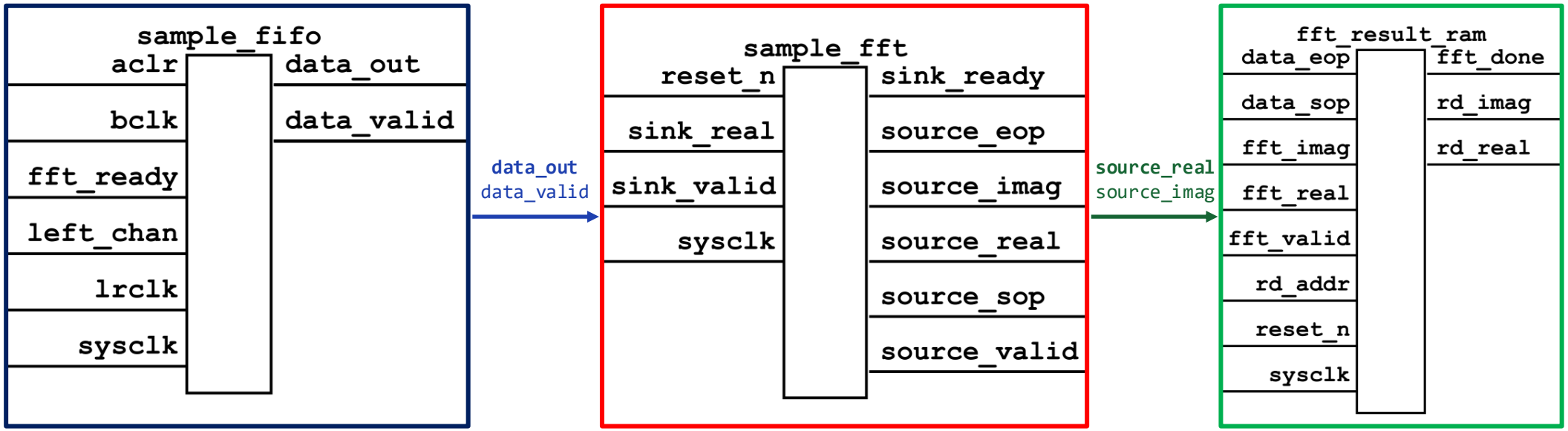




Calibration Engine



Calibration Engine Submodules



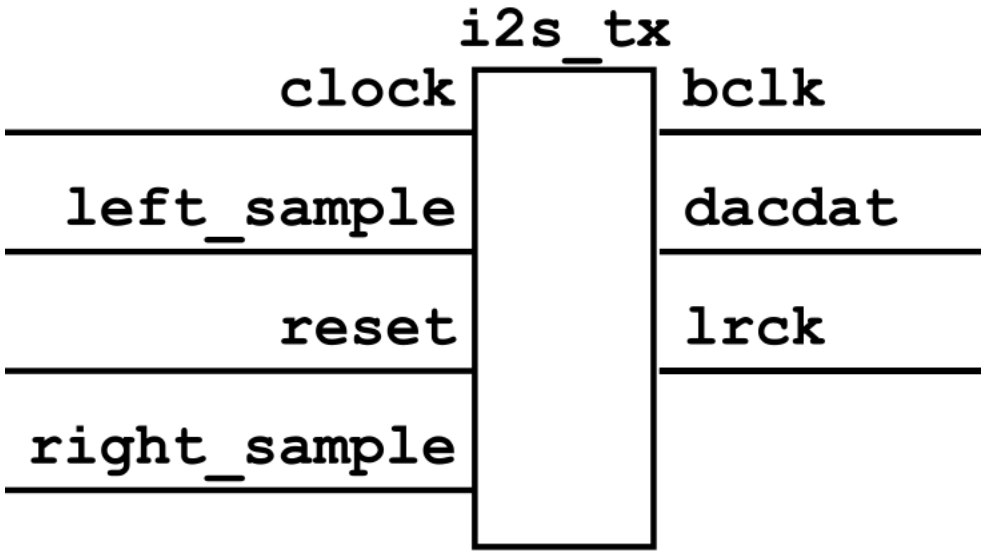
I2S TX

Inputs

- clock — 12.288 MHz PLL
- reset — Active-high reset
- left_sample — Signed 24-bit left channel sample
- right_sample — Signed 24-bit right channel sample

Outputs

- bclk — 3.072 MHz bit clock → AUD_BCLK
- lrck — 48 kHz frame clock → AUD_DACLRCK
- dacdat — Serial data → AUD_DACDAT



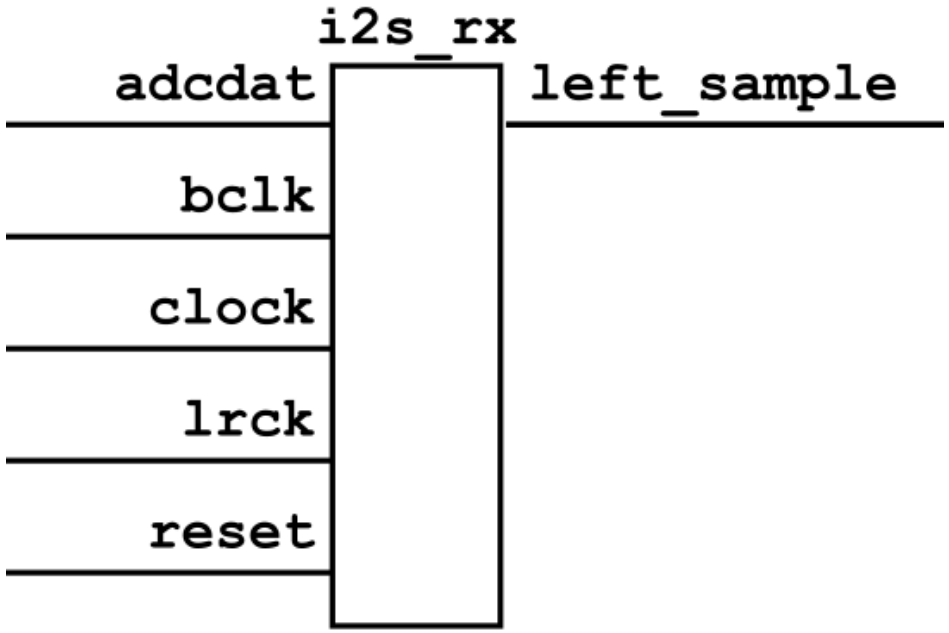
I2S RX

Inputs

- clock — 12.288 MHz PLL
- reset — Active-high reset
- bclk — 3.072 MHz bit clock from i2s_tx
- lrck — 48 kHz frame clock
- adcdat — Serial ADC data from codec

Outputs

- left_sample — Deserialized left channel

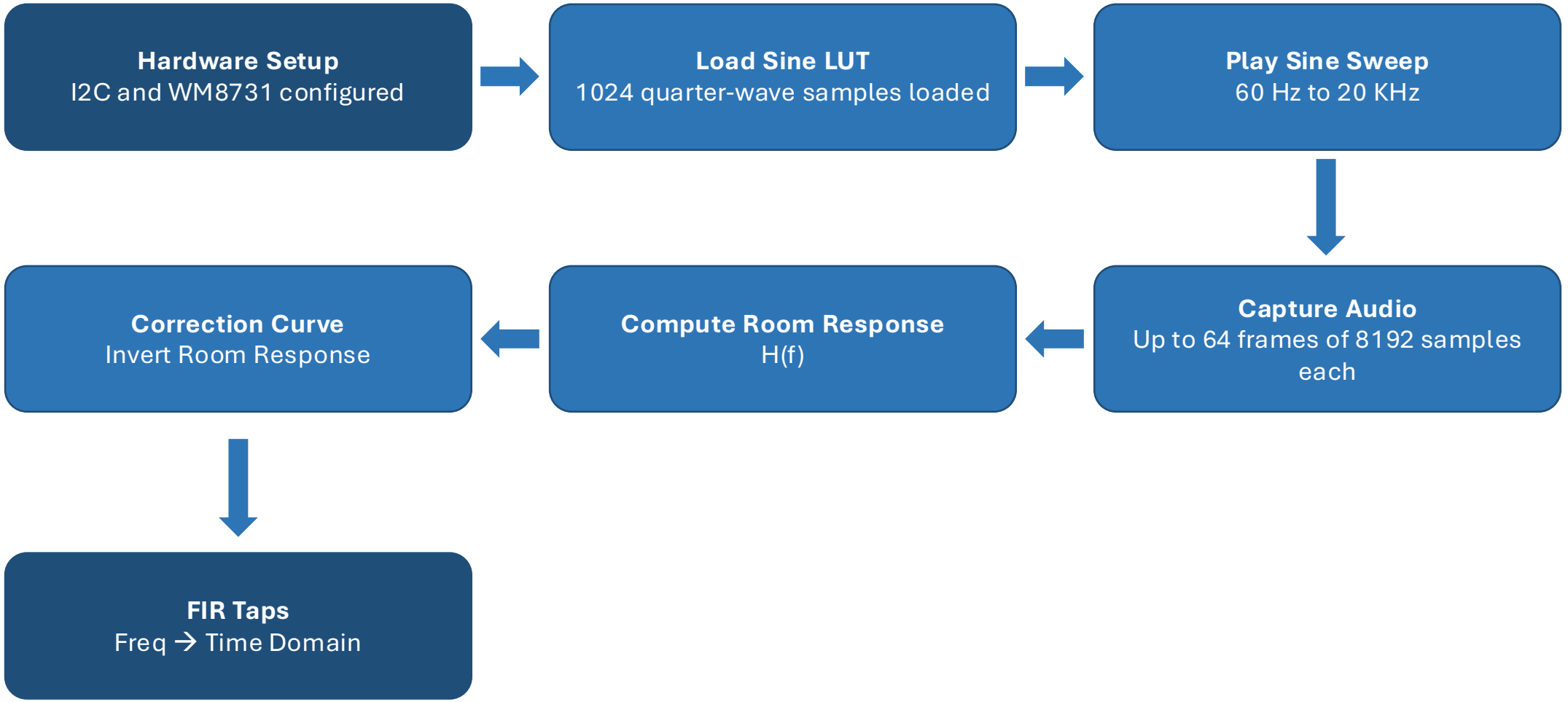


HPS Software Interface

Pointer	Offset	Physical Base	Target
`i2c_base`	`0x0000`	`0xFF200000`	Altera I2C (codec control)
`room_eq_base`	`0x2000`	`0xFF202000`	Room EQ peripheral register bank

- I2C and Room EQ Peripheral accessed via linux **/dev/mem**
- Lightweight HPS – FPGA Bridge
- 32 bit read/writes

HPS Software Pipeline



HPS Software Example

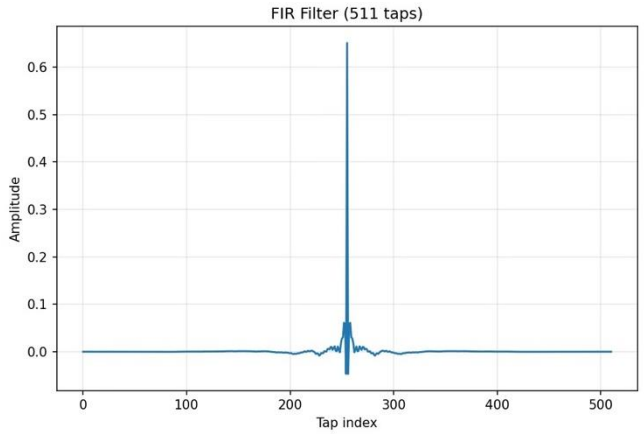
Compute Room Response
H(f)

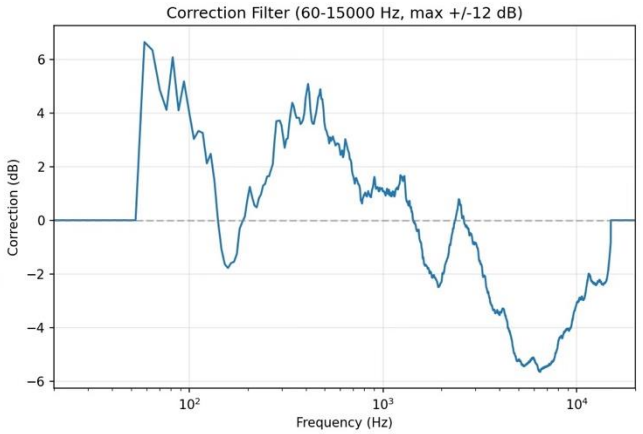
→

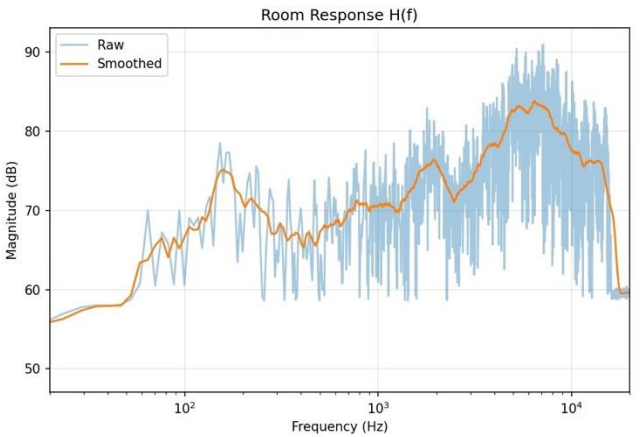
Correction Curve
Invert Room Response

→

FIR Taps
Freq → Time Domain







DEMO

```
module_exit(Thank_You);
```