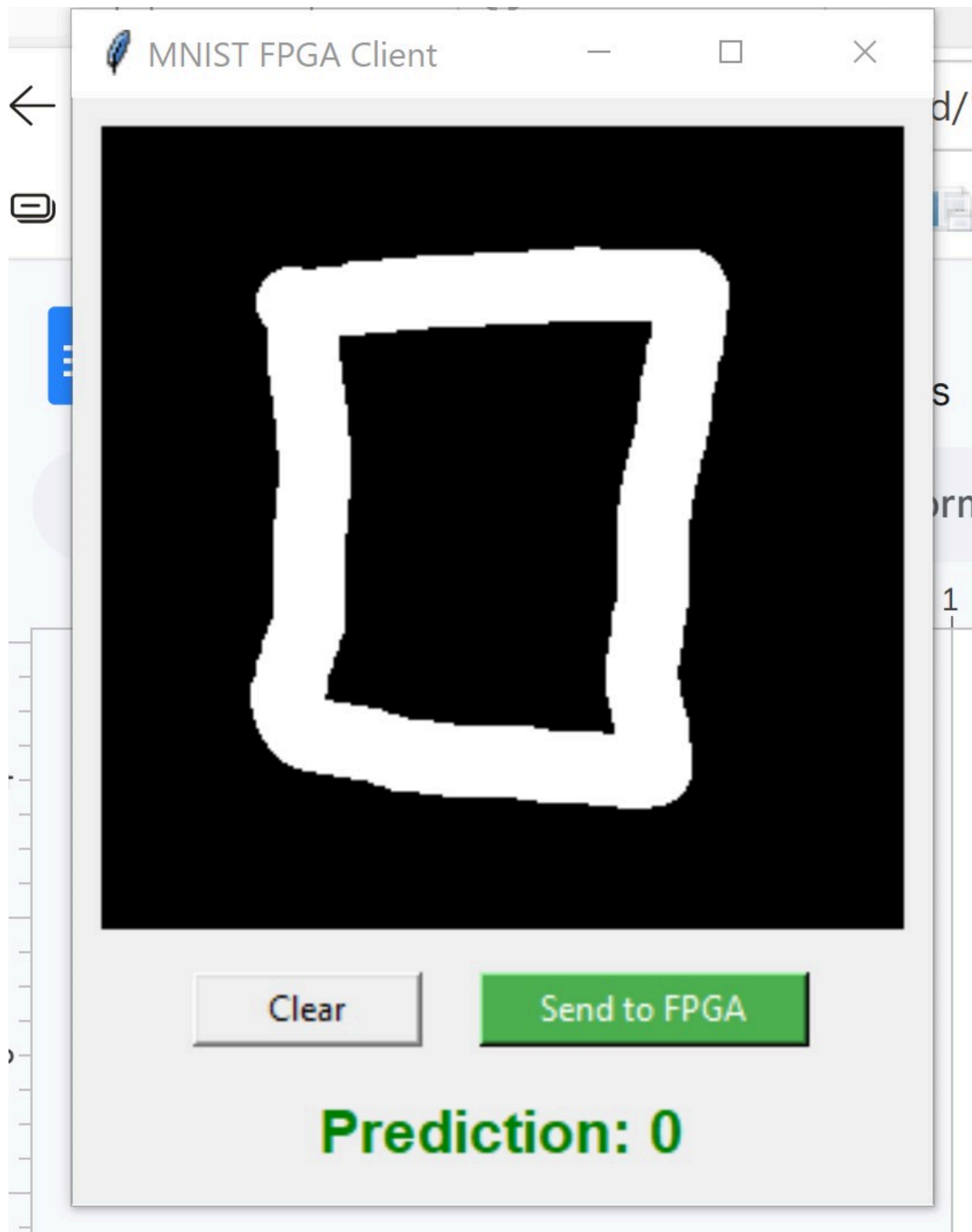
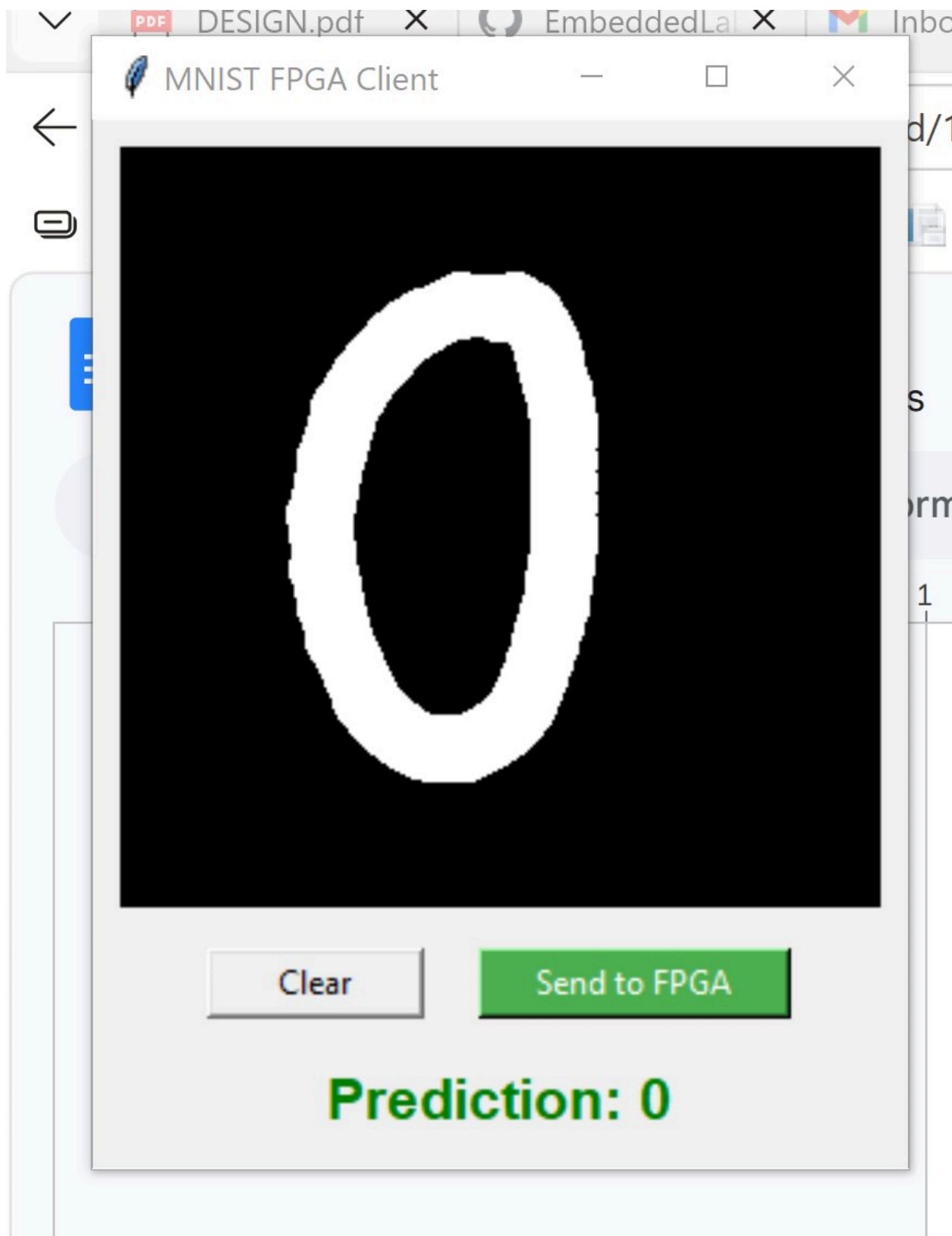
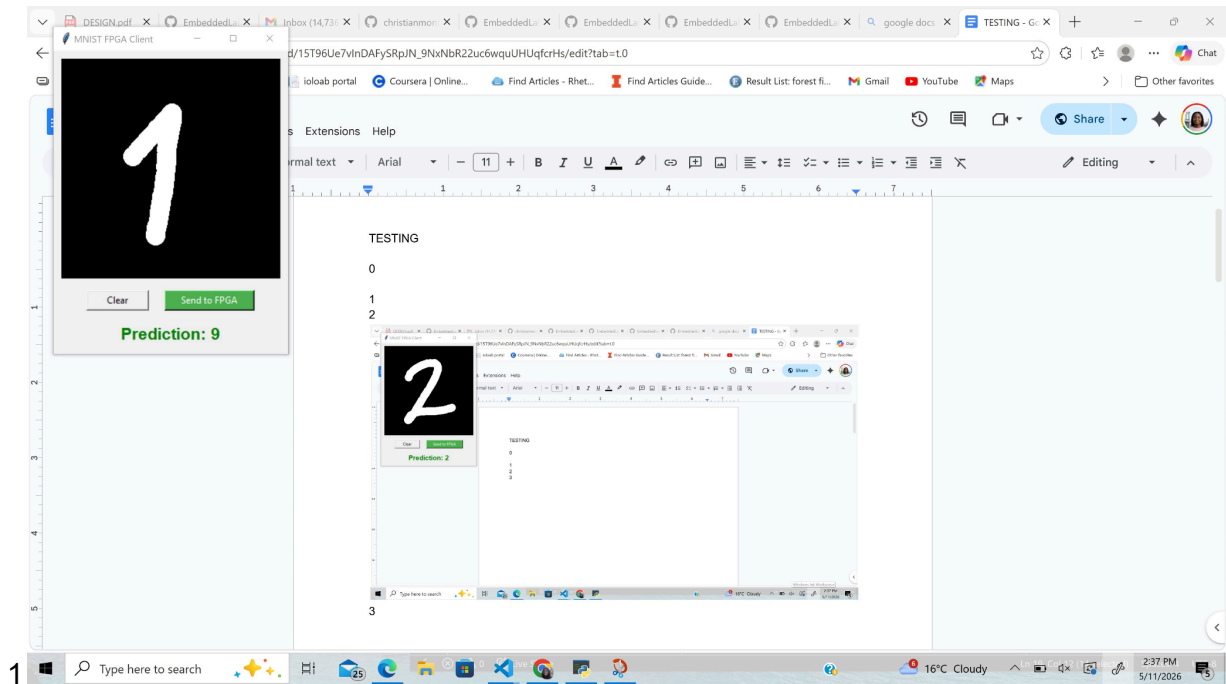


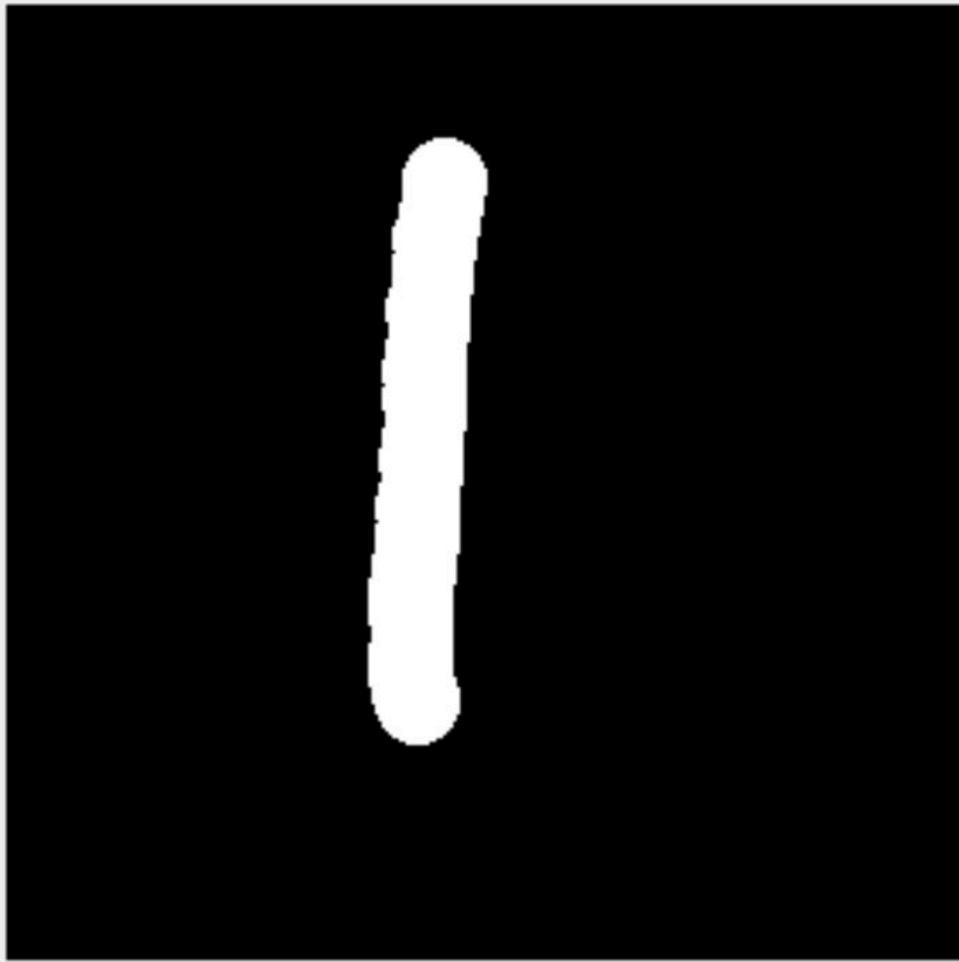
TESTING

0







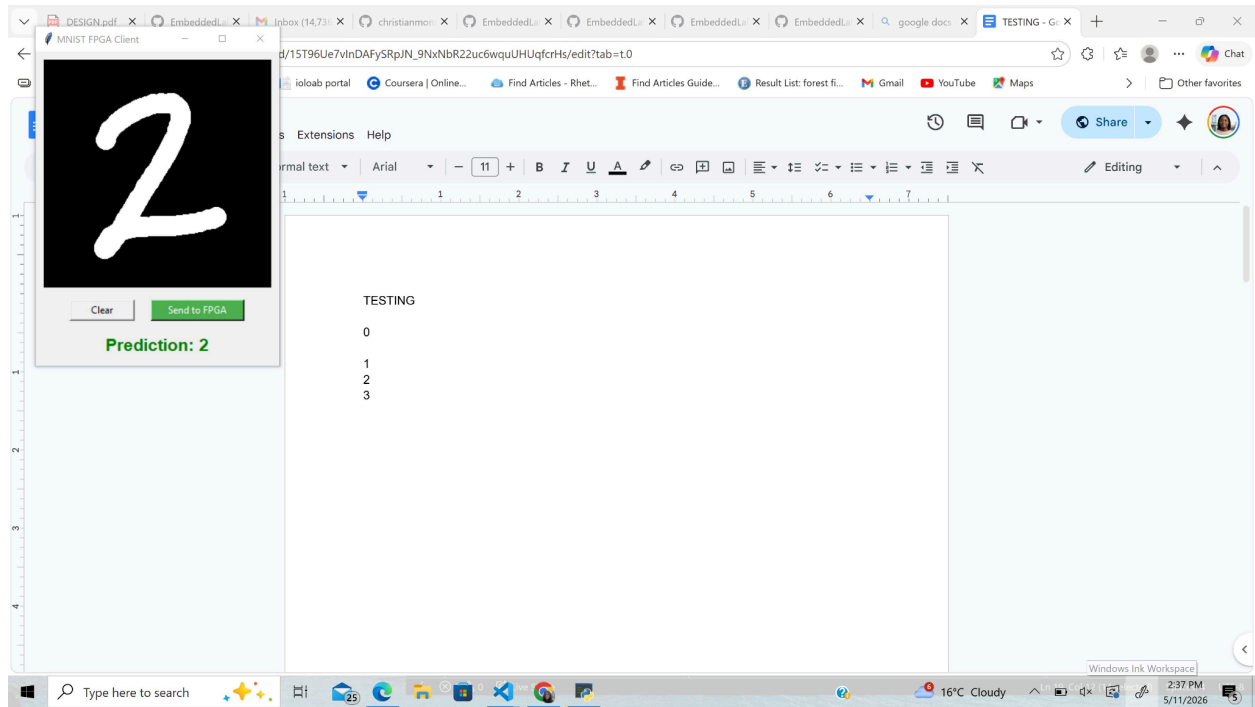


Clear

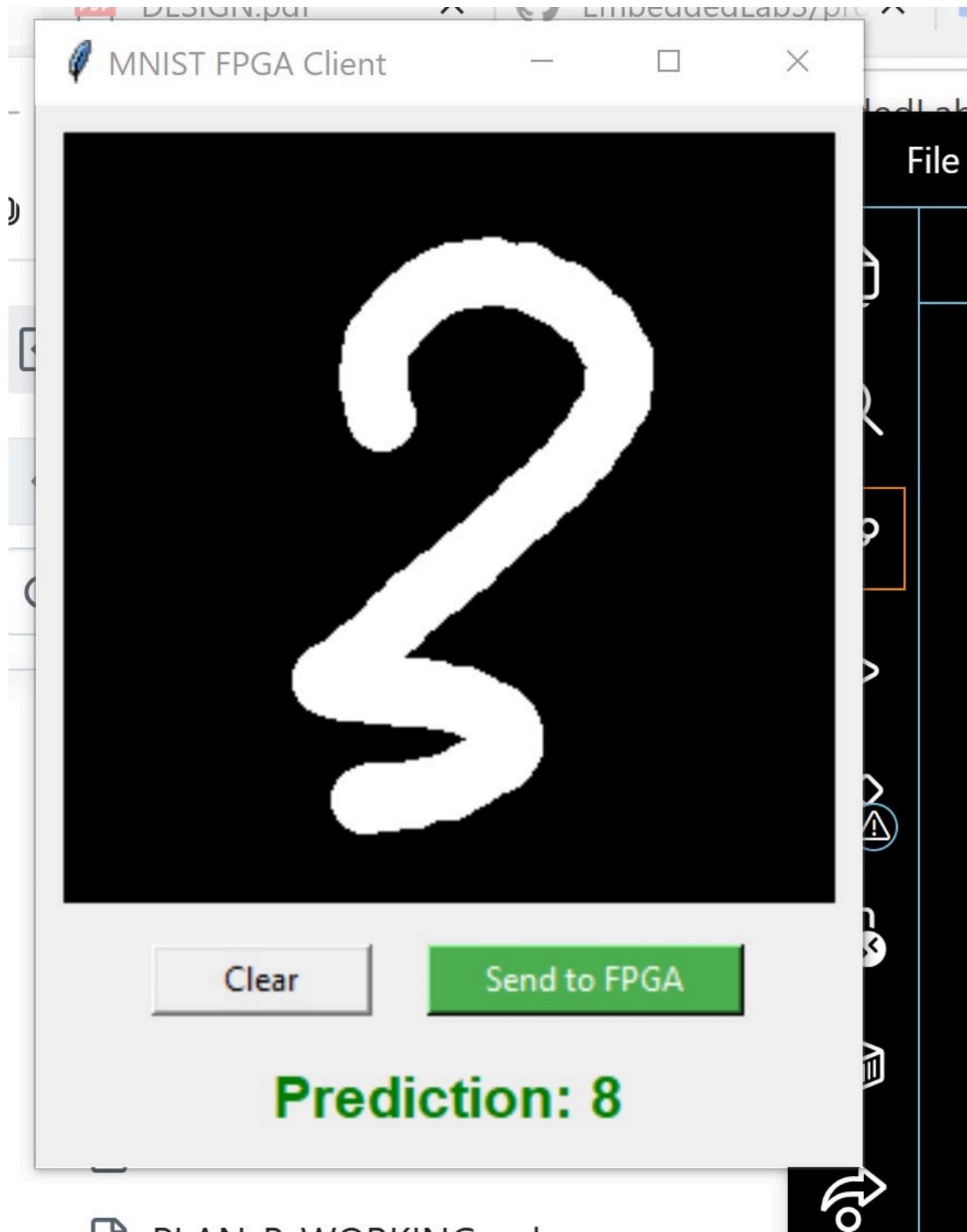
Send to FPGA

Prediction: 1

2



3





MNIST FPGA Client



Clear

Send to FPGA

Prediction: 9



MNIST FPGA Client



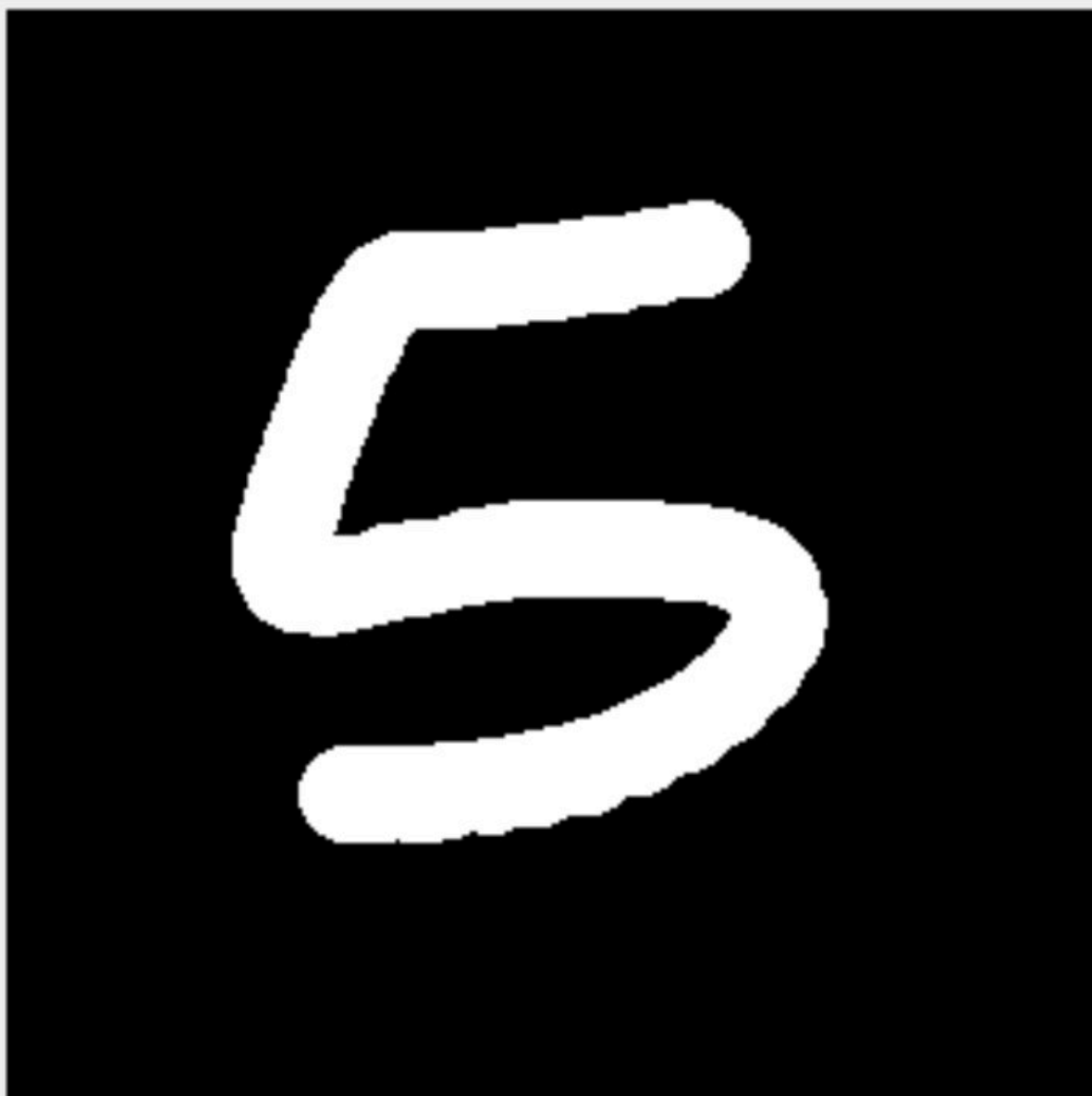
Clear

Send to FPGA

Prediction: 4



MNIST FPGA Client

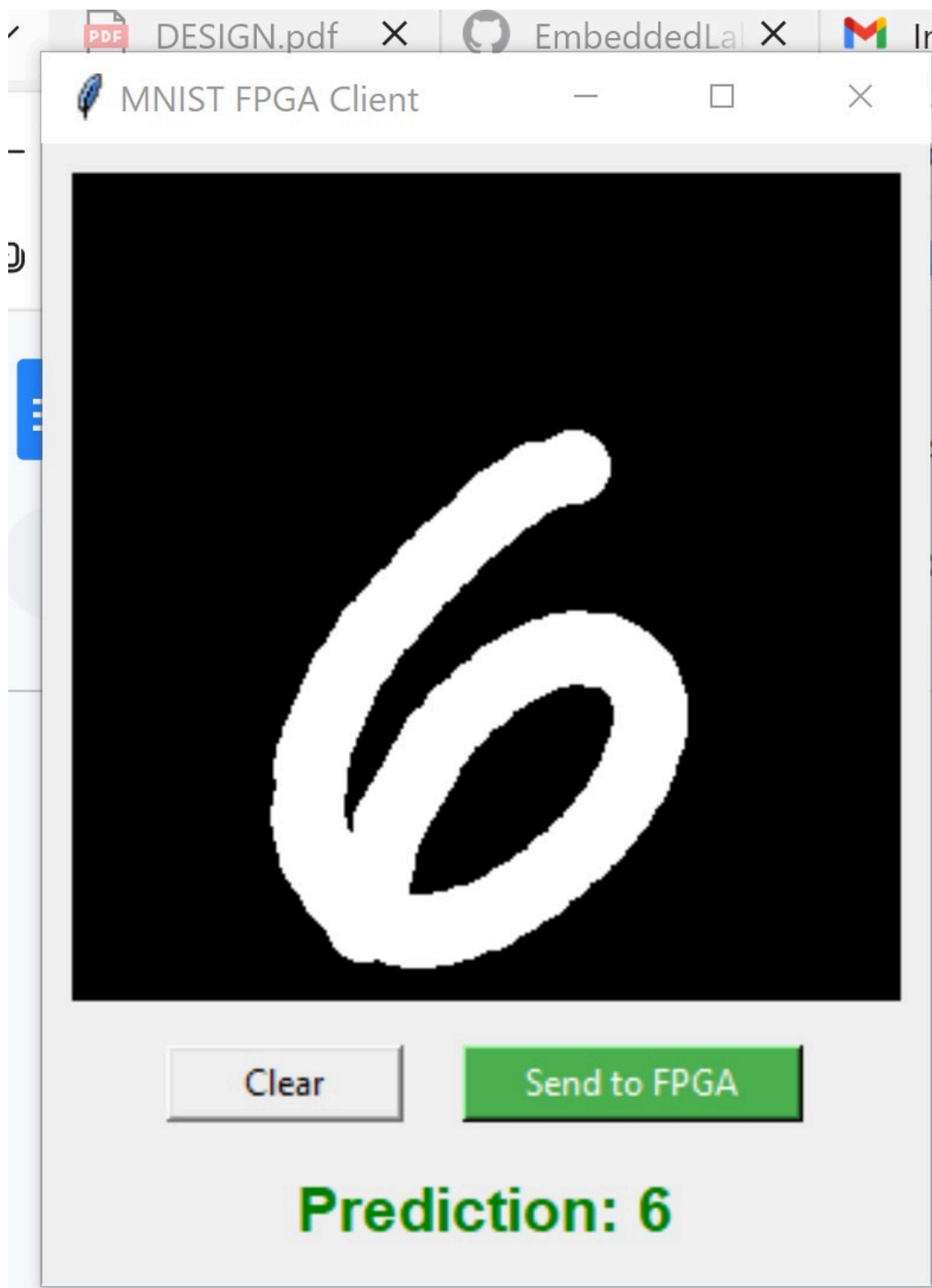


Clear

Send to FPGA

Prediction: 5









MNIST FPGA Client



Clear

Send to FPGA

Prediction: 7



MNIST FPGA Client



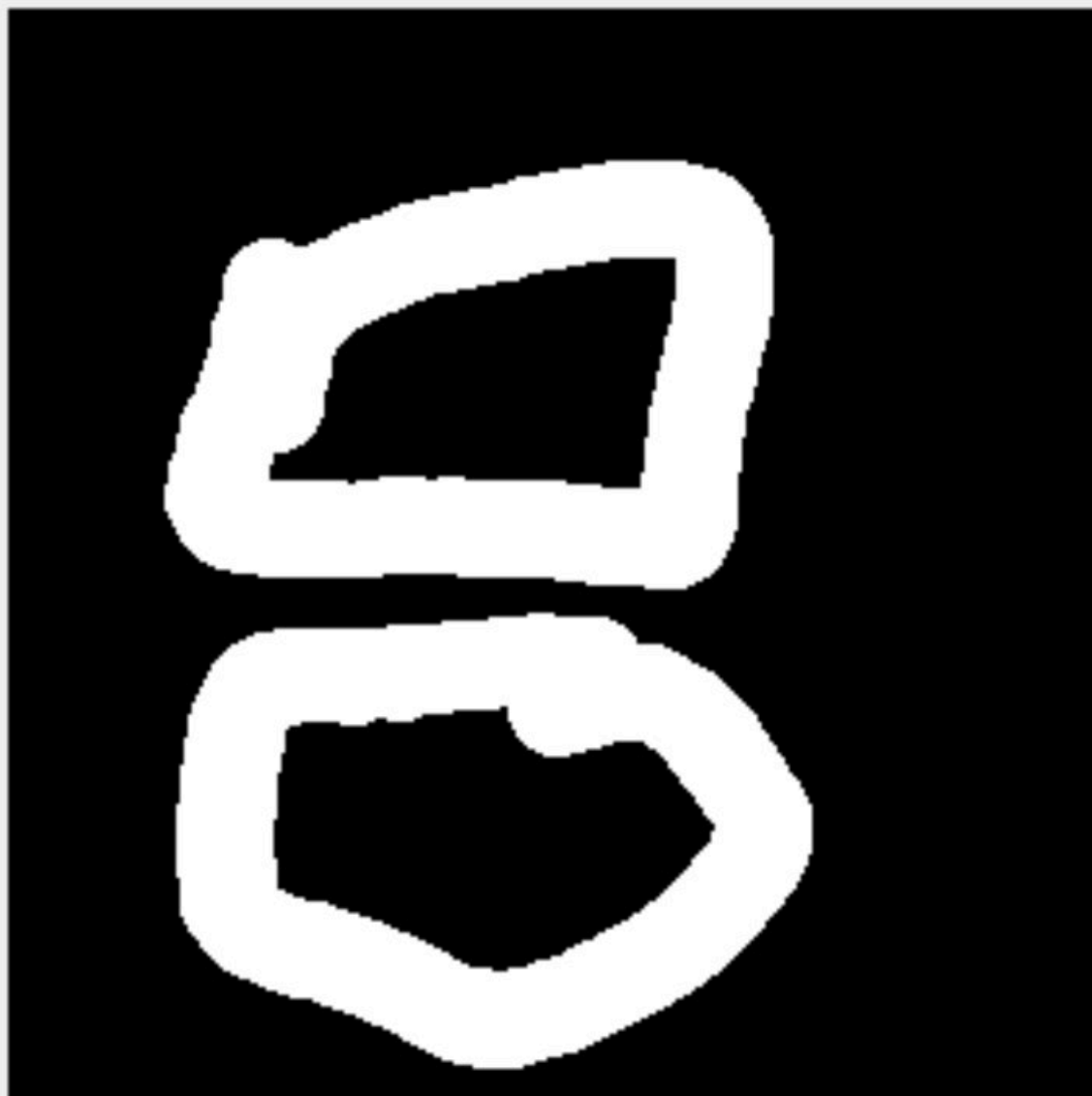
Clear

Send to FPGA

Prediction: 8



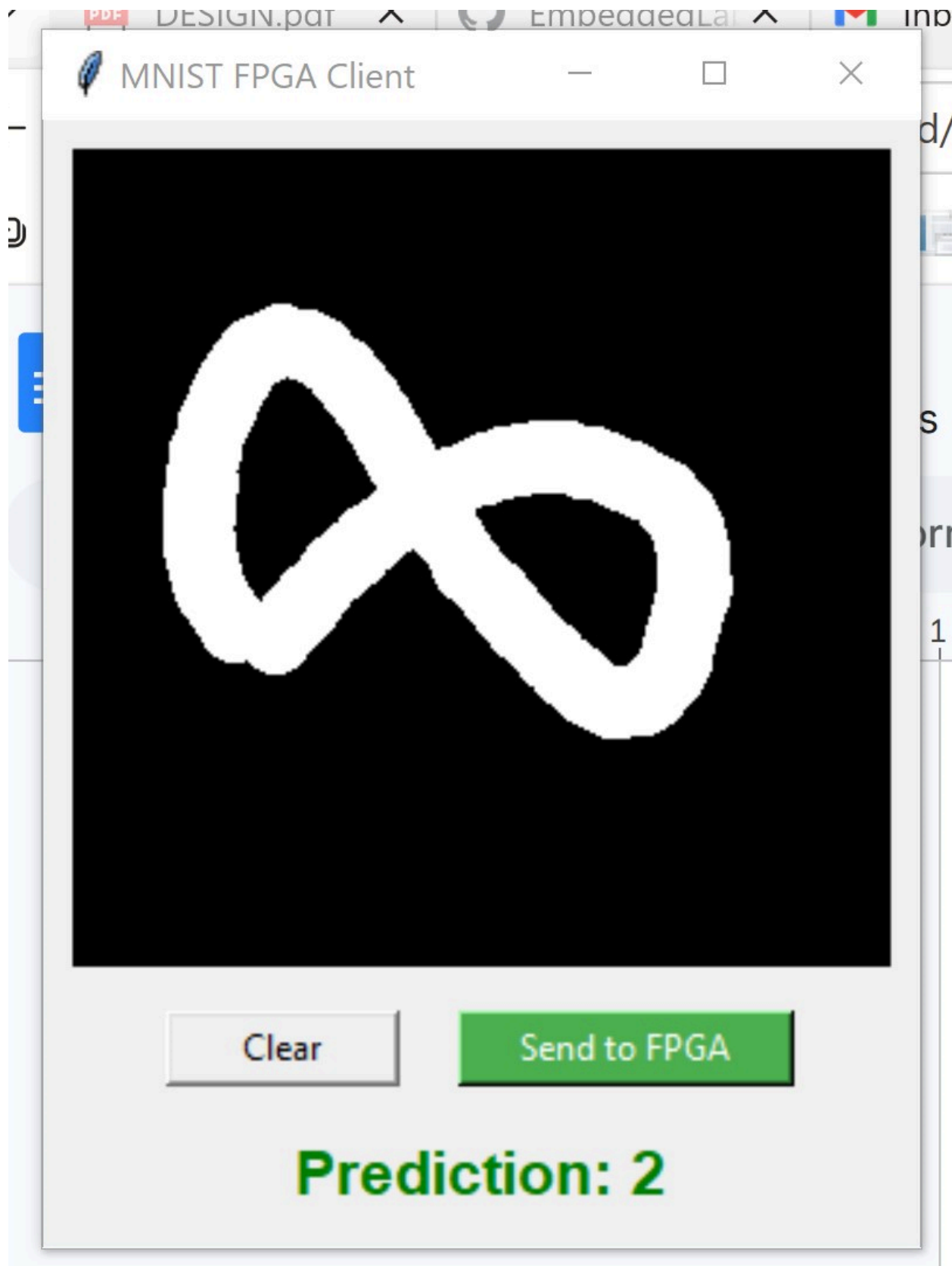
MNIST FPGA Client



Clear

Send to FPGA

Prediction: 8





MNIST FPGA Client



Clear

Send to FPGA

Prediction: 9



MNIST FPGA Client



Clear

Send to FPGA

Prediction: 9

