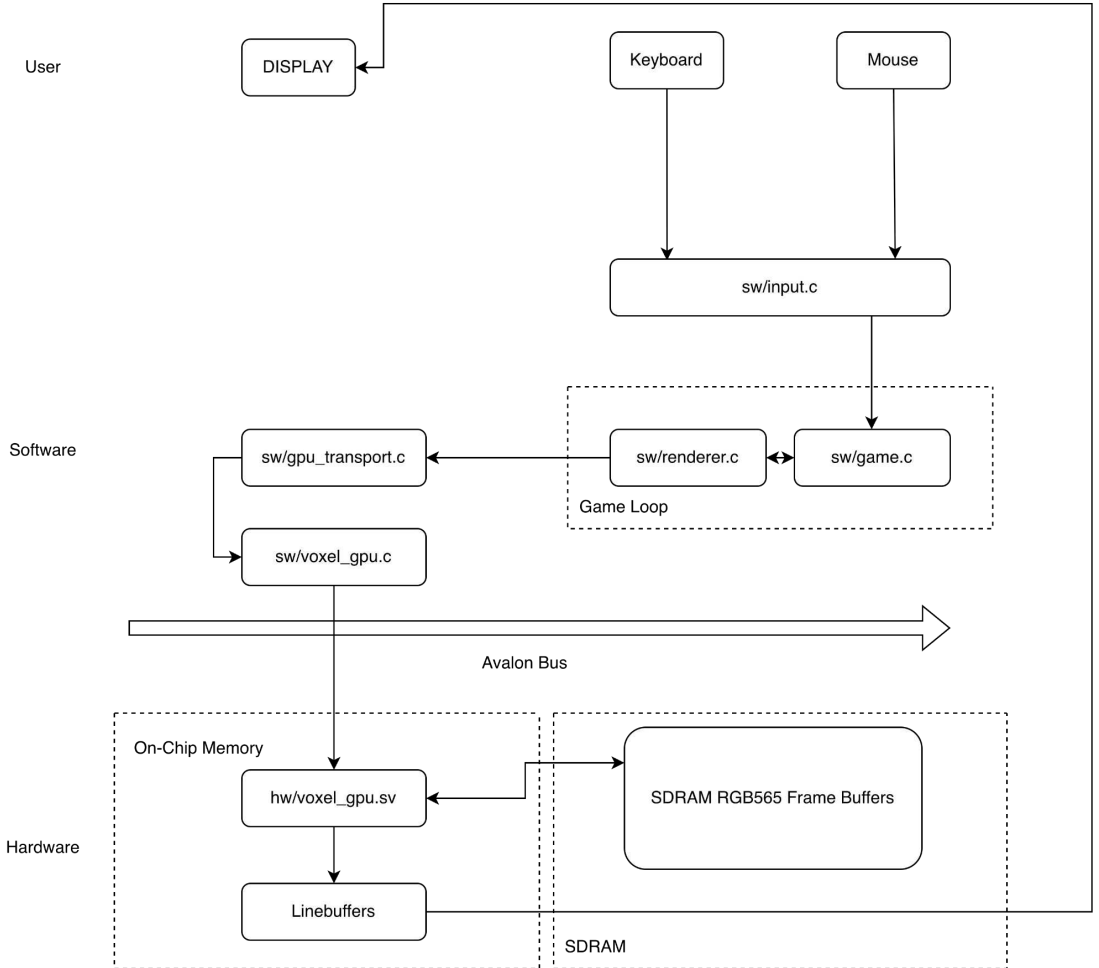
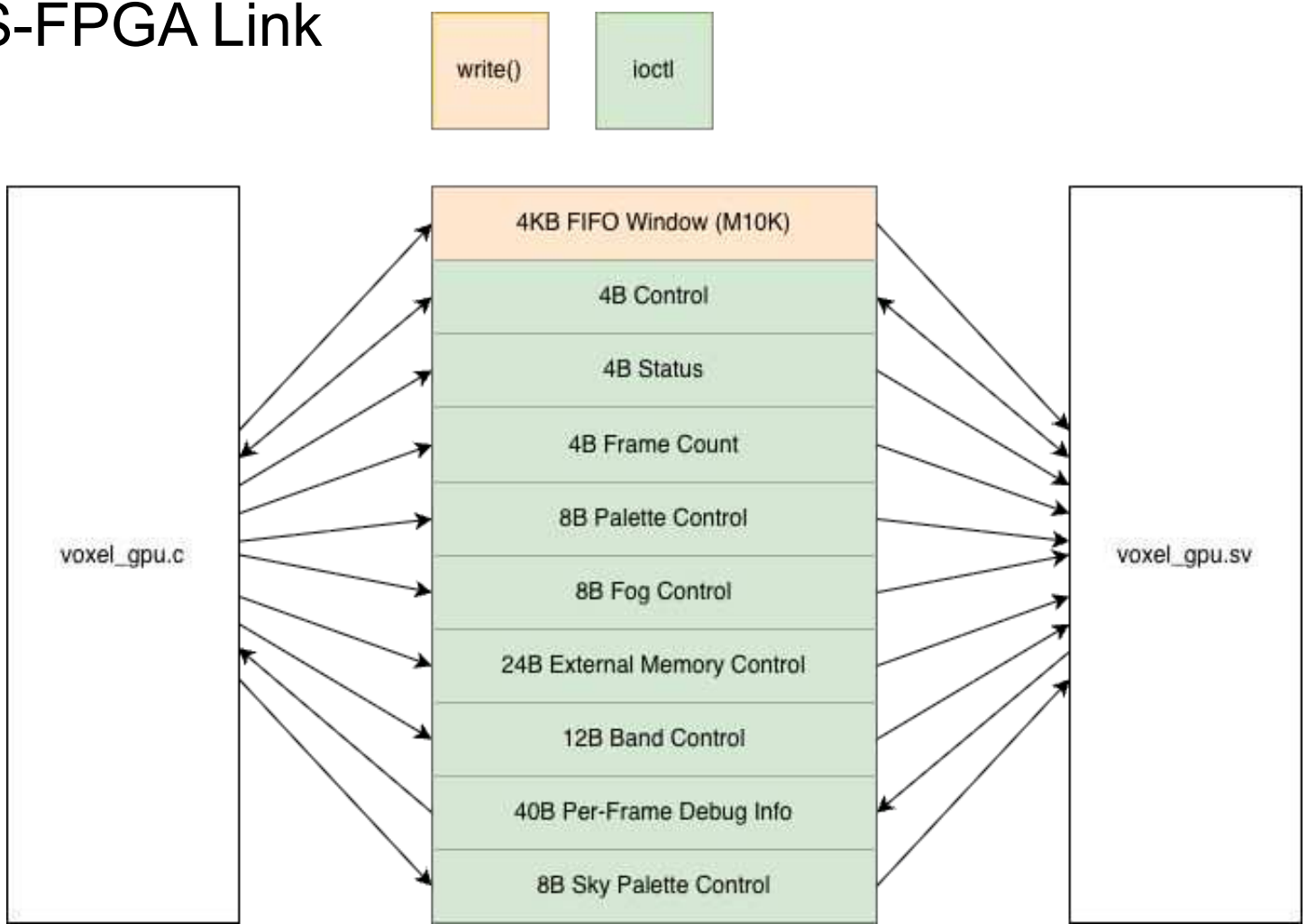

Block Game
by Mihir, Wesley, and Josh
1
2
3
4
5
6
7
8
9

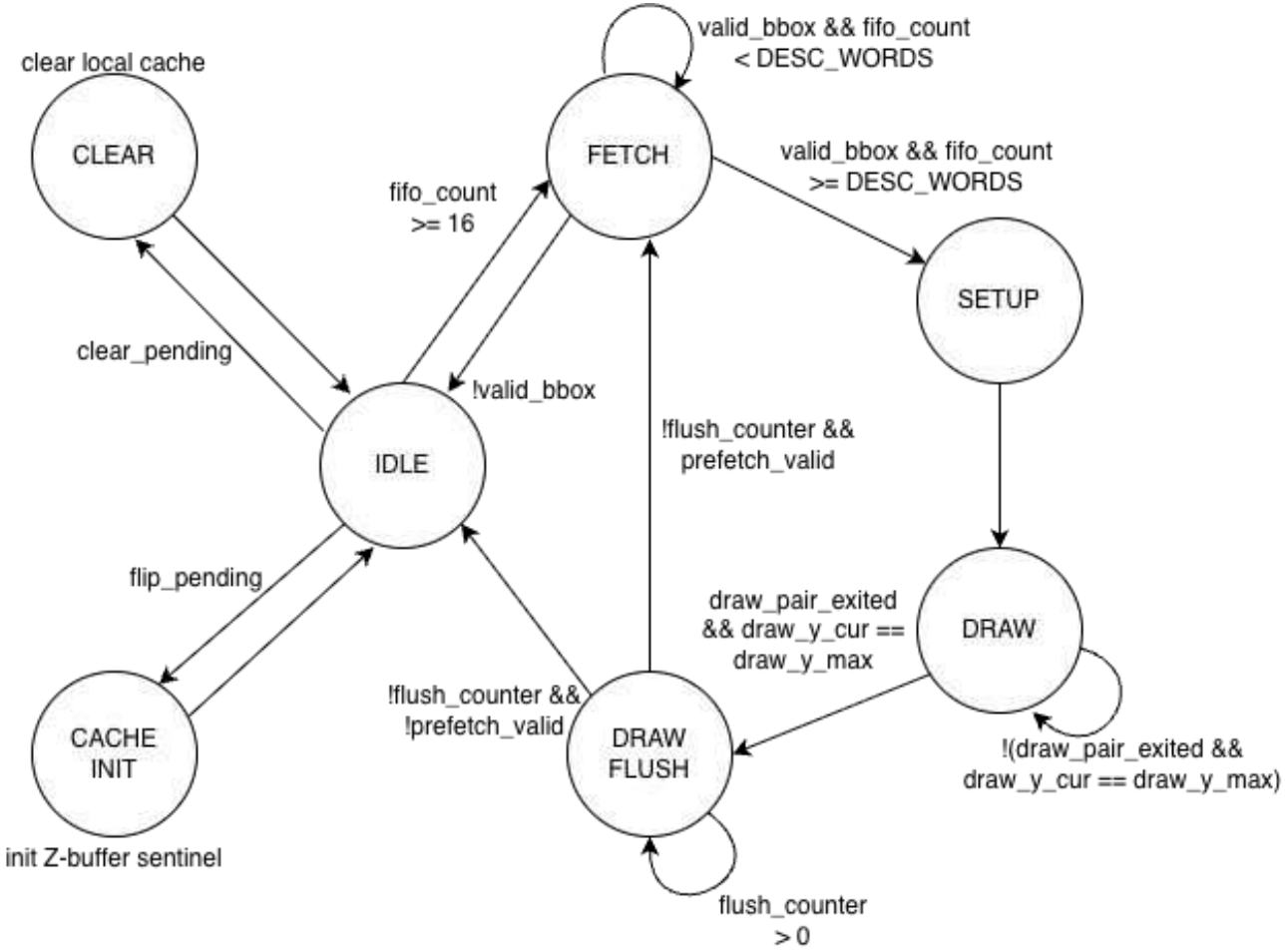
Program Overview - Block Diagram



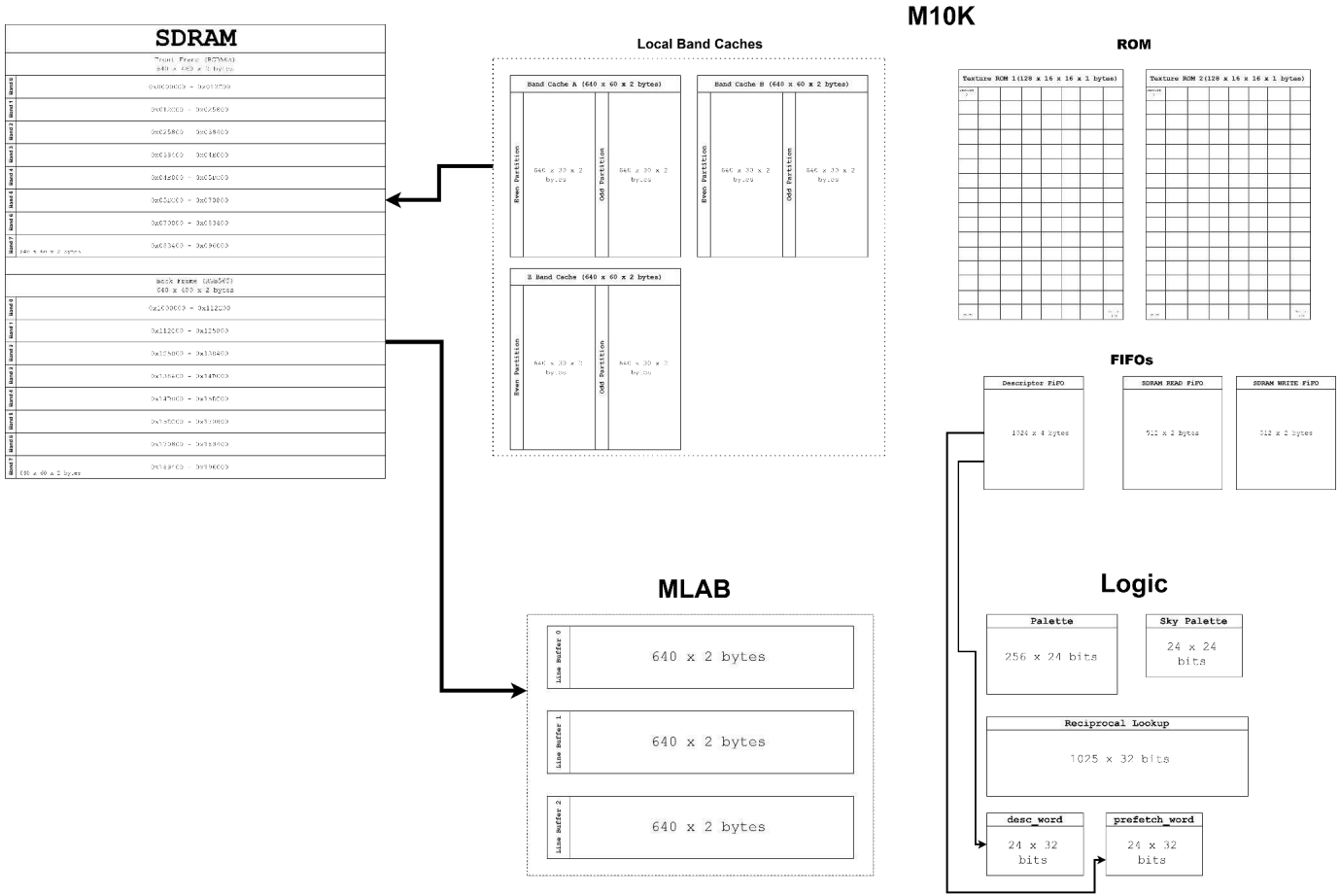
HPS-FPGA Link



Rasterizer Finite State Machine



Memory Layout



SDRAM

Front Frame (RGB565)
640 x 480 x 2 bytes

Band 0	0x0000000 - 0x012C00
Band 1	0x012C00 - 0x025800
Band 2	0x025800 - 0x038400
Band 3	0x038400 - 0x04B000
Band 4	0x04B000 - 0x05DC00
Band 5	0x05DC00 - 0x070800
Band 6	0x070800 - 0x083400
Band 7	0x083400 - 0x096000

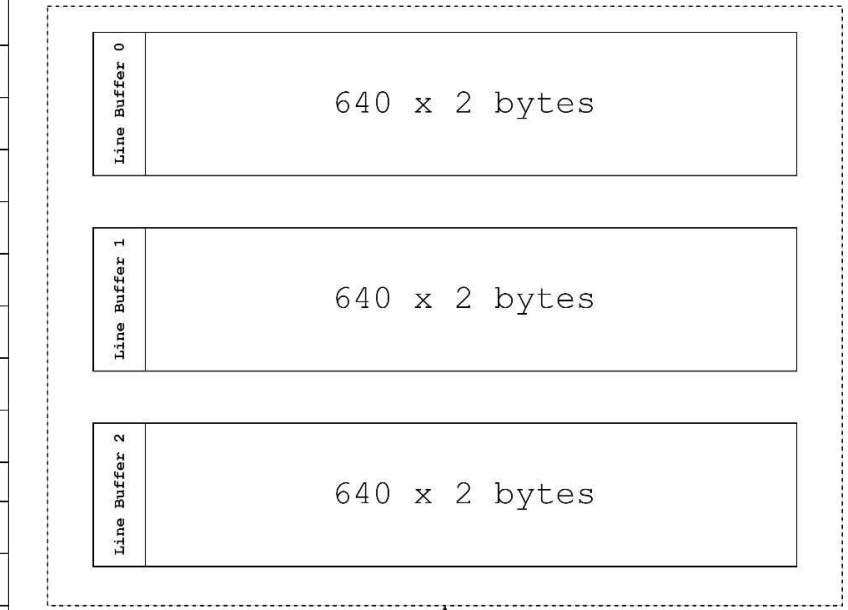
640 x 60 x 2 bytes

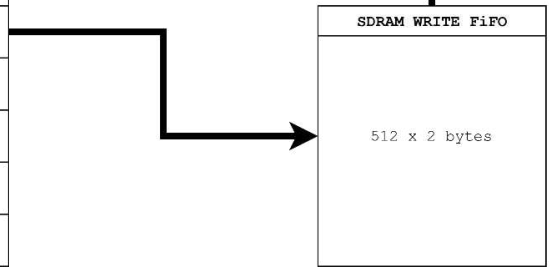
Back Frame (RGB565)
640 x 480 x 2 bytes

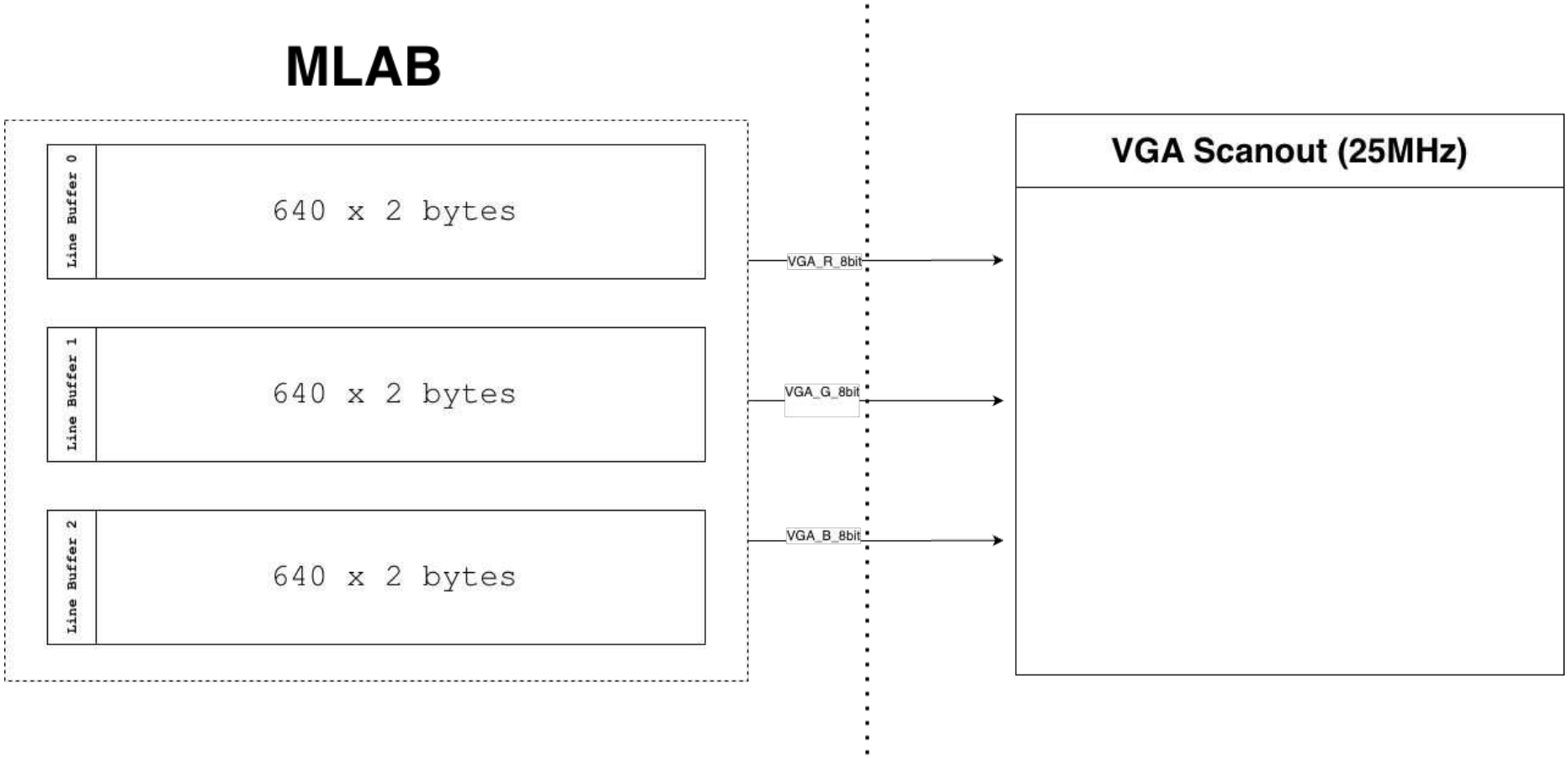
Band 0	0x1000000 - 0x112C00
Band 1	0x112C00 - 0x125800
Band 2	0x125800 - 0x138400
Band 3	0x138400 - 0x14B000
Band 4	0x14B000 - 0x15DC00
Band 5	0x15DC00 - 0x170800
Band 6	0x170800 - 0x183400
Band 7	0x183400 - 0x196000

640 x 60 x 2 bytes

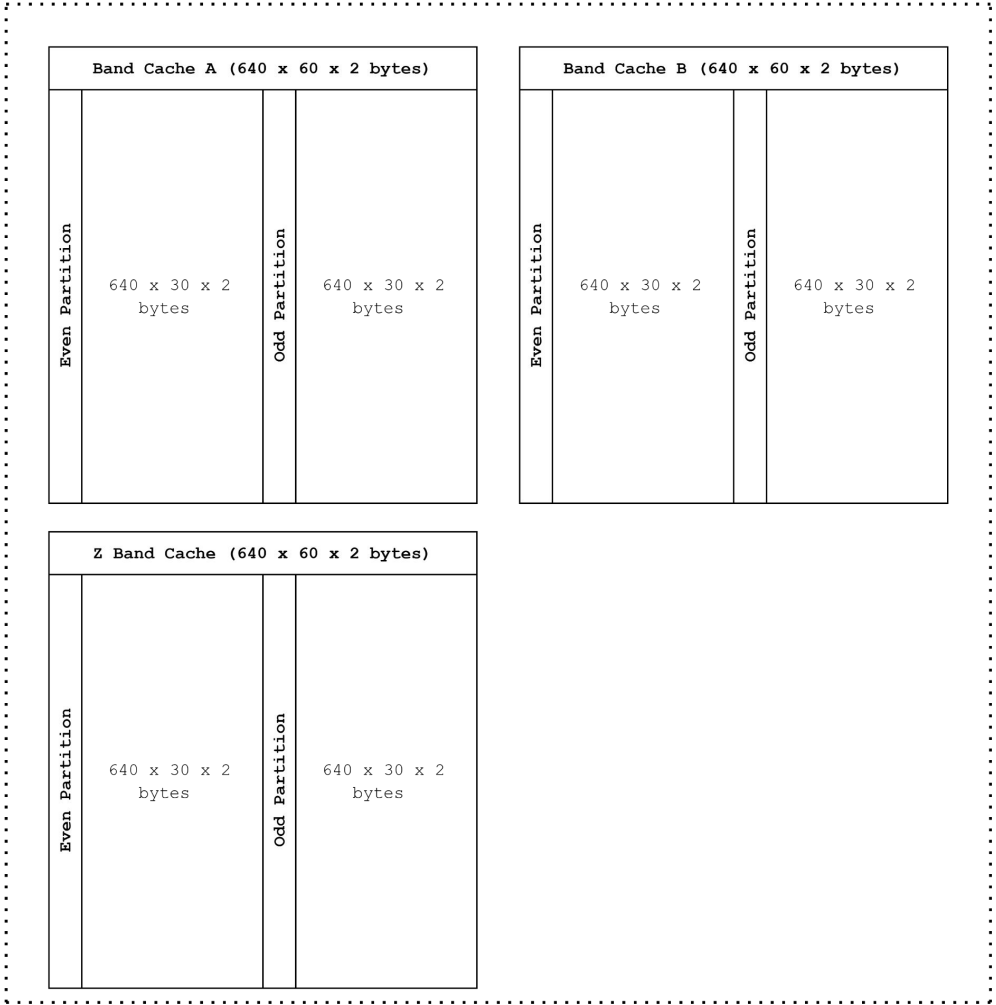
MLAB

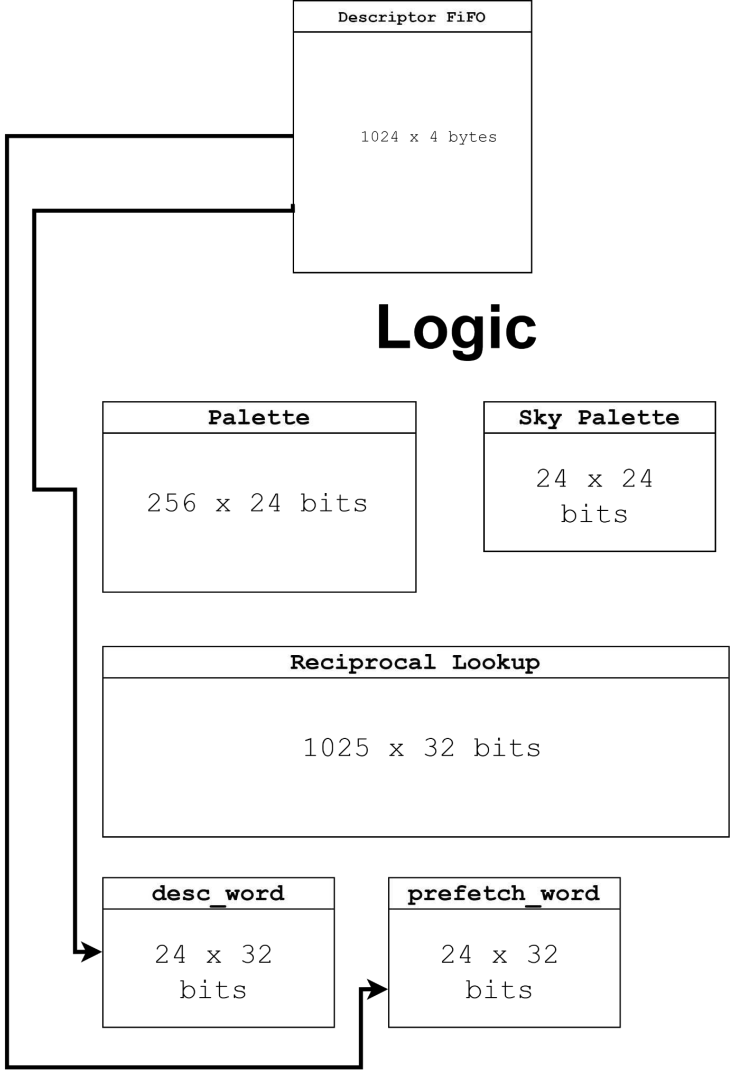




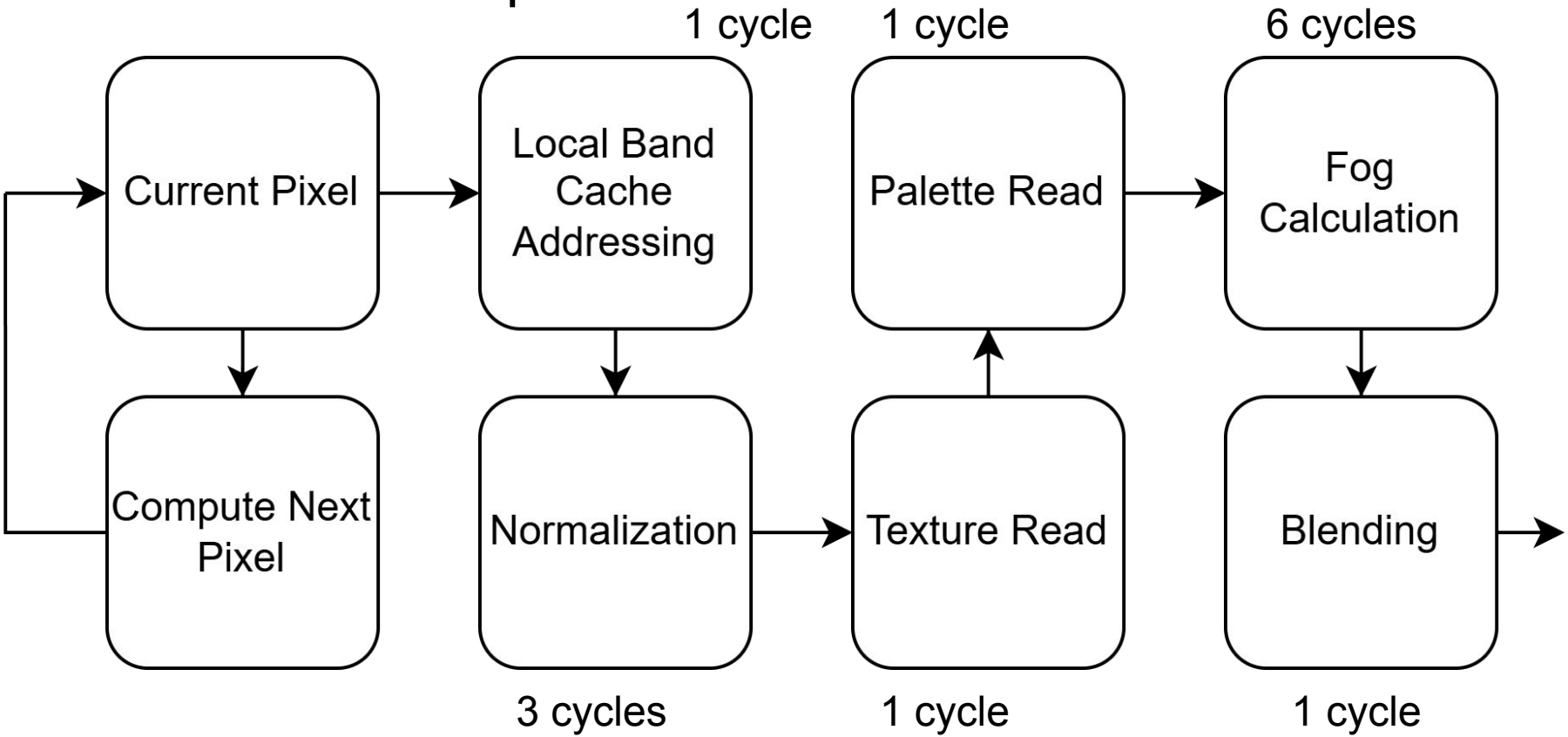

MLAB
Line Buffer 0
640 x 2 bytes
Line Buffer 1
640 x 2 bytes
Line Buffer 2
640 x 2 bytes
VGA_R_8bit
VGA_G_8bit
VGA_B_8bit
VGA Scanout (25MHz)

Local Band Caches

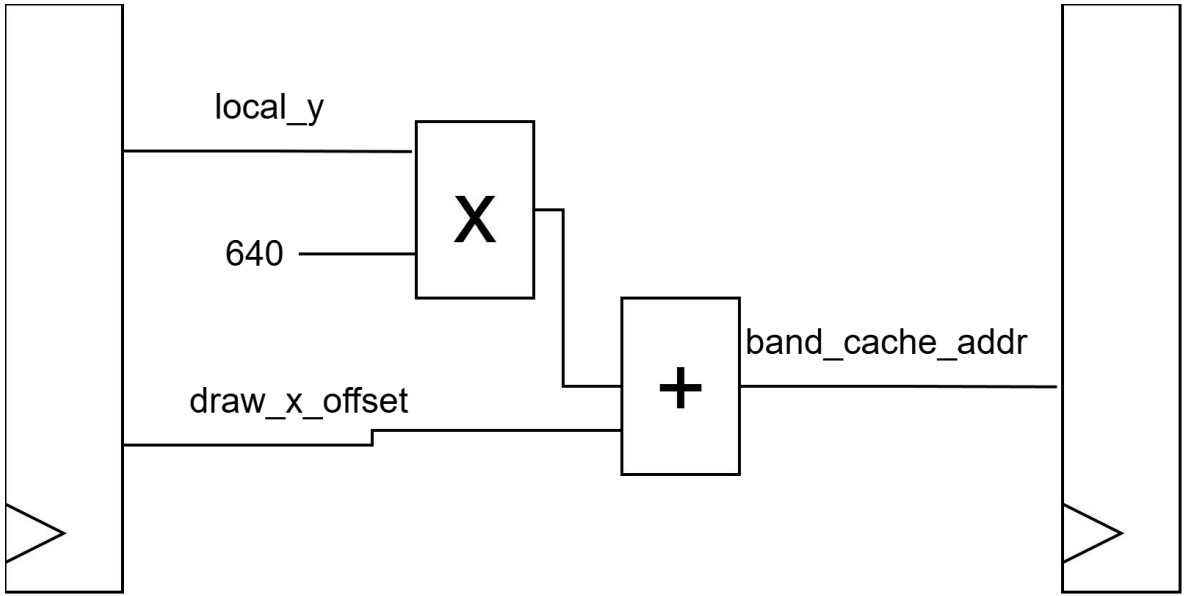



Descriptor FiFO
1024 x 4 bytes
Logic
Palette
256 x 24 bits
Sky Palette
24 x 24 bits
Reciprocal Lookup
1025 x 32 bits
desc_word
24 x 32 bits
prefetch_word
24 x 32 bits

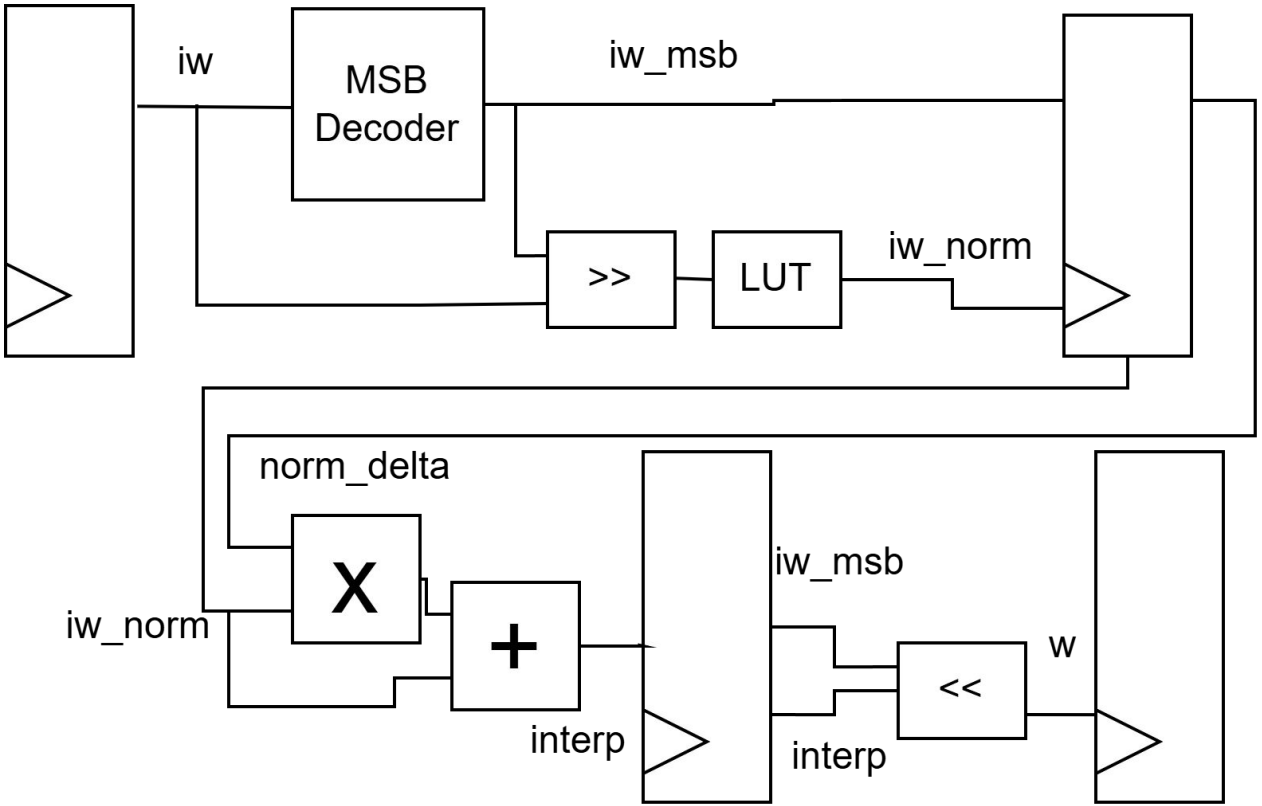
Hardware Quad Pipeline



Band Cache Indexing



Reciprocal Calculation

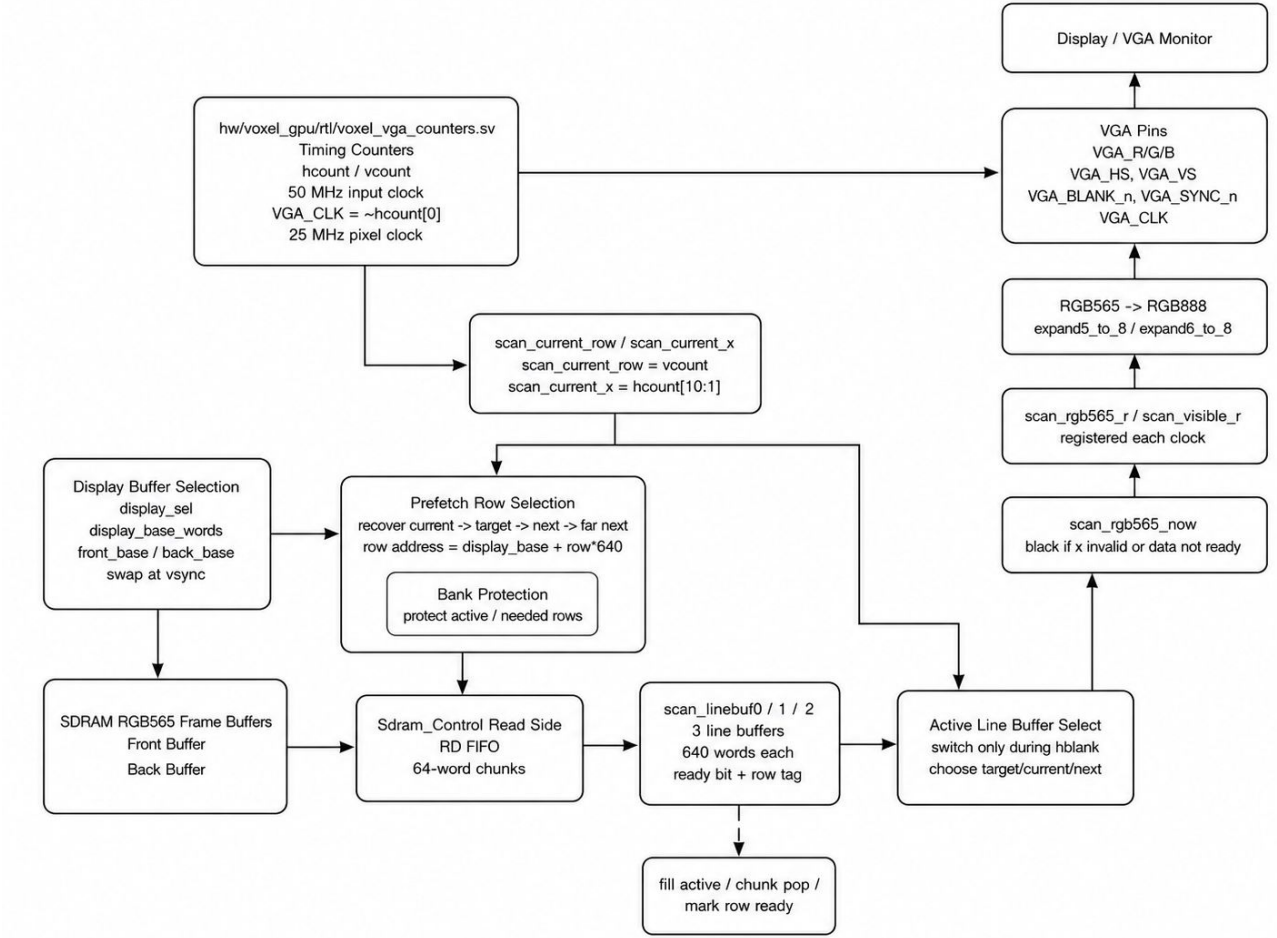


Quad Descriptor Memory Layout

quad_desc
s16 x__min, y_min, x_max, y_max
edges[4] - s32 A, B, C
u16 z0
s16 dz_dx, dz_dy
u8 tex_or_color
u8 flags

quad_desc_uv
s32 u/w, u/w dx, u/w dy
s32 v/w, v/w dx, v/w dy
s32 1/w, 1/w dx, 1/w dy

VGA Scanout


Display / VGA Monitor
hw/voxel_gpu/rtl/voxel_vga_counters.sv
Timing Counters
hcount / vcount
50 MHz input clock
VGA_CLK = ~hcount[0]
25 MHz pixel clock
VGA Pins
VGA_R/G/B
VGA_HS, VGA_VS
VGA_BLANK_n, VGA_SYNC_n
VGA_CLK
RGB565 -> RGB888
expand5_to_8 / expand6_to_8
scan_current_row / scan_current_x
scan_current_row = vcount
scan_current_x = hcount[10:1]
scan_rgb565_r / scan_visible_r
registered each clock
Display Buffer Selection
display_sel
display_base_words
front_base / back_base
swap at vsync
Prefetch Row Selection
recover current -> target -> next -> far next
row address = display_base + row*640
Bank Protection
protect active / needed rows
scan_rgb565_now
black if x invalid or data not ready
SDRAM RGB565 Frame Buffers
Front Buffer
Back Buffer
Sdram_Control Read Side
RD FIFO
64-word chunks
scan_linebuf0 / 1 / 2
3 line buffers
640 words each
ready bit + row tag
Active Line Buffer Select
switch only during hblank
choose target/current/next
fill active / chunk pop /
mark row ready

Quad Generation Math

$$\begin{bmatrix} x_{clip} \\ y_{clip} \\ z_{clip} \\ w_{clip} \end{bmatrix} = \mathbf{P} \cdot \mathbf{V} \cdot \begin{bmatrix} x_{world} \\ y_{world} \\ z_{world} \\ 1 \end{bmatrix}$$

Quartus Fitter Report

Metric	Used / Result	Available on DE1-SoC FPGA	Utilization
LABs	`3,207`	`3,207`	`100%`
MLAB memory bits	`337`	up to ~ `1,026,000` bits, using LABs as MLABs	`<1%`
ALMs	`28,687`	`32,070`	`89%`
ALUTs, logic	`31,792`	~ `64,140` ALUTs	~ `50%`
M10K blocks	`397`	`397`	`100%`
DSP blocks	`44`	`87`	`51%`
Slowest same-clock Fmax	`62.07 MHz`	target domain: `50 MHz`	passes Fm
Voxel SDRAM Fmax	`122.34–126.18 MHz`	target: `100 MHz`	passes Fm