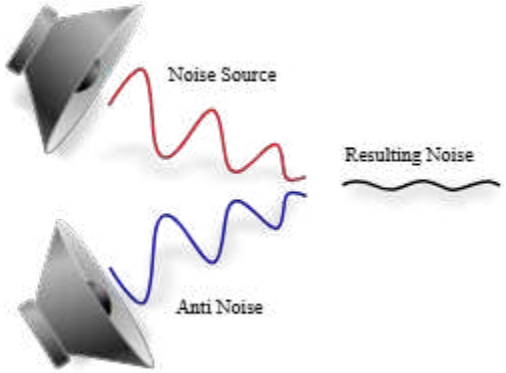


Adaptive Noise Cancellation

Sharvani Vadlamani (sv2734), Sayem Kamal (sk5336), Huda Jafri (shj2127)
Embedded Systems Spring 2026

Goal + Setup

recorded at same time

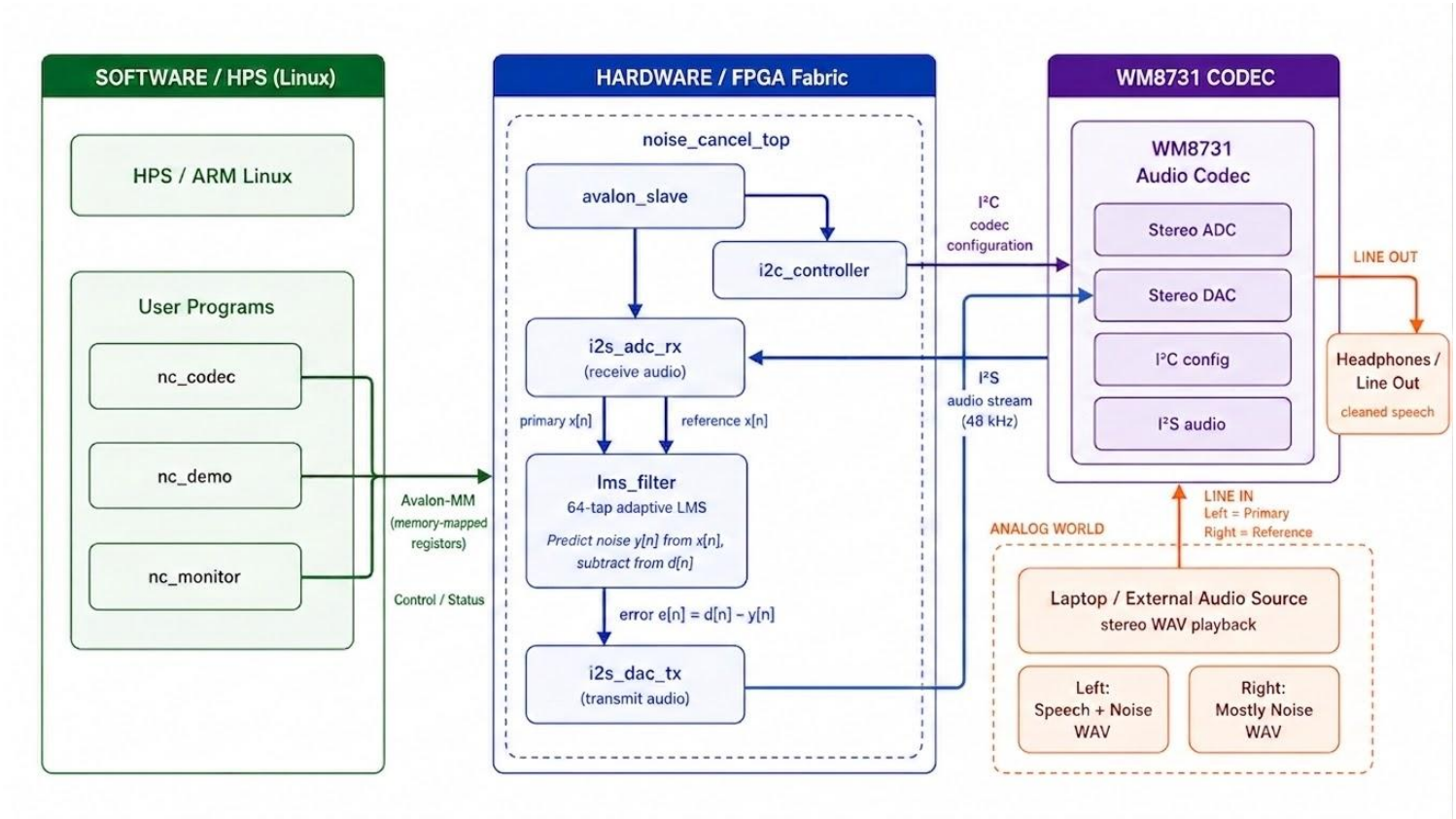
Reference WAV
w/ background noise

WAV with speech
+ noise

FPGA w/ LMS
algorithm

Only speech!

System Architecture



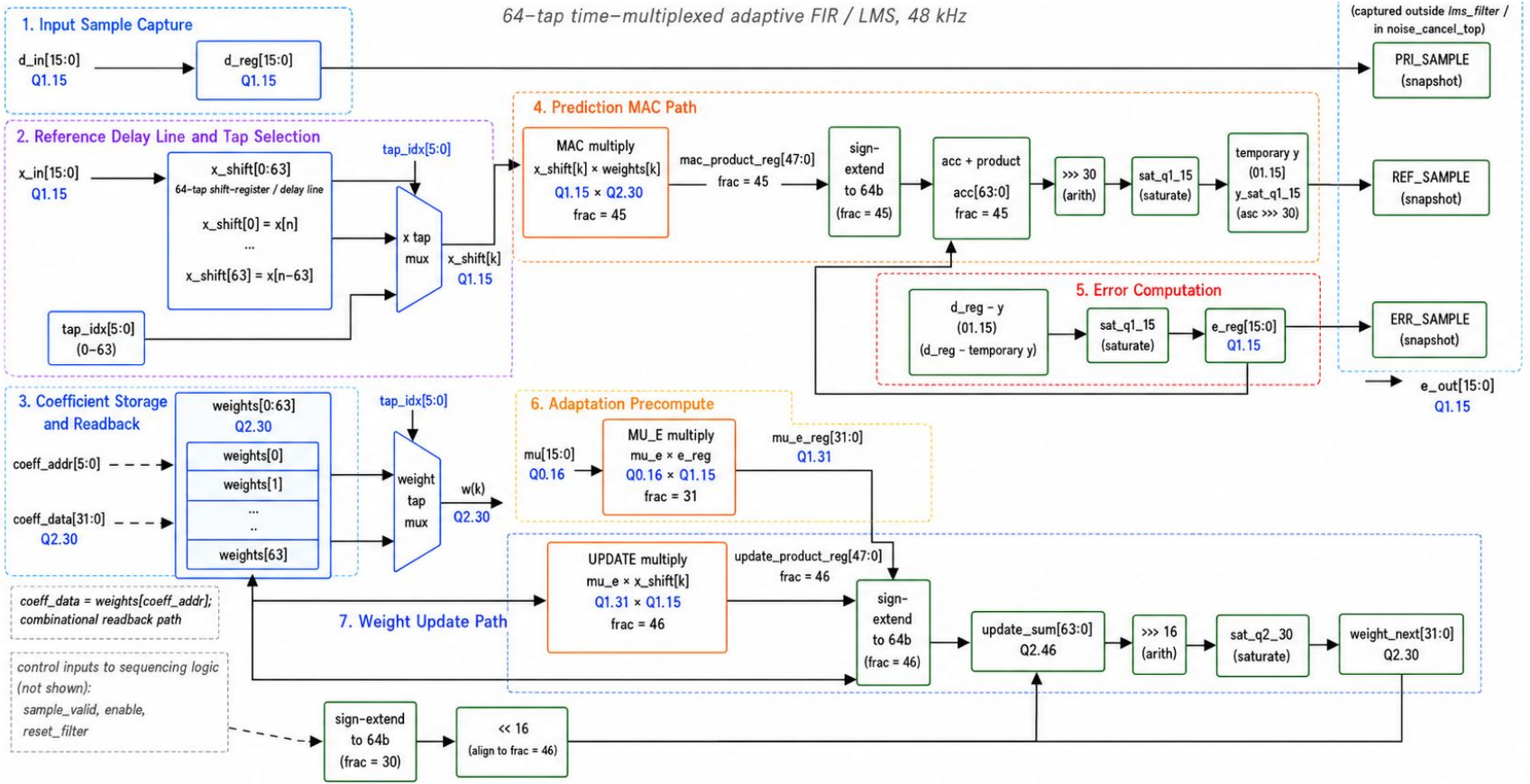
Register Map (HW→SW)

Register	Data	Purpose
CTRL	enable, bypass, reset_filter	Start/stop LMS learning, bypass LMS output, zero all weights
MU	μ (16-bit)	Learning rate, controls how aggressively weights update each sample
COEFF_ADDR	index (6-bit)	Selects which of the 64 weights to expose for readback
I2C_CTRL	reg (7-bit) + data (9-bit)	WM8731 register address and value, triggers one I^2C write transaction
STATUS	W1C bits	Acknowledge sticky events: saturation, mclk_lost
I2C_STATUS	W1C bits	Acknowledge I^2C events: done, nack

Register Map (SW→HW)

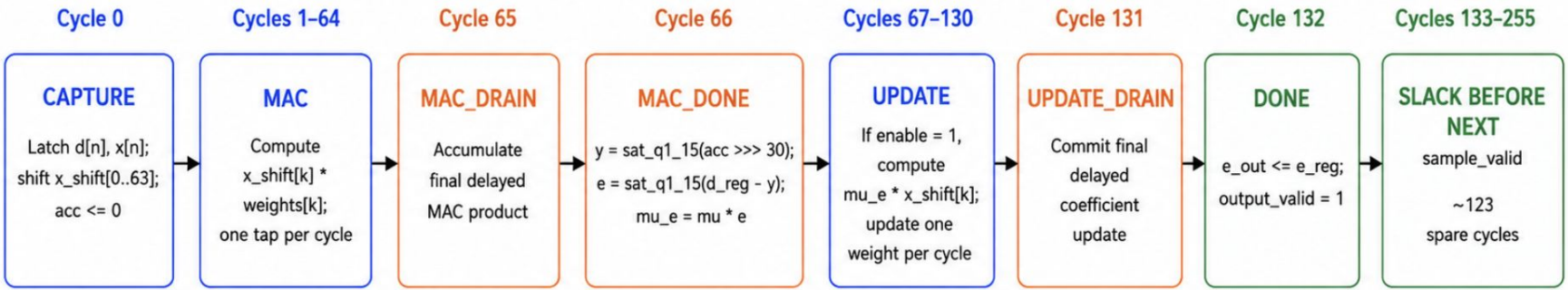
Register	Data	Purpose
MAGIC	`0x4E433031`	Device identification — confirms PLL locked and correct device
STATUS	codec_alive, mclk_lost, saturation	Hardware health flags — saturation means μ too high
REF_SAMPLE	x[n] (16-bit)	Last reference mic sample for monitoring
PRI_SAMPLE	d[n] (16-bit)	Last primary mic sample for monitoring
ERR_SAMPLE	e[n] (16-bit)	Last LMS error output — the cleaned speech signal
COEFF_DATA	w[k] (32-bit)	Weight at index set by COEFF_ADDR — inspect filter convergence
I2C_STATUS	busy, done, nack, last_ack_ok	I^2C transaction state — confirms codec configured correctly

LMS Datapath



Timing

aud_mclk:	sample rate:	cycles per sample:	cycle time:	sample period:
12.288 MHz	48 kHz	256	81.38 ns	20.833 us



Enabled LMS path: ~133 cycles = ~10.82 us

Disabled path (no adaptation): ~68 cycles

Note: MAC_DRAIN and UPDATE_DRAIN are required because the multiply/accumulate and update paths are one-cycle pipelined.