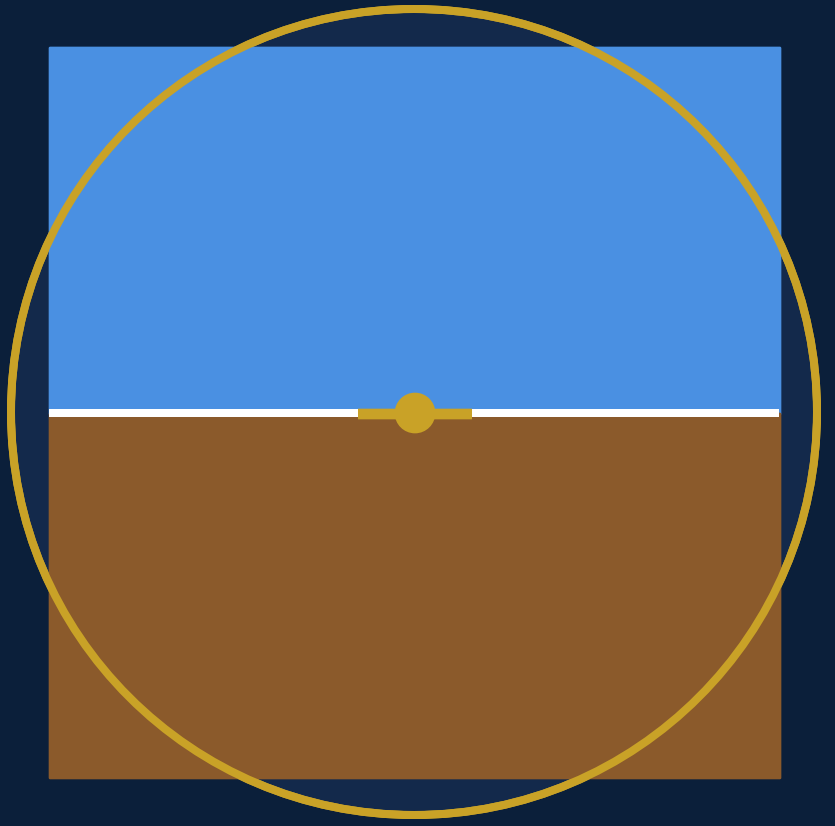
HARDWARE ACCELERATED

AHRS

Attitude & Heading Reference System on DE1-SoC



TEAM

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Project Overview

Real-time attitude estimation accelerated in FPGA fabric

- MPU-6050 IMU streamed over I^2C at 1 kHz
- HPS performs bias calibration, atan2 angle extraction, Q3.9 encoding
- Custom Kalman filter accelerator on FPGA fuses accel + gyro
- Avalon-MM Lightweight Bridge mediates HPS ↔ FPGA traffic
- Filtered roll / pitch rendered as VGA artificial horizon @ 60 Hz

AT A GLANCE

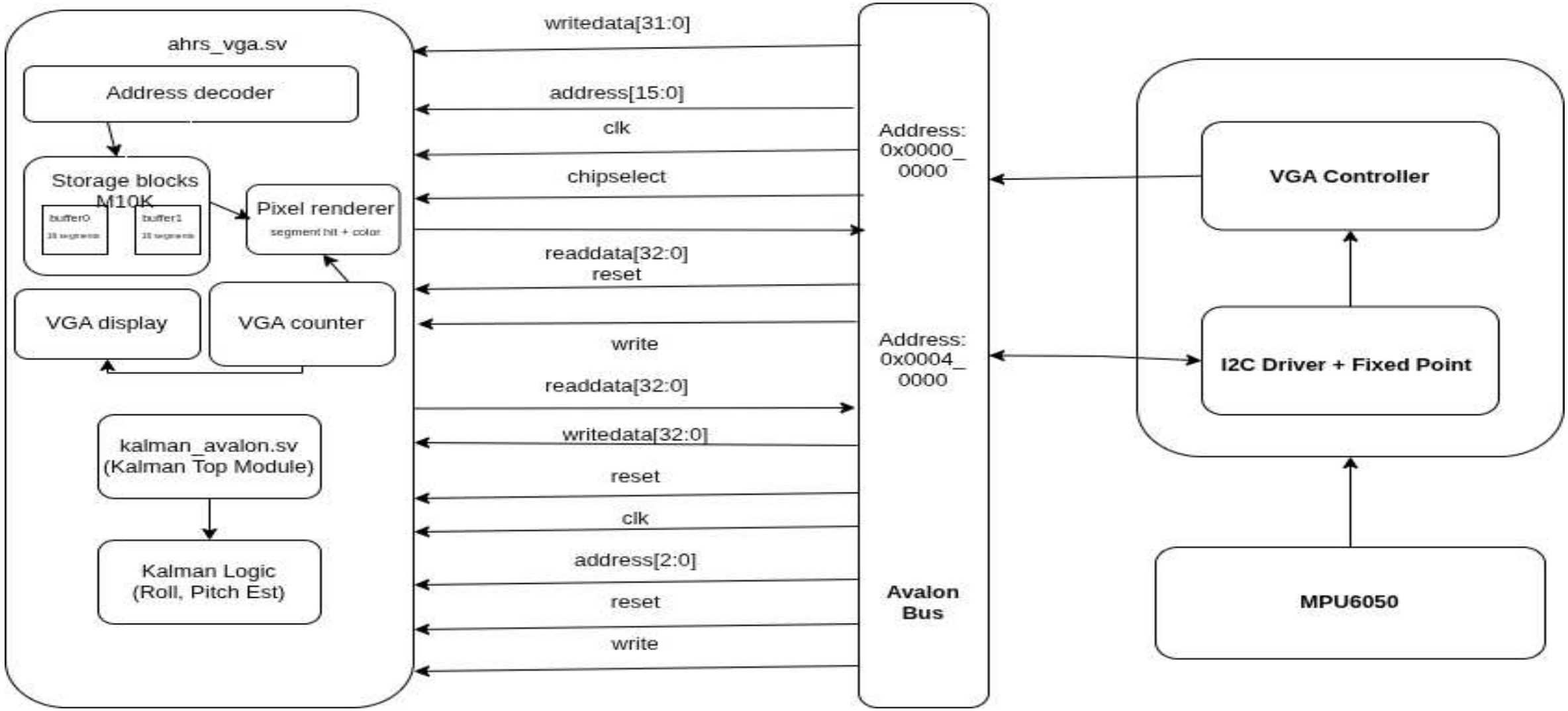
1 kHz
IMU sampling rate

Q3.9
fixed-point format

60 Hz
VGA display refresh

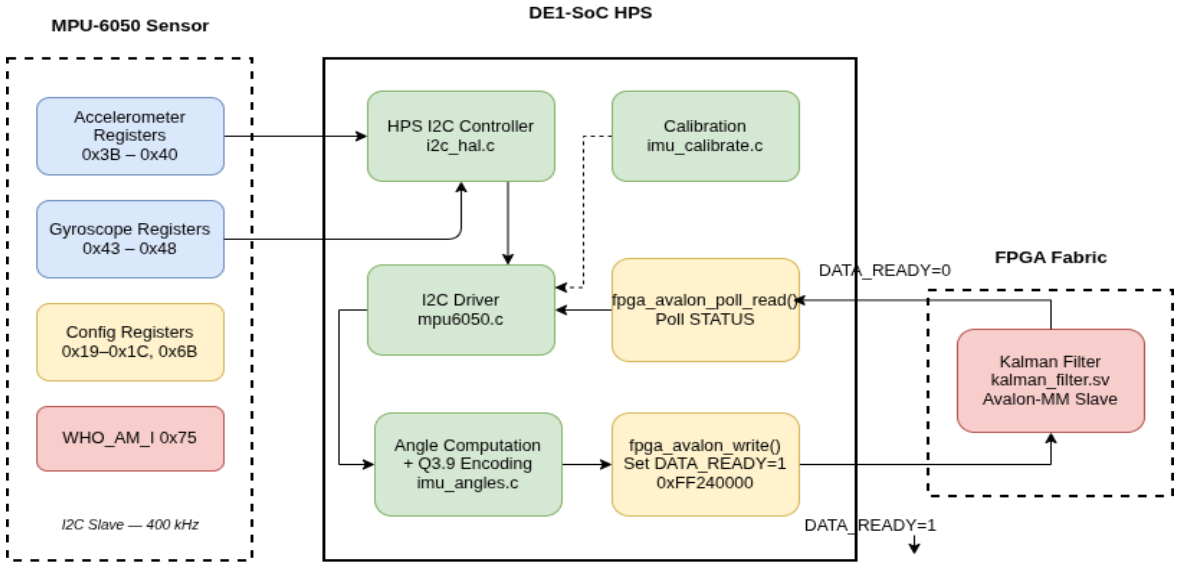
50 MHz
FPGA system clock

System Architecture



Sensor Interface & I²C Driver

- User space driver — no custom kernel module
- Linux i2c-dev via /dev/i2c-1, I2C_RDWR ioctl with repeated START
- WHO_AM_I (0x68) probe confirms device on boot
- 1 kHz sample rate, 188 Hz DLPF, ±250 °/s gyro, ±2 g accel
- 14-byte burst read at 0x3B → 6 axes per transaction
- 1000-sample bias calibration on startup, gravity-corrected az
- atan2f → roll/pitch; gyro LSB → rad/s; encoded as Q3.9

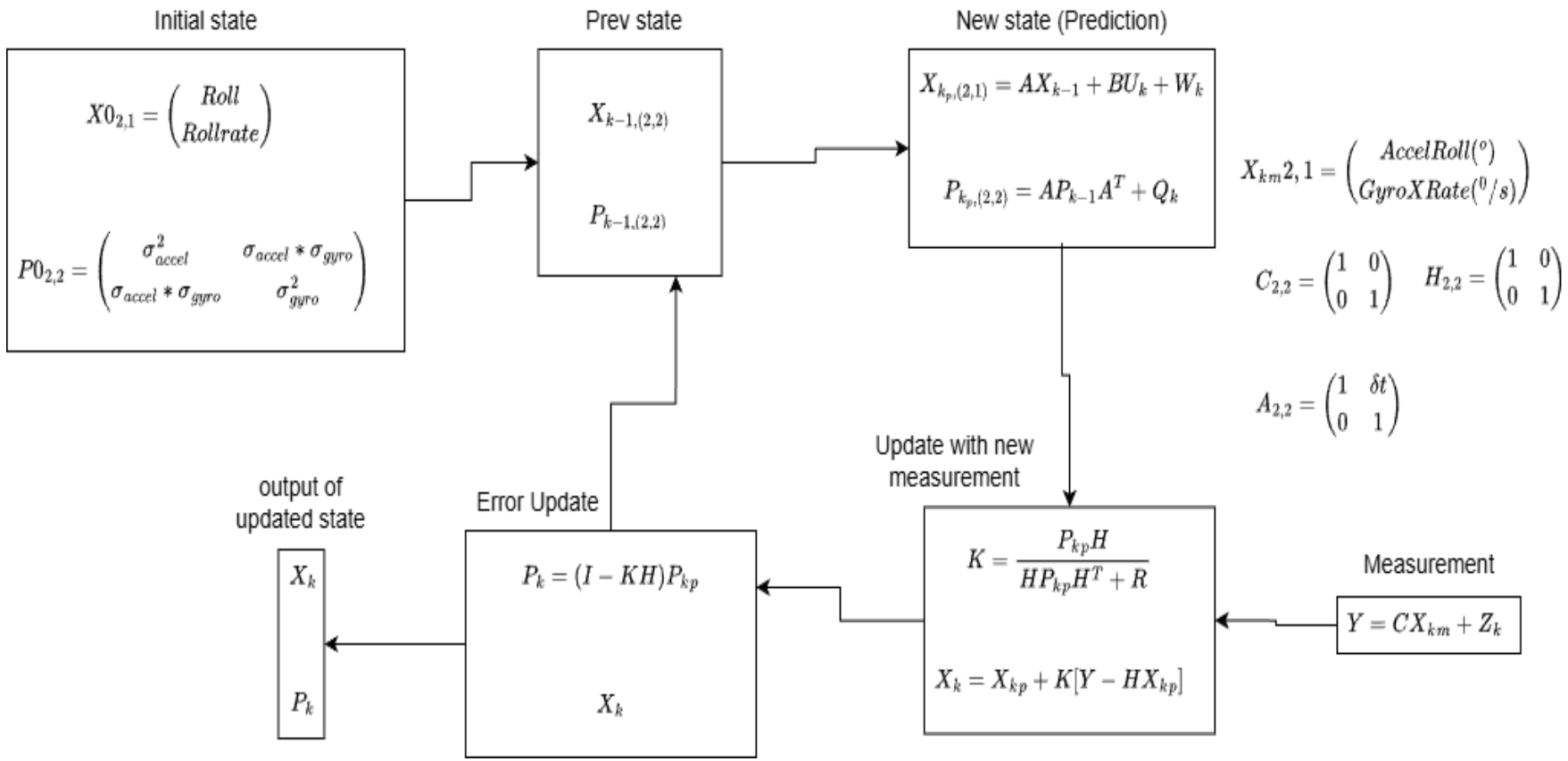


DATA PIPELINE (per sample)

1. **Raw IMU read**
   int16 ax,ay,az,gx,gy,gz
2. **Apply bias**
   subtract calibration offsets
3. **Compute angles**
   roll = atan2(ay, az)
4. **Convert gyro**
   LSB → rad/s
5. **Encode Q3.9**
   scale ×512, clip ±2048, 12 bits

Q3.9 fixed-point · range ±3.998 · resolution ~0.00195 · 12-bit signed

Kalman Filter — Concept



U_k – Control variable matrix

W_k – Predicted state noise matrix

Q – Process noise covariance matrix

R – Sensor Noise Covariance matrix from measurement

Y – Output vector

P – Process covariance matrix- error in the process

C – Output Matrix

H – Observation matrix

A – State Matrix

X – State vector

B – Control matrix

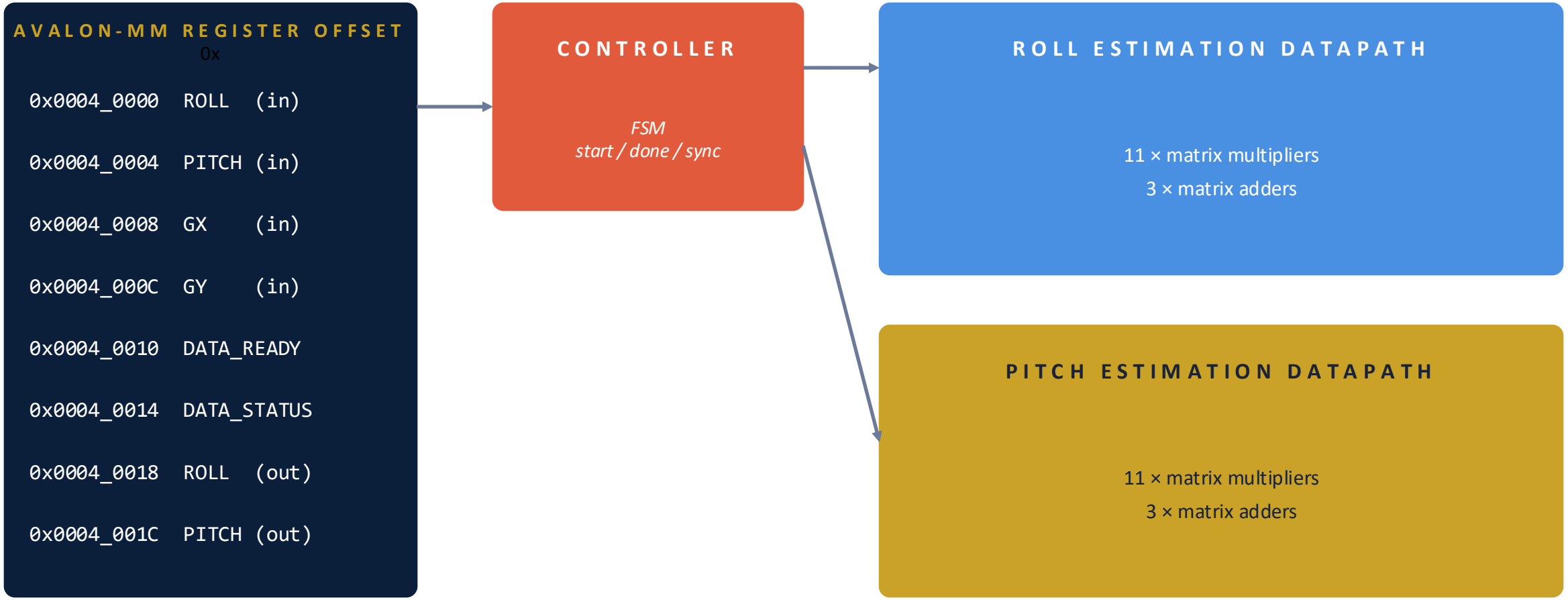
Z – Measurement noise matrix

X_{km} – Measurement matrix

K – Kalman Gain

Kalman Filter — Hardware Top Level

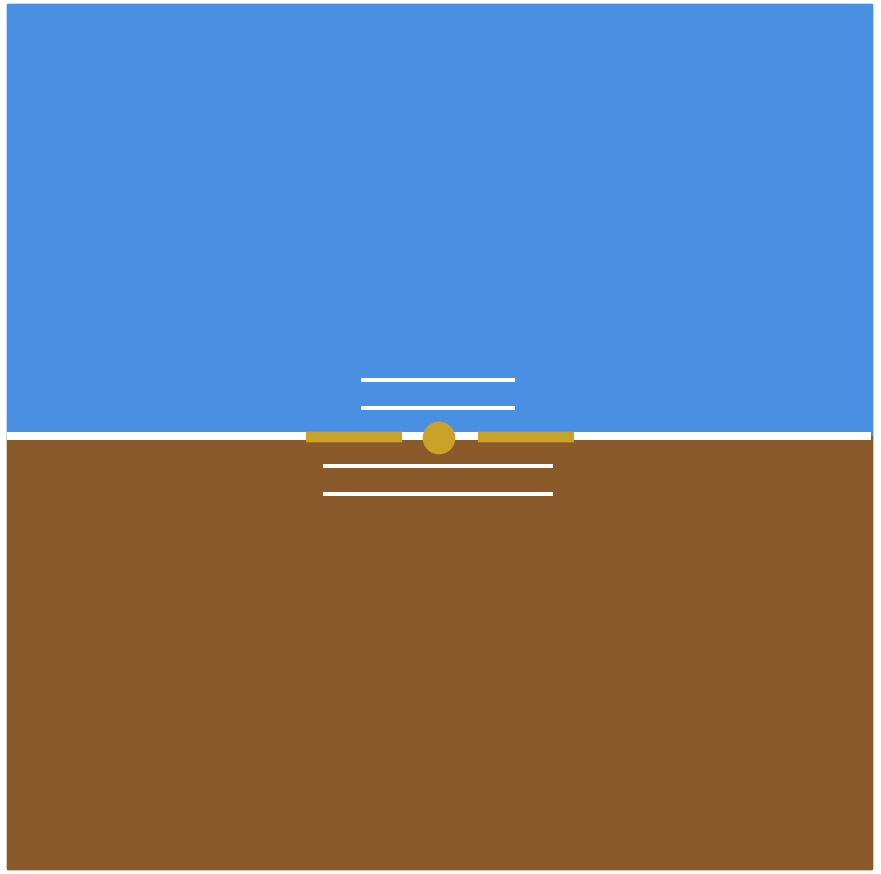
Roll and pitch estimation pipelines run in parallel; Avalon-MM register file is the HPS handshake surface



Total compute: 176 × 16-bit multipliers · 112 × 16-bit adders

VGA Display — Segment-Based Renderer

- 640 × 480 artificial horizon, generated directly from on-chip RAM
- Per-row segment list instead of full pixel framebuffer
- 16 segments × 32 bits per scanline → [12b xstart | 12b xstop | 8b RGB332]
- Reduces memory from 921 kB to ~64 kB
- 16 parallel M10K RAMs — one per segment slot, checked simultaneously
- Double-buffered swap during vertical blanking — no tearing



Live attitude indicator — sky / ground / horizon all encoded as a handful of segments per row

Resource Budgets, Timing & Utilisation

Cyclone V 5CSEMA5F31C6 · Quartus Prime 21.1 · Slow 1100 mV 85 °C model

4,939
ALMs used
15% of 32,070

3,884
Registers
—

64
M10K RAM blocks
16% of 397

87
DSP Blocks
100% utilised

MEMORY

Block memory bits	**524,288 / 4,065,280 (13%)**
VGA controller (ALMs / regs)	**568 ALM · 964 regs**
Display buffers (calculated)	**2 × 480 × 16 × 32 b = 61.44 kB**
Total I/O pins	**362 / 457 (79%)**
DLLs	**1 / 4 (25%)**

TIMING — STA RESULTS

28.91 MHz

Fmax on clock_50_1 (target: 50 MHz)

Worst setup slack: **−0.766 ns**

HPS PLL clock: **1184.83 MHz (restricted 717.36)**