Digital Instrument Multi Effects Processing Unit

Presented by Ziqian Deng (zd2285), Longyi Li (ll3527), Yifan Zhan (yz4149), Yuqi Zhu (yz4137)

Contents

Overview

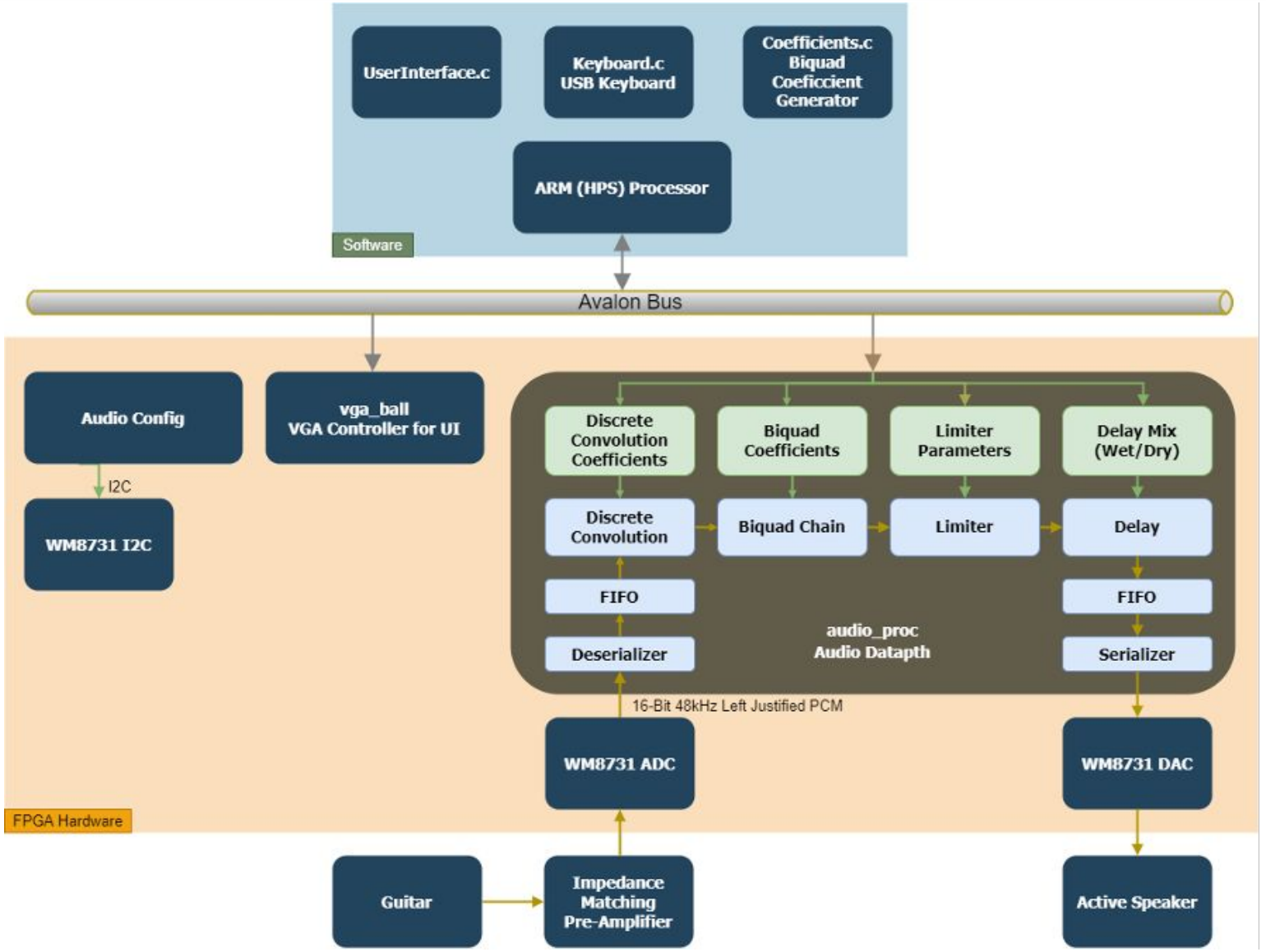
- Proposed multi-effects processor: cabinet IR, limiter effect, equalizer effect and delay effect
- Contribution: an ADC-DAC signal path, effects implementation and VGA UI

DeArmond Guitar

Effect Pedals

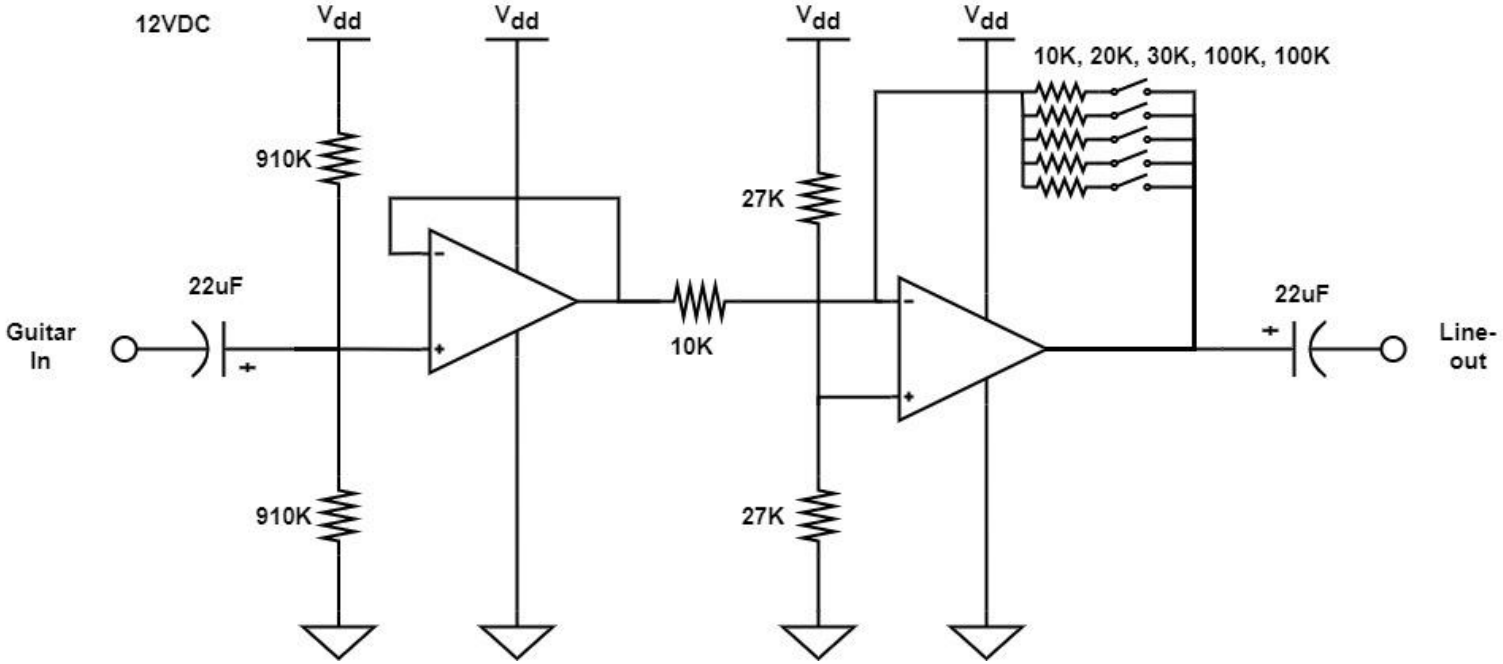
Rack Mount Effects

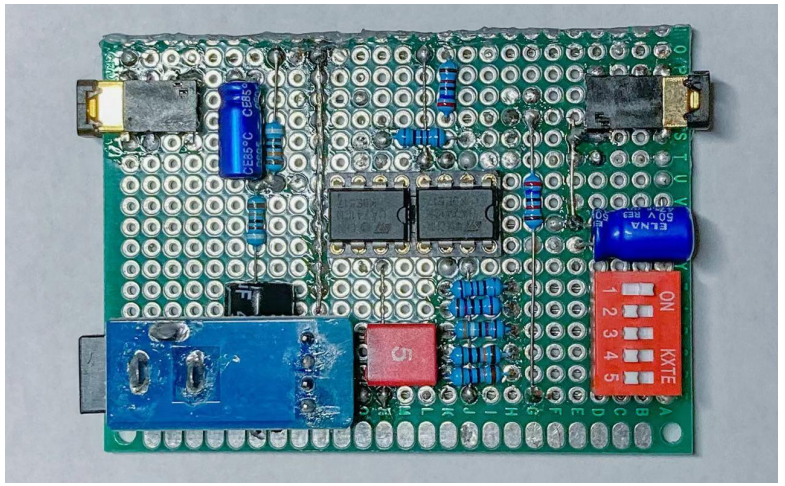
System Architecture



Analog Pre-Amplifier

An analog pre-amplifier is required for connecting the guitar to the DE1.





I2S Interface

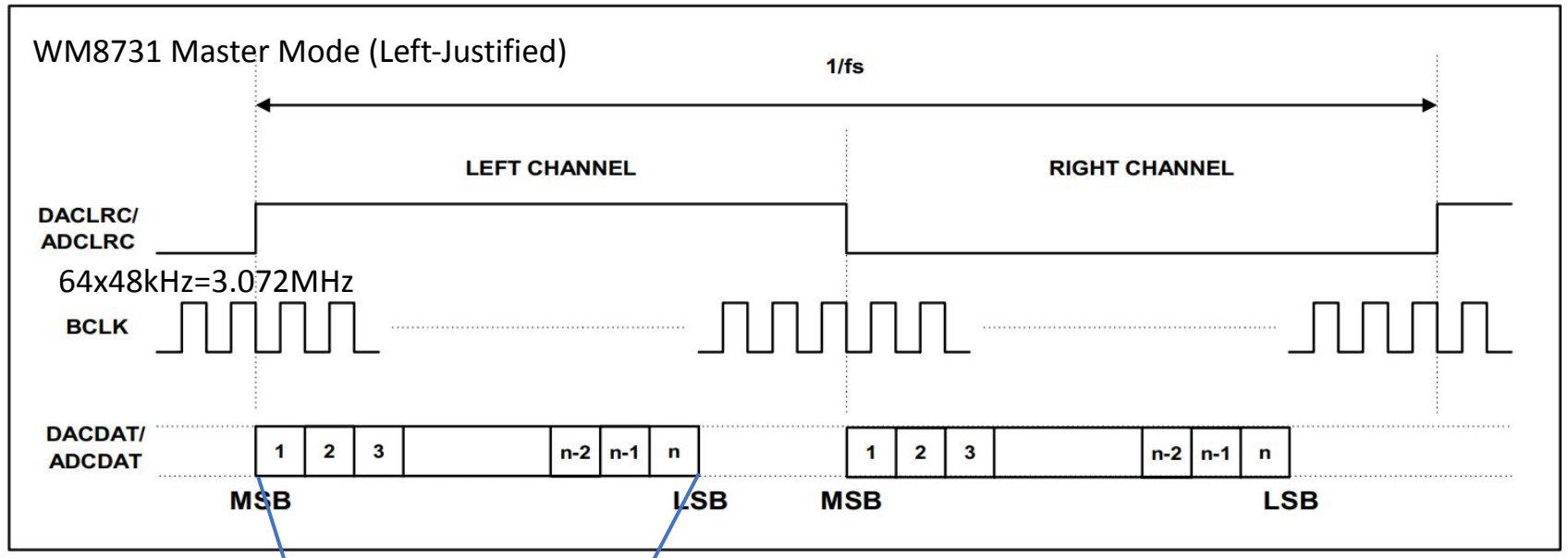
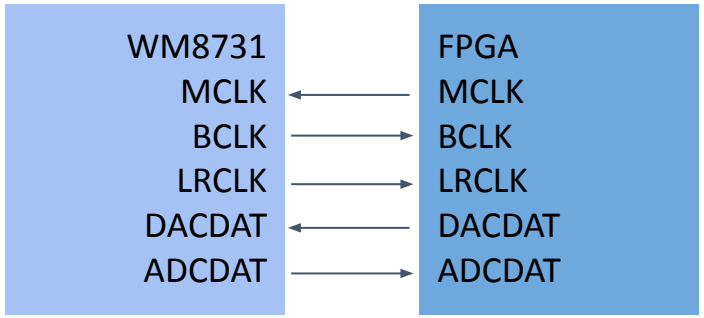
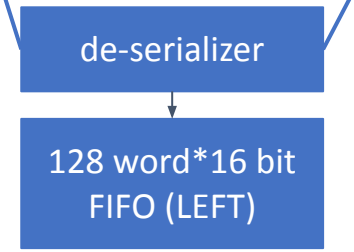


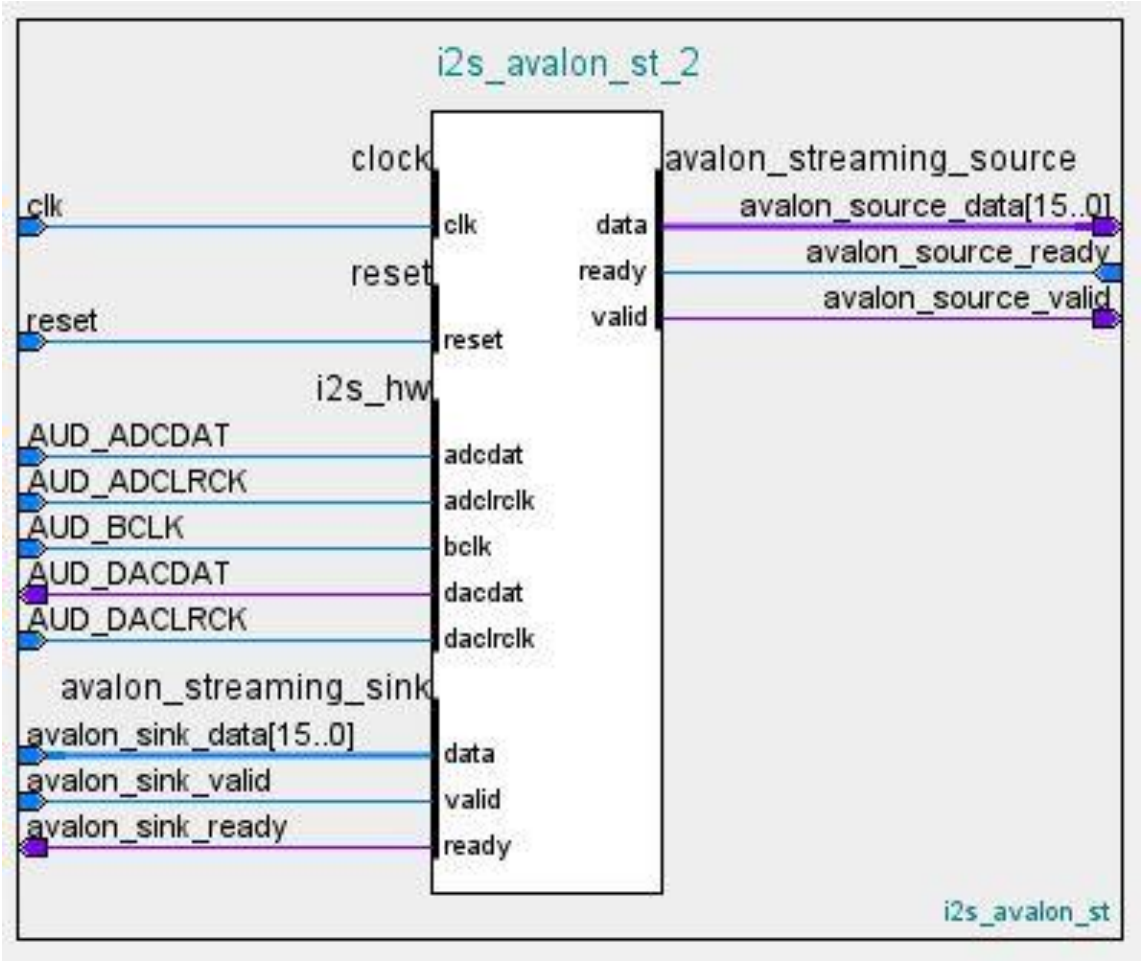
Figure 26 Left Justified Mode





I2S Interface

- Avalon-ST source
  - ADC Input Data
- Avalon-ST source
  - DAC Output Data
- Exported I2S signals
- MCLK is generated separately with pll



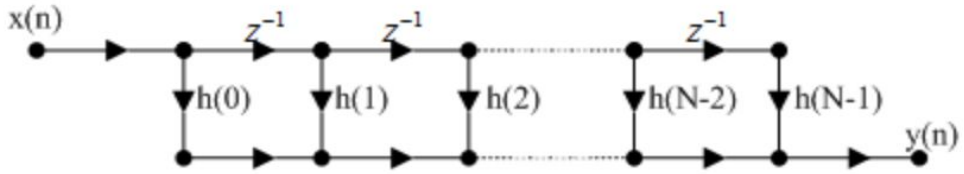
FIR Module

Cabinet IR

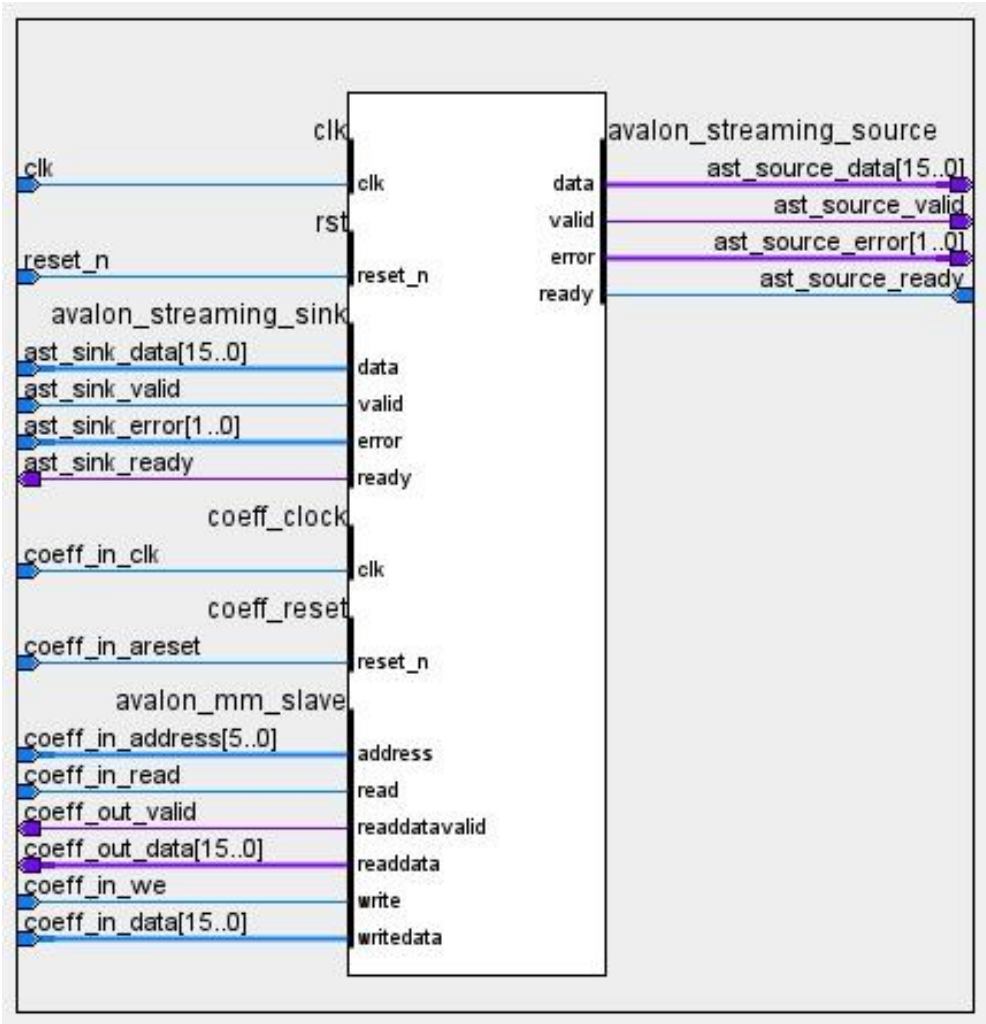
- FIR Filter
- 500 configurable coeffs

Interface

- Address: 0x0000_1000 - 0X0000_13ff
- 500 FIR coefficient



$$y[n] = \sum_{k=-\infty}^{\infty} x[k]h[n-k]$$



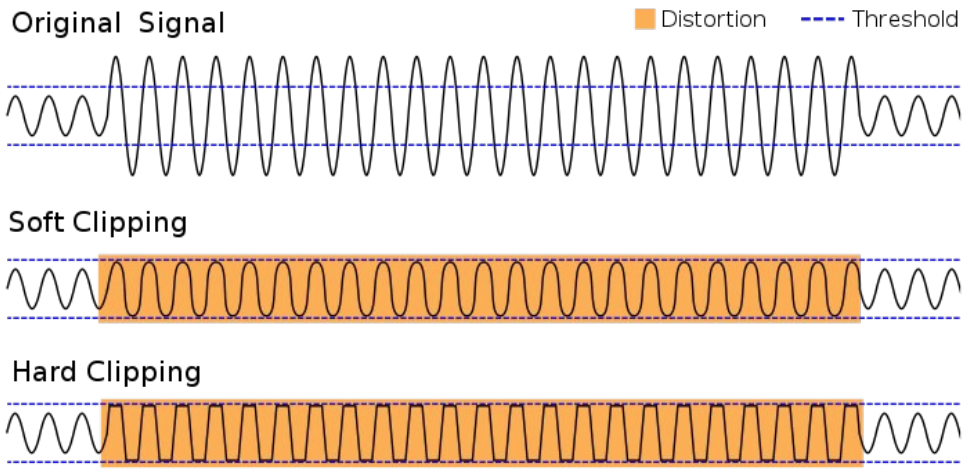
Clip Module

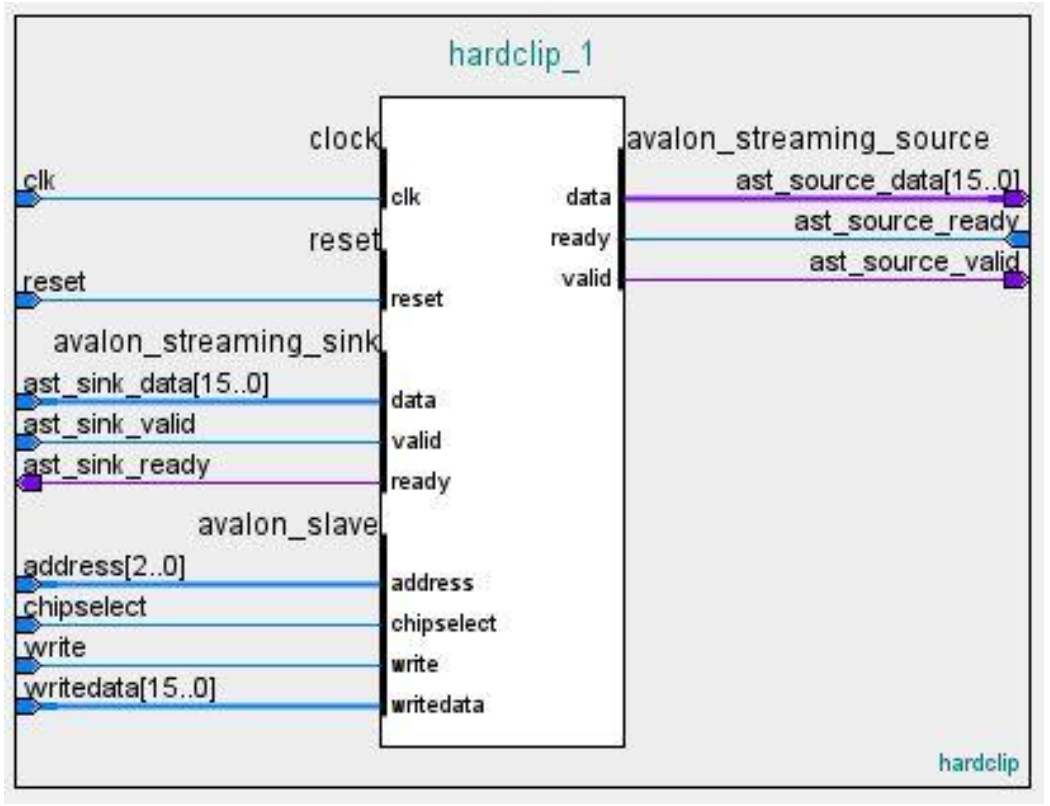
Limiter

- Clips the audio signal above a certain threshold

Interface

- Address: 0x0000_0010 - 0x0000_001f
- reg 0: threshold positive
- reg 1: threshold negative





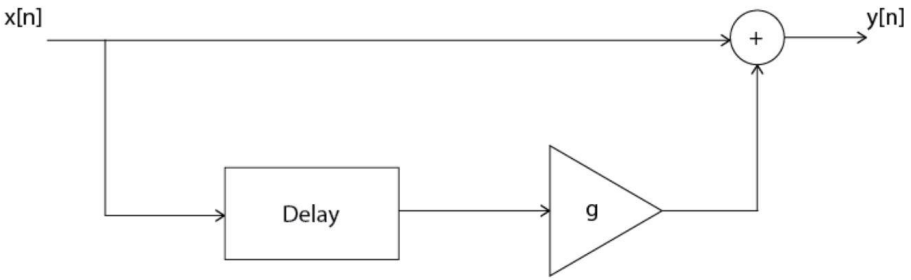
Delay Module

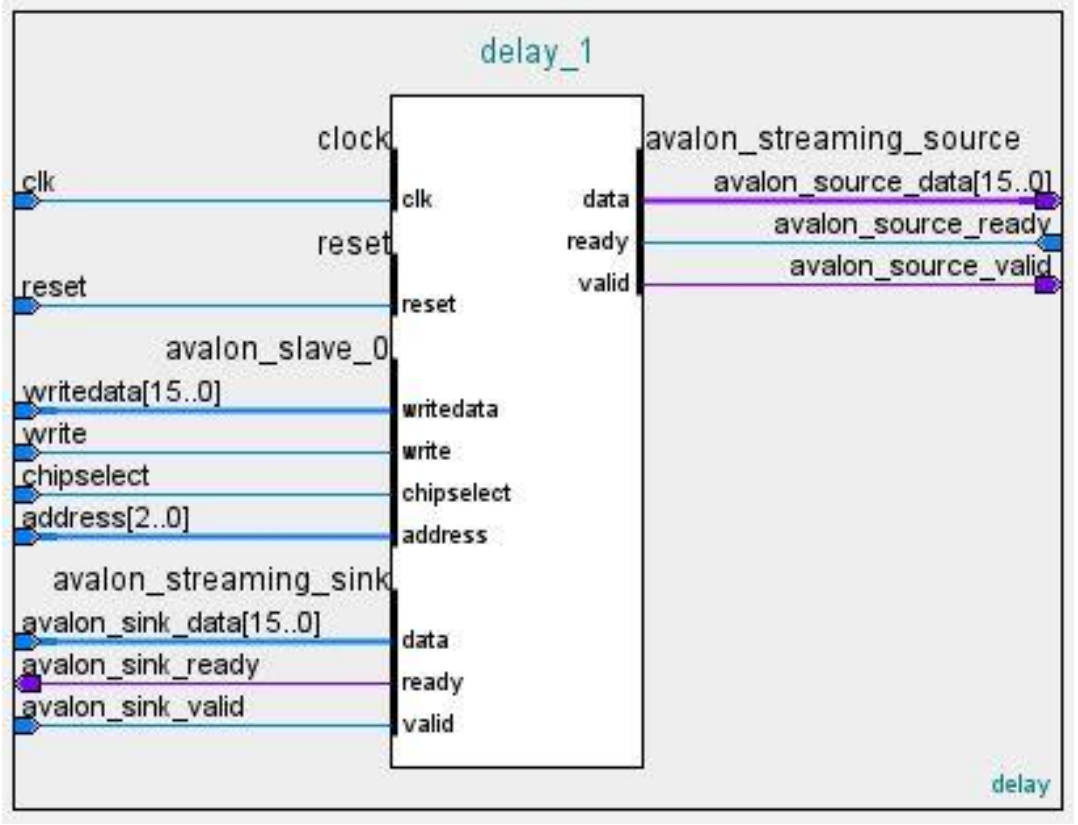
Delay

- Mixing delayed sound with not delayed sound

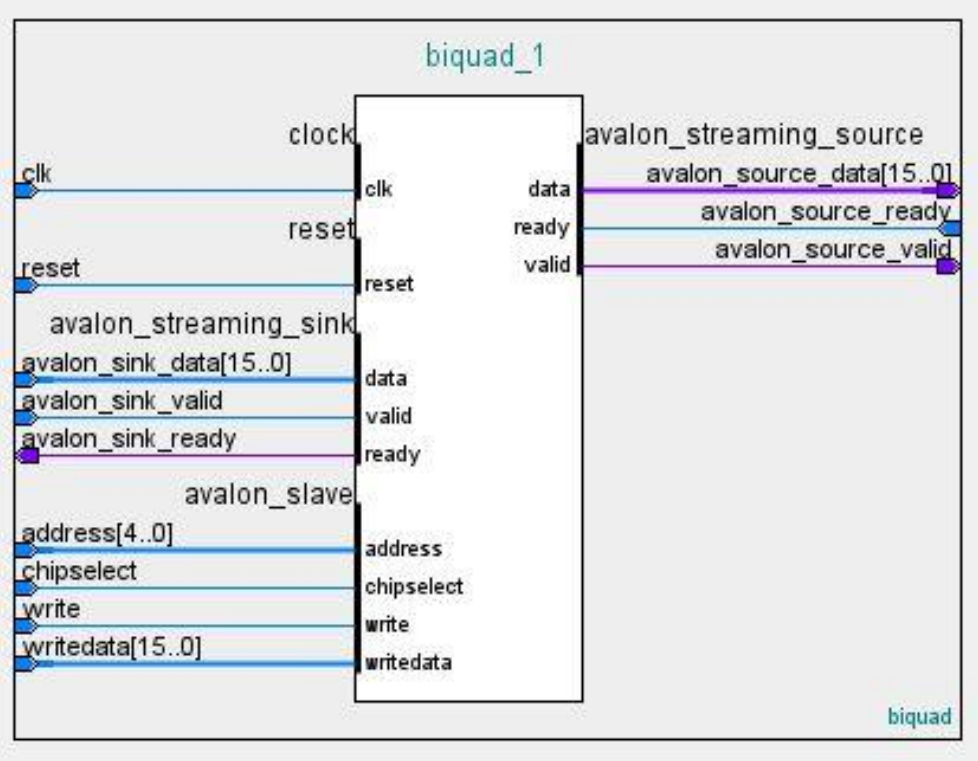
Interface

- Address: 0x0020 - 0X0000_002f
- reg 0: Bypass
- reg 1: Delay length
- reg 2: Mix

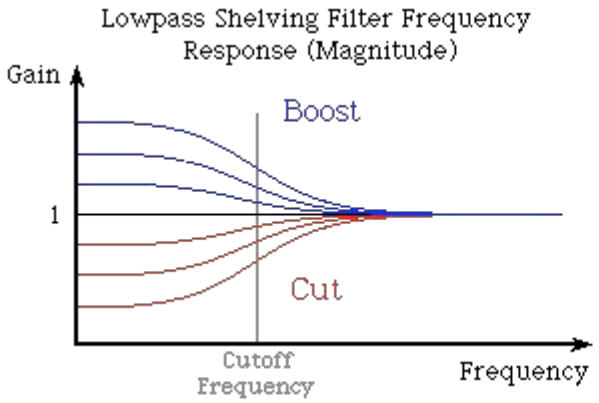


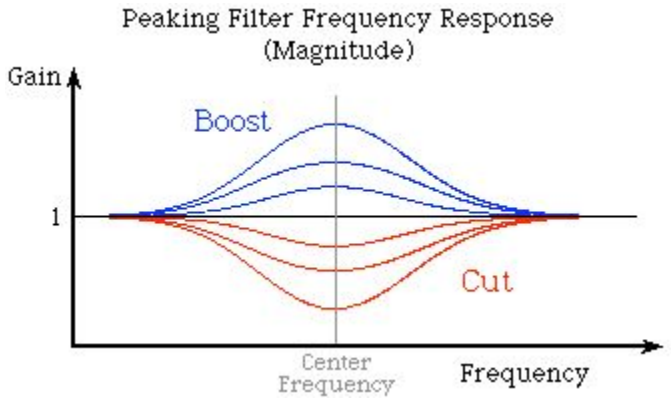


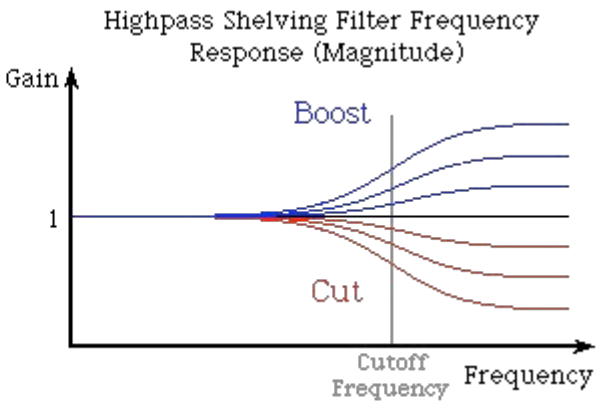
Biquad Chain



Biquad 3-band Equalizer

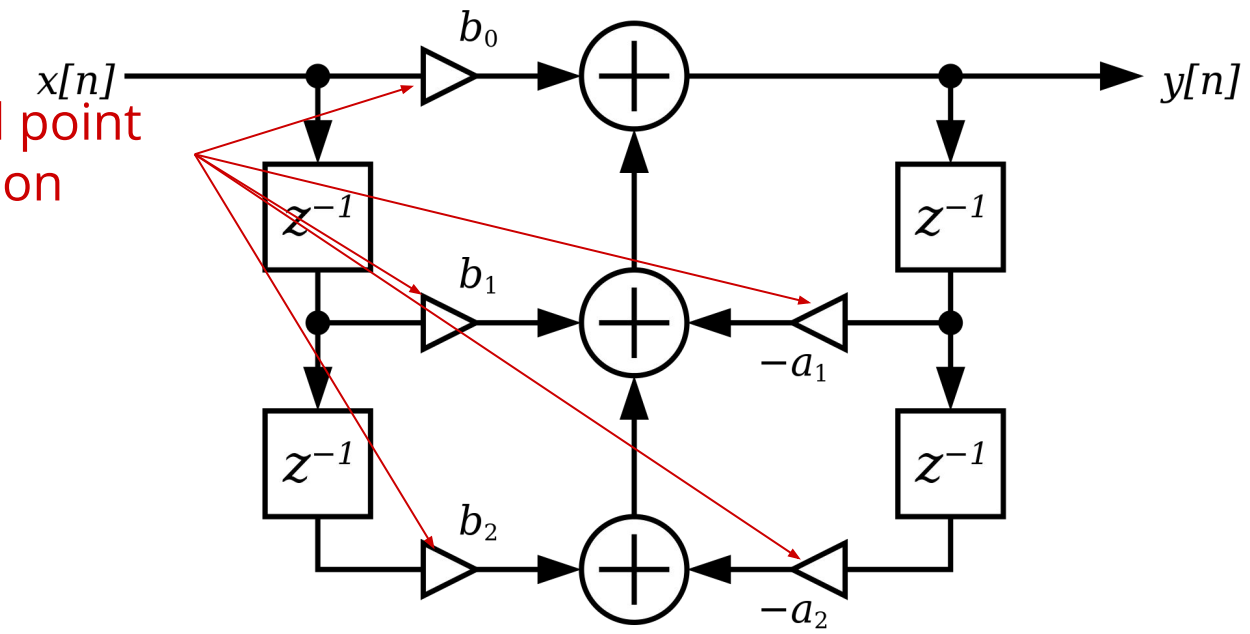






Biquad 3-band Equalizer

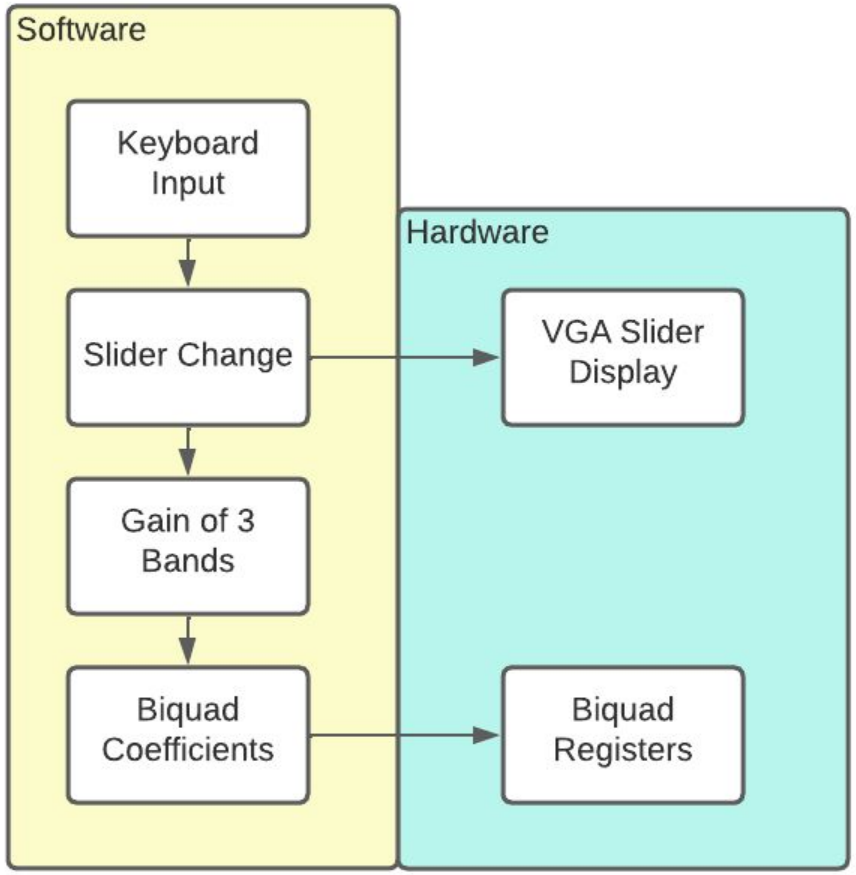
16-bit fixed point multiplication



$$H(z) = \frac{Y(z)}{X(z)} = \frac{b_0 + b_1 Z^{-1} + b_2 Z^{-2}}{1 + a_1 Z^{-1} + a_2 Z^{-2}}$$

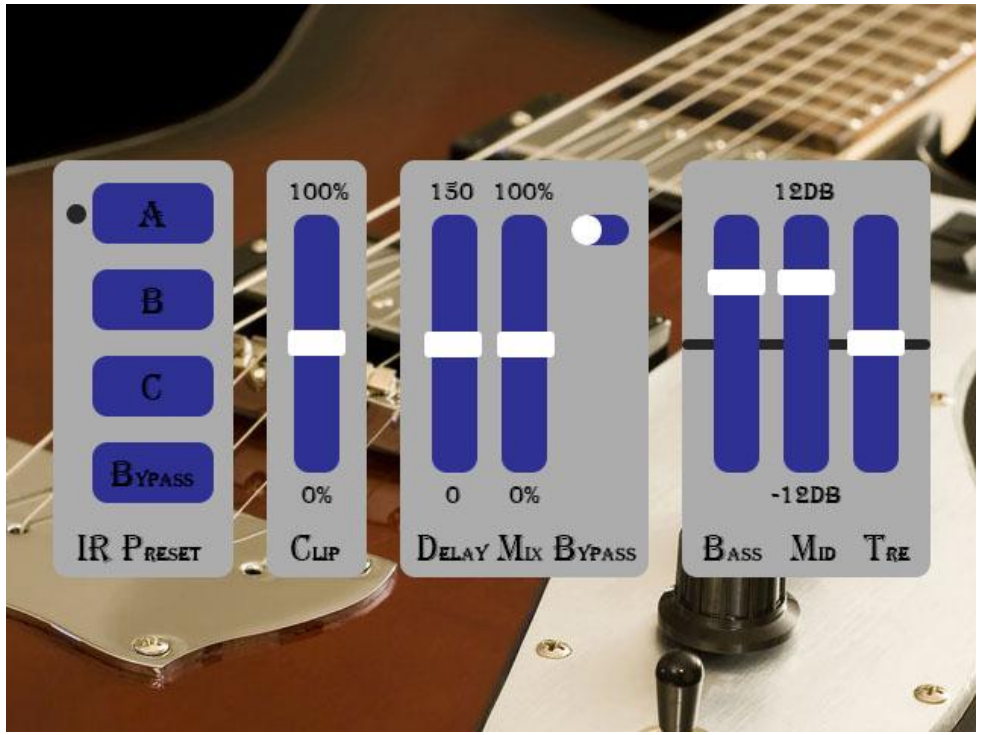
$$y[n] = \left(\frac{b_0}{a_0}\right) x[n] + \left(\frac{b_1}{a_0}\right) x[n-1] + \left(\frac{b_2}{a_0}\right) x[n-2] - \left(\frac{a_1}{a_0}\right) y[n-1] - \left(\frac{a_2}{a_0}\right) y[n-2]$$

Biquad 3-band Equalizer



VGA User Interface

- Memory initialization file
  - background image
  - sliders and switches sprites
- Background image: 640*480, 8-bit color
- Control and select via keyboard
  - IR preset (Key 1, 2, 3, 4)
  - clip (Key Q, A)
  - delay time (Key W, S)
  - delay mix (Key E, D)
  - delay bypass (Key B, N)
  - bass (Key R, F)
  - mid (Key T, G)
  - treble (Key Y, H)
- Controller sprites position
  - preset sel, bypass sw and 6 sliders
  - stored in 8 16-bit registers
  - address: 0x0000_2000 - 0x0000_200f



Resource Budget

On-Chip BRAM Budget					
	INPUT FIFO LEFT	**INPUT FIFO RIGHT**	**FIR FIFO**	**FIR COEFF**	**VGA SPRITE**
SAMPLES (WORD)	128	128	500	500	640x480
MEMORY (BIT)	128x16	128x16	500x16	500x16	640x480x8
			TOTAL	**2478/4460Kb**	**55.6%**

DSP BLOCK Budget			
		FIR	**BIQUAD**
BLOCKS USED		2	20
	TOTAL	**22/87**	**25.29%**

Conclusion

- Work statement
  - Ziqian Deng - FIR module, delay module and clip module
  - Longyi Li - Top level of design and pre-amplifier hardware
  - Yifan Zhan - VGA user interface
  - Yuqi Zhu - Biquad module

- Milestone completion
  - Complete an ADC-DAC signal path ✓
  - Implement a cabinet IR ✓
  - Implement a boost/overdrive effect ✓
  - Add user interface to configure effects ✓
  - Add delay effect ✓

- Design files
  - Hardware
    - soc_system.sv
    - vga_ball.sv
    - i2s_avalon_st.sv
    - hardclip.v
    - delay.v
    - biquad.v
  - Software
    - Makefile
    - biquad.h/c
    - eq_coeff.h/c
    - delay.h/c
    - fir.h/c
    - hardclip.h/c
    - hello.c
    - usbkeyboard.h/c
    - vga_ball.h/c

Demo

Thanks for listening