Qsys (Platform Designer) and IP Core Integration

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IP Cores

Altera’s IP Core Integration Tools

Connecting IP Cores

IP Cores

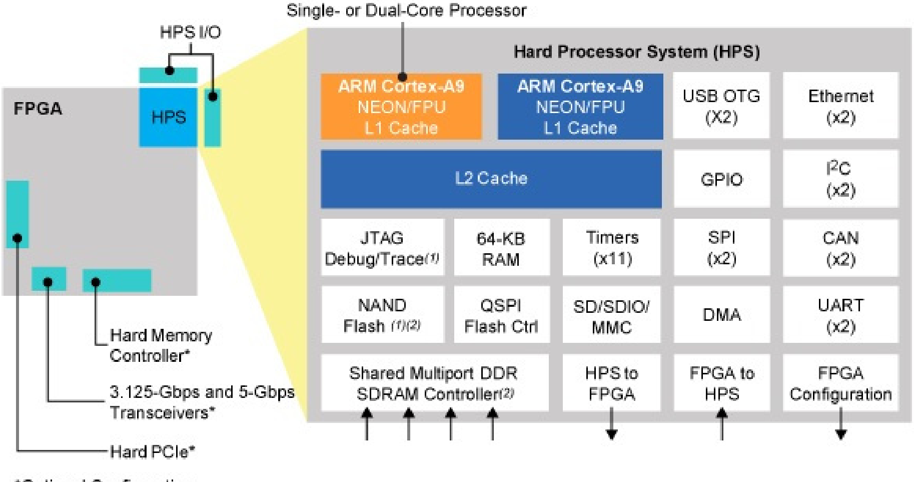
Cyclone V SoC: A Mix of Hard and Soft IP Cores

IP = Intellectual Property

Core = block, design, circuit, etc.

Hard = wires & transistors

Soft = implemented w/ FPGA



*Optional Configuration

Source: Altera

Example IP Cores

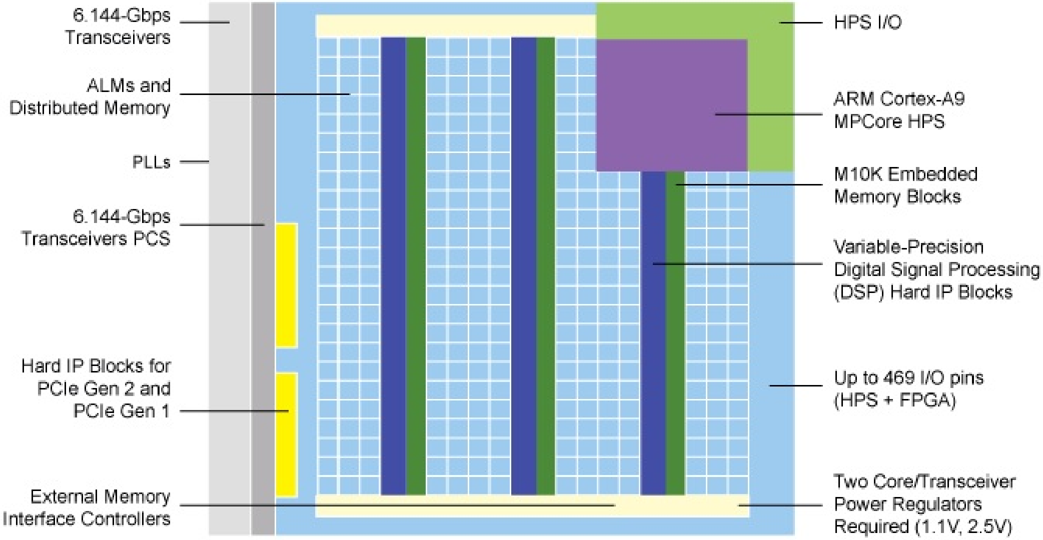
CPUs: ARM (hard), NIOS-II (soft)

Highspeed I/O: Hard IP Blocks for High Speed Transceivers (PCI Express, 10Gb Ethernet)

Memory Controllers: DDR3

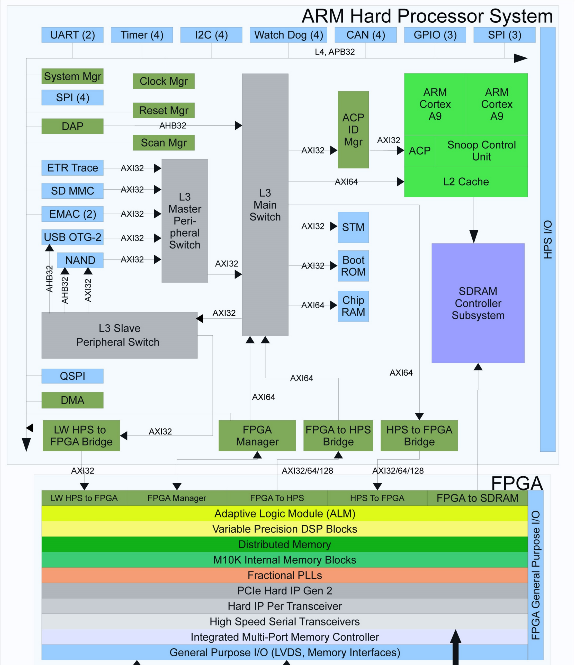
Clock and Reset signal generation: PLLs

Cyclone V SoC: FPGA layout


6.144-Gbps Transceivers
ALMs and Distributed Memory
PLLs
6.144-Gbps Transceivers PCS
Hard IP Blocks for PCIe Gen 2 and PCIe Gen 1
External Memory Interface Controllers
HPS I/O
ARM Cortex-A9 MPCore HPS
M10K Embedded Memory Blocks
Variable-Precision Digital Signal Processing (DSP) Hard IP Blocks
Up to 469 I/O pins (HPS + FPGA)
Two Core/Transceiver Power Regulators Required (1.1V, 2.5V)

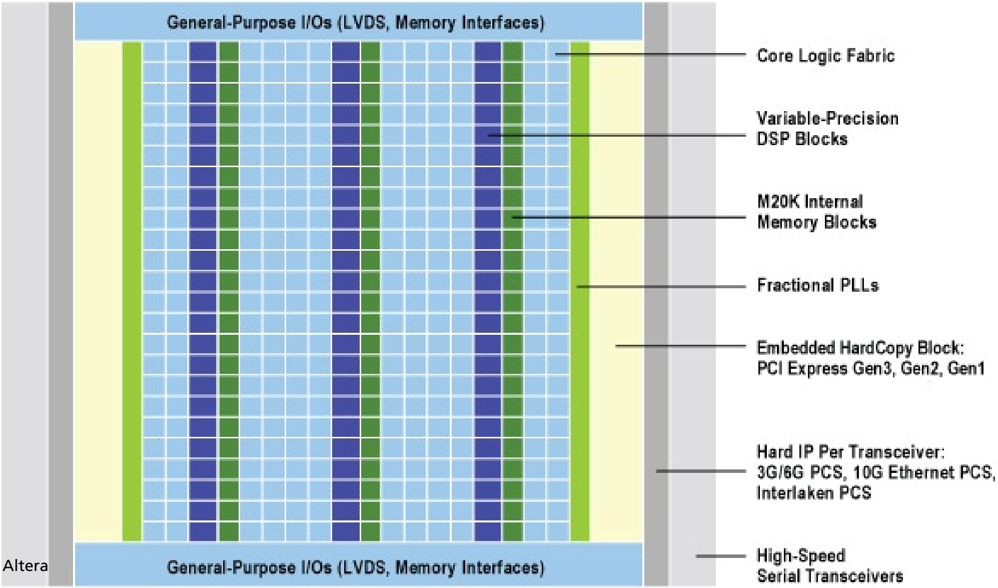
Source: Altera

Cyclone V SoC: HPS Layout



Source: NARD, LLC.

Stratix V: FPGA Layout


General-Purpose I/Os (LVDS, Memory Interfaces)
Core Logic Fabric
Variable-Precision DSP Blocks
M20K Internal Memory Blocks
Fractional PLLs
Embedded HardCopy Block: PCI Express Gen3, Gen2, Gen1
Hard IP Per Transceiver: 3G/6G PCS, 10G Ethernet PCS, Interlaken PCS
High-Speed Serial Transceivers
General-Purpose I/Os (LVDS, Memory Interfaces)

Source: Altera

Bus Bridges

A bus bridge connects two, often different, buses.

Enables multiple clock domains, different protocols (e.g., AXI ↔ Avalon), bus widths, etc.

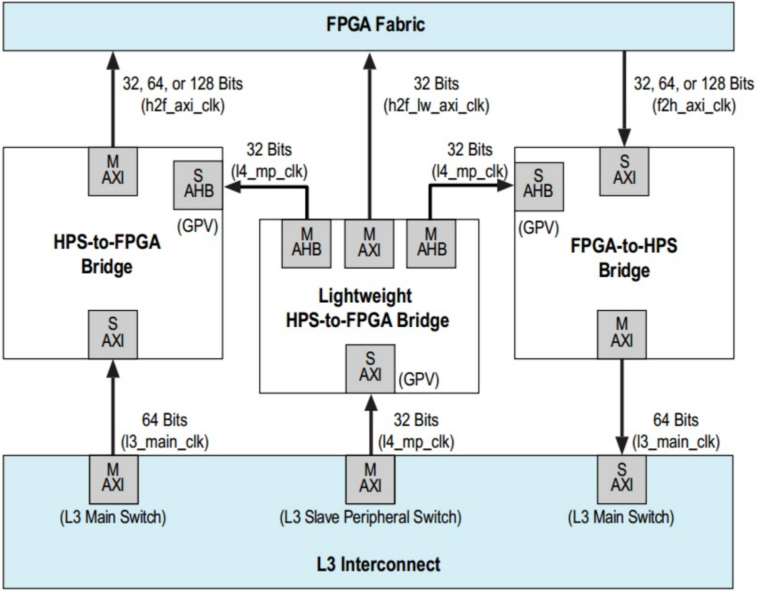
Example Bridge Types:

SOC HPS ↔ FPGA Bridge

Avalon MM Clock Crossing Bridge

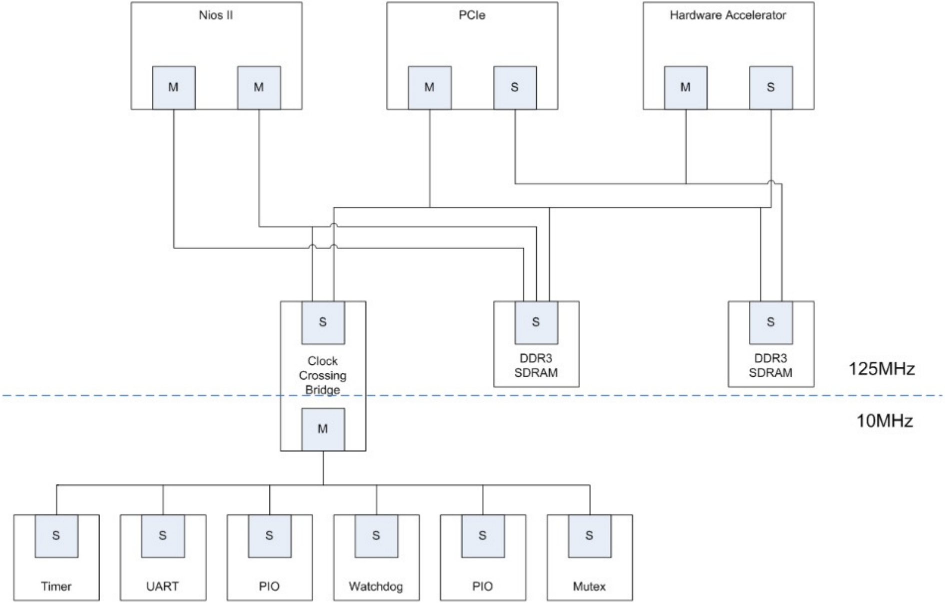
Avalon MM Pipeline Bridge

Cyclone V SoC: FPGA ↔ HPS Bridge



Source: Altera

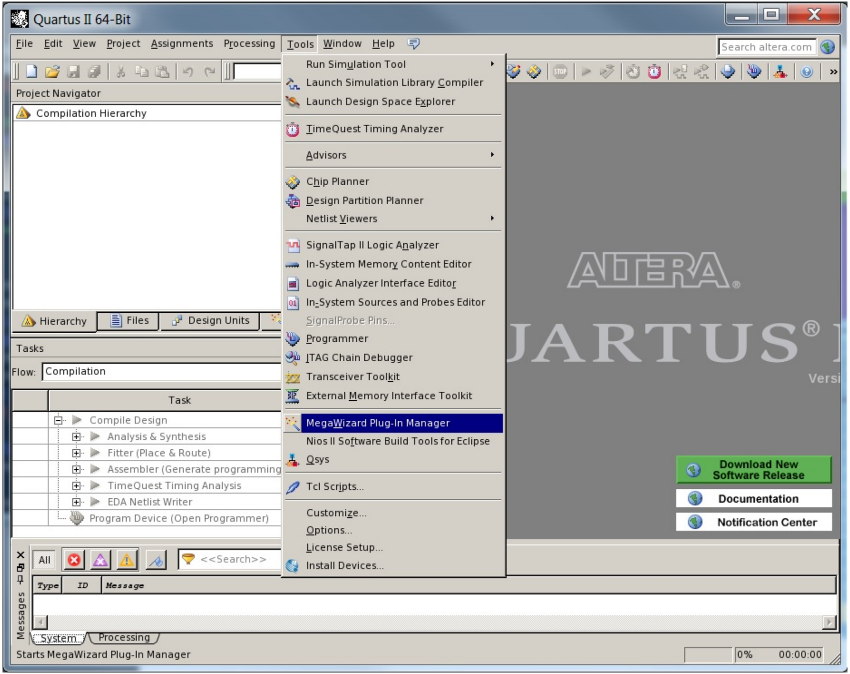
Clock Crossing Bridge Example



Source: Altera

Altera’s IP Core Integration Tools

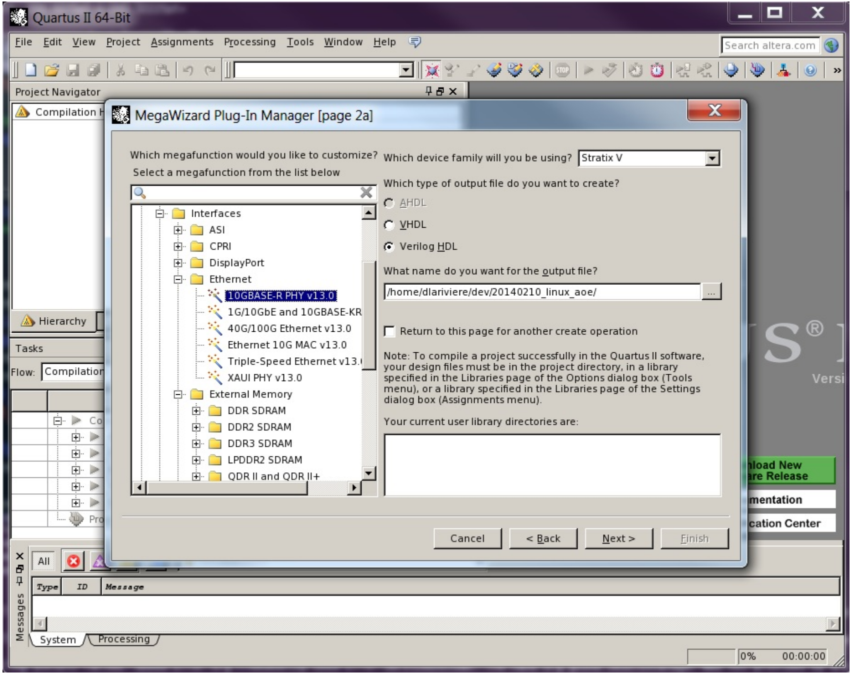
The Quartus Megawizard



Starts MegaWizard Plug-In Manager

Source: Altera

Megawizard Example: 10Gb Ethernet PHY



MegaWizard Plug-In Manager [page 2a]

Which megafunction would you like to customize?
Select a megafunction from the list below

Which device family will you be using? Stratix V

Which type of output file do you want to create?

○ AHDL
○ VHDL
● Verilog HDL

What name do you want for the output file?

/home/dlariviere/dev/20140210_linux_aoe/

□ Return to this page for another create operation

Note: To compile a project successfully in the Quartus II software, your design files must be in the project directory, in a library specified in the Libraries page of the Options dialog box (Tools menu), or a library specified in the Libraries page of the Settings dialog box (Assignments menu).

Your current user library directories are:

Source: Altera

Megawizard IP Cores

Core-specific interfaces on each

Arithmetic: $+$, $-$, $\times$, $\div$, Multiply-Accumulate, ECC

Floating Point: $+$, $-$, $\times$, $\div$

Gate Functions: Shift Registers, Decoders, Multiplexers

I/O Functions: PLL, temp sensor, remote update, high speed transceivers

Memory: Single/Dual-port RAMs, Single/Dual-clock FIFOs, Shift registers

DSP: FFT, ECC, FIR, etc.

Video: large suite

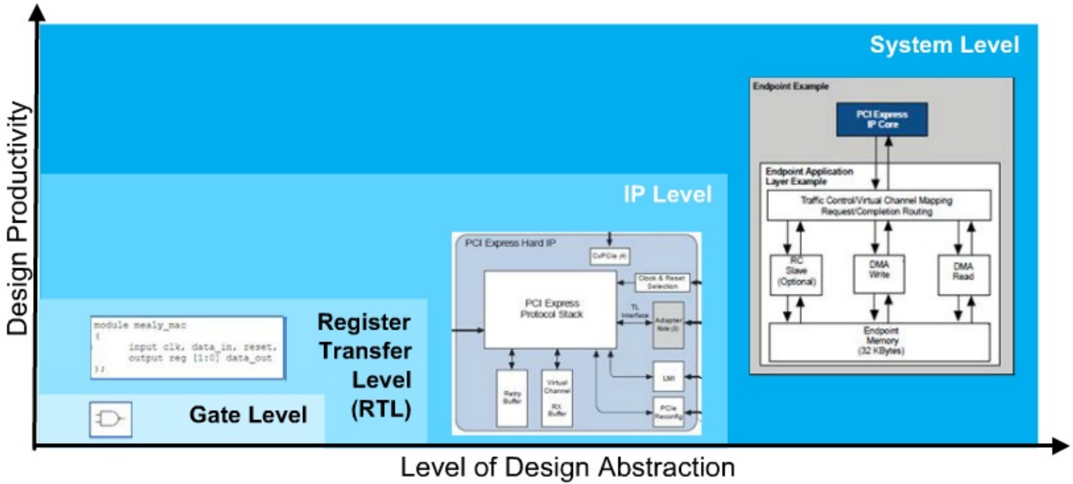
Some megafunctions are only available on certain FPGAs

Qsys/Platform Designer

Platform Designer (formerly Qsys) is Altera’s system integration tool for building Network-on-Chip (NoC) designs connecting multiple IP cores.

You	Qsys
List the IP components and how you want them connected	Generates the interconnect (arbiters, etc.), adds adapters as necessary, warns of errors

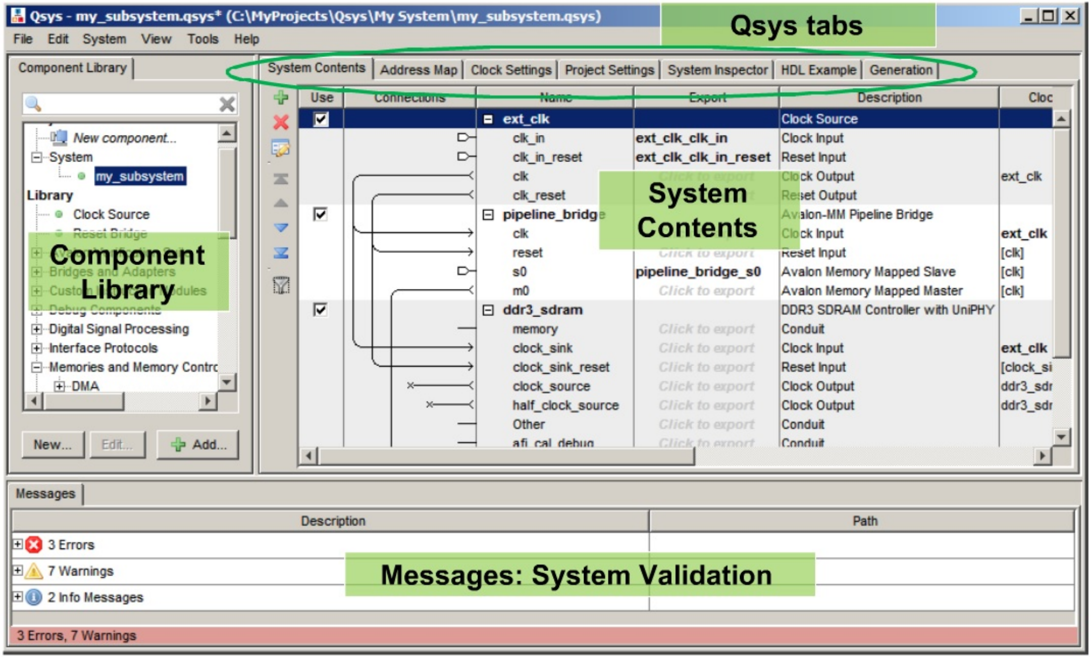
Qsys: Raising Level of Abstraction



```
module mealy_mac
(
        input clk, data_in, reset,
        output reg [1:0] data_out
);
```

ALTERA — Schematic Entry — Quartus II Synthesis — SOPC Builder — Qsys

Source: Altera



Use	Connections	Name	Export	Description	Cloc
☑		⊟ ext_clk		Clock Source	
		clk_in	ext_clk_clk_in	Clock Input	
		clk_in_reset	ext_clk_clk_in_reset	Reset Input	
		clk	Click to export	Clock Output	ext_clk
		clk_reset		Reset Output	
☑		⊟ pipeline_bridge		Avalon-MM Pipeline Bridge	
		clk		Clock Input	ext_clk
		reset	Click to export	Reset Input	[clk]
		s0	pipeline_bridge_s0	Avalon Memory Mapped Slave	[clk]
		m0	Click to export	Avalon Memory Mapped Master	[clk]
☑		⊟ ddr3_sdram		DDR3 SDRAM Controller with UniPHY	
		memory	Click to export	Conduit	
		clock_sink	Click to export	Clock Input	ext_clk
		clock_sink_reset	Click to export	Reset Input	[clock_si
		clock_source	Click to export	Clock Output	ddr3_sdr
		half_clock_source	Click to export	Clock Output	ddr3_sdr
		Other	Click to export	Conduit	
		afi_cal_debug	Click to export	Conduit	

Messages

Description	Path
⊞ 3 Errors	
⊞ 7 Warnings	
⊞ 2 Info Messages	

3 Errors, 7 Warnings

System Level Design: Why Use Qsys

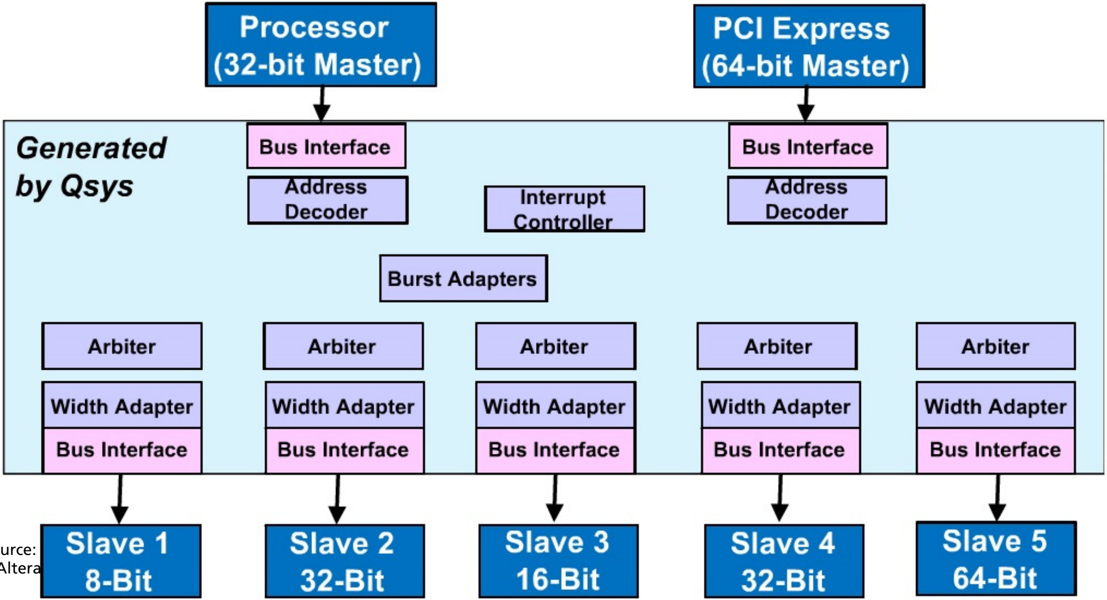
Avoids manually developing custom interconnect fabrics and signaling.

Instead of cycle-to-cycle coordination between every individual IP core, focus on transaction-level designs.

Design IP without knowing exactly when data will transfer and instead only focus on how (once it does).

(Only valid if you design your individual components to one of the standardized interfaces)

Qsys-based Method of Desian



Source:
Altera

Connecting IP Cores

Interface Types

Memory-mapped Interfaces:

Avalon MM (Altera)

AXI (ARM, supported by Qsys now for SoC)

Streaming Interfaces: Avalon ST:

Avalon ST source port: outputs streaming data

Avalon ST sink port: receives incoming streaming data

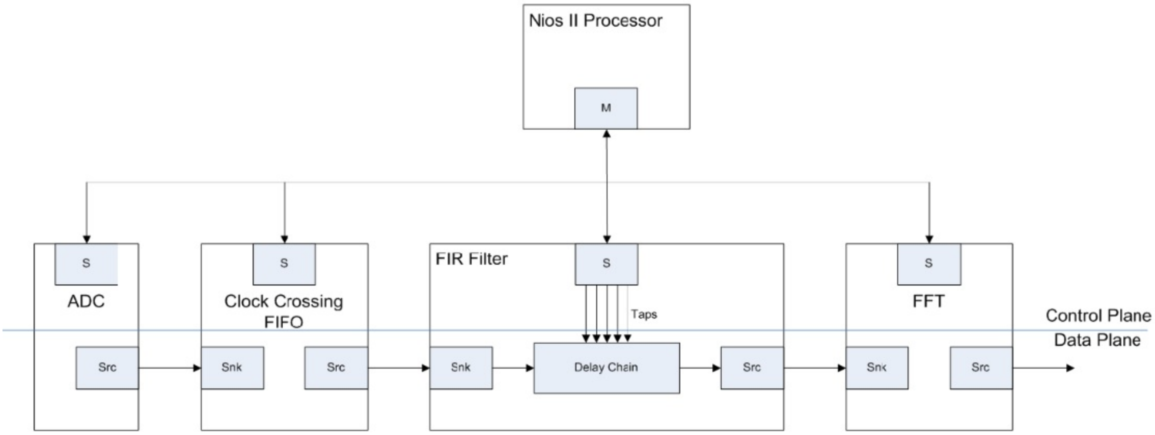
Control vs. Data Planes

Control Plane: Memory mapped registers typically used for configuring devices, querying status, initiating transactions, etc (low bandwidth)

Data Plane: Streaming directed graphs for actually moving and processing large amounts of data (audio/video, network packets, etc); high bandwidth

A single IP core can have both MM and ST interfaces (including multiple of each).

Control and Data Planes Example



Source: Altera

Additional References

Altera online training lectures: (HIGHLY recommended; many of these slides are taken directly from them)

`http://www.altera.com/education/training/curriculum/trn-curriculum.html`

Introduction to Qsys

Advanced System Design Using Qsys

Custom IP Development Using Avalon and AXI Interfaces

(Everything has moved to Intel; above link still works)