Processors, FPGAs, and ASICs
Part 1: Full Custom to PLDs

Stephen A. Edwards

Columbia University

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Spectrum of IC choices

Flexible, efficient

- Full Custom
- ASIC
- Gate Array
- FPGA
- PLD
- GP Processor
- SP Processor
- Multifunction
- Fixed-function

You choose

- Polygons (Intel)
- Circuit (Sony)
- Wires
- Logic network
- Logic function
- Program (e.g., ARM)
- Program (e.g., DSP)
- Settings (e.g., Ethernet Ctrl.)
- Part number (e.g., 74HCT00)

Cheap, quick to design
An N-Channel MOS Transistor
An N-Channel MOS Transistor

Oxide (SiO$_2$)

Gate

Drain (n)  Source (n)

Channel (p)
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO₂)

Gate

Drain (n)  

Source (n)

Channel (p)

3 V

Ammeter
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO$_2$)

Gate

Drain (n) → Source (n)

Channel (p)

3 V

Ammeter
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO$_2$)

Channel (p)

Source (n)

Drain (n)

Ammeter

3 V

0 V
An N-Channel MOS Transistor

![Diagram of an N-Channel MOS Transistor with labels for Gate, Drain, Source, and Channel, along with Oxide (SiO₂). The circuit includes a 3V source, an ammeter, and a Gate set to positive, indicating the transistor is 'On'.]
CMOS Inverter Layout
CMOS Inverter Layout

\[ V_{dd} \]

A \hspace{2cm} Y

\[ V_{ss} \]
CMOS Inverter Layout

Cross Section Through N-channel FET

Top View
The CMOS NAND Gate

Two-input NAND gate:

A
B
Y
The CMOS NAND Gate

Two-input NAND gate:
two n-FETs in series;
The CMOS NAND Gate

Two-input NAND gate:
two n-FETs in series;
two p-FETs in parallel
The CMOS NAND Gate

Both inputs 1:
Both n-FETs turned on
Output pulled low
Both p-FETs turned off
One input 1, the other 0:
One p-FET turned on
Output pulled high
One n-FET turned on, but does not control output
The CMOS NAND Gate

Both inputs 0:
Both p-FETs turned on
Output pulled high
Full Custom: Intel 4004 Masks (2,250 Transistors)
Full Custom: Intel 4004 Die Photograph
Standard Cell ASICs
Standard Cell
ASICs
### Channeled Gate Arrays

<table>
<thead>
<tr>
<th>Underpasses</th>
<th>NFETs PFETs</th>
<th>Gates</th>
<th>Ground/Power</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;ss&lt;/sub&gt; V&lt;sub&gt;dd&lt;/sub&gt;</td>
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</table>

- **Big N**
- **Big P**
- **Protection Diode**
Sea-of-Gates
Gate Arrays
FPGAs: Floorplan
FPGAs: CLB
FPGAs: Routing

Single-length line Switch Matrix connections

SIX PASS TRANSISTORS PER SWITCH MATRIX INTERCONNECT POINT

Double-length lines in CLB array
PLAs/CPLDs:
The 22v10