DIGITAL INSTRUMENT MULTI-EFFECTS PROCESSING UNIT DESIGN DOCUMENT

CSEE 4840

Contents

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Block Diagram

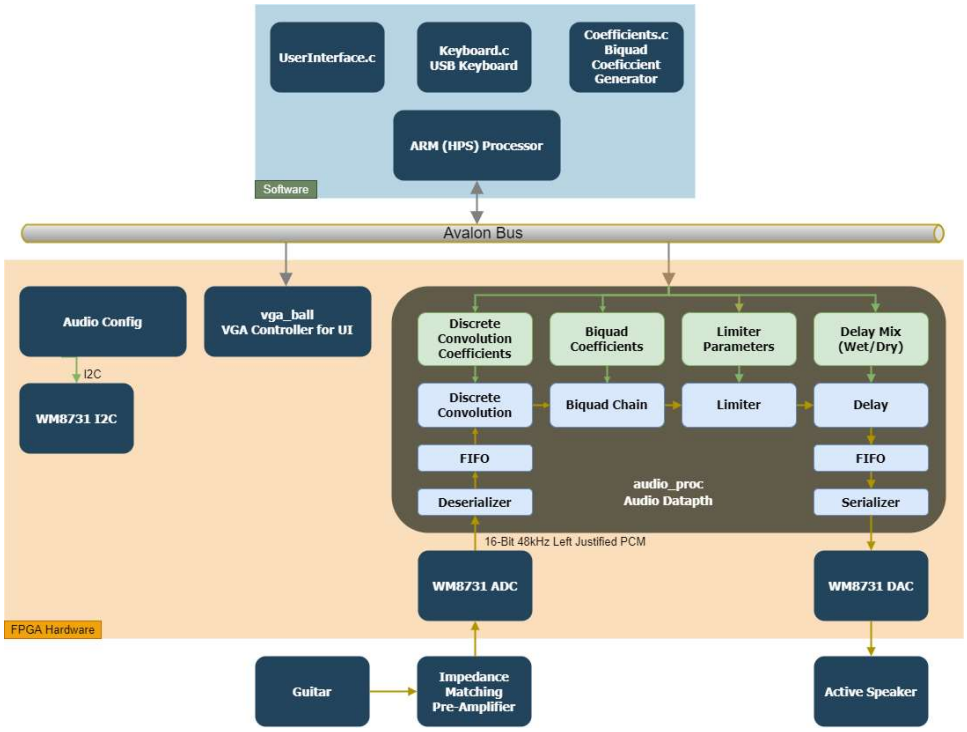

Figure 1: Block Diagram

The proposed system consists of two major parts including the hardware audio data path and software control implemented on the DE1-SOC.

Audio samples are sourced from the line-in input of the WM8731 Codec on the DE-1 SOC board. The ADC on the WM8731 sends serial PCM audio data in 16-bit 48kHz Left Justified format to the FPGA. A deserializer is used to convert the audio data into a parallel format and store them into FIFO registers to be processed. Following the FIFO will be the various signal processing hardware, connected by Avalon Streaming Interface, including a discrete convolution block, a series of biquads, a limiter, and a delay block. The blocks are connected in series and there is a bypass control for each block to turn the effect on or off in the software. The parameters used in the blocks such as gain, biquad coefficients, and discrete convolution coefficients will be configured through the Avalon Memory-Mapped bus by the software. At the end of the Datapath will be a serializer to convert the audio data into the 16-bit 48kHz Left Justified format supported by the DAC of the WM8731.

To configure the effects, a VGA user interface is implemented using sprites with various sliders to control parameters such as mixing ratio and delay length. The software receives user input from a USB keyboard, controls the display content, and configures parameters such as biquad coefficients in the audio data path.

Additional analog hardware, the Impedance Matching Pre-Amplifier, is required to connect the guitar to the WM7831's Line-In due to the guitar's high output impedance and low output voltage swing. The analog hardware is a two-stage amplifier with a high input impedance at the first stage and a programmable gain at the second stage.

Algorithms

Four algorithms (guitar effects) are implemented in this project including Cabinet IR, EQ, hard-clip, and delay.

Cabinet IR

The Cabinet IR effect is the discrete convolution of the audio signal with an impulse response signal to recreate the sound of a particular speaker cabinet. In this project, a pipelined FIR filter is used to perform discrete convolution with a set of coefficients set by software with the input audio signal.

$$y[n] = \sum_{k=-\infty}^{\infty} x[k]h[n-k]$$

Equation 1: Discrete Convolution

Biquad Chain

Biquads are second-order IIR filter units that are used to create analog filters such as peaking, shelving, etc. Each biquad has five coefficients, as shown in Equation 2. The time-domain difference equation implemented in Verilog for each biquad is shown in Equation 3. A three-band EQ is implemented with a chain of such biquads to adjust bass, mid, and treble.

$$H(z) = \frac{Y(z)}{X(z)} = \frac{a_0 + a_1 Z^{-1} + a_2 Z^{-2}}{1 + b_1 Z^{-1} + b_2 Z^{-2}}$$

Equation 2: Biquad Transfer Function

$$y[n] = \left(\frac{b_0}{a_0}\right)x[n] + \left(\frac{b_1}{a_0}\right)x[n-1] + \left(\frac{b_2}{a_0}\right)x[n-2] - \left(\frac{a_1}{a_0}\right)y[n-1] - \left(\frac{a_2}{a_0}\right)y[n-2]$$

Equation 3: Biquad Difference Equation.

Limiter

The limiter clips the audio signal above a certain threshold, adding distortion, which is desired in electric guitars. Two forms of clipping are implemented. The first is a hard clip, which places a hard limit on the signal's amplitude. The second is a soft clip, which is implemented by combining the hardclip with a low pass biquad to remove the sharp edges.

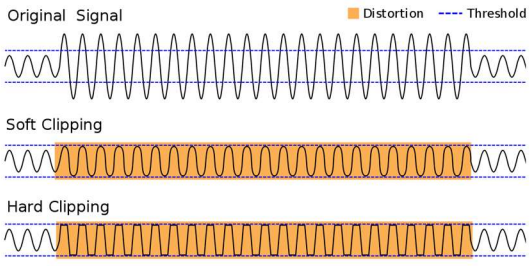

Figure 2: Limiter

Delay

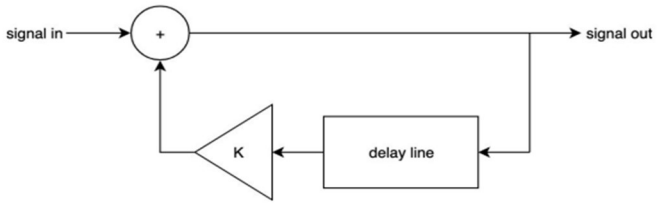

Figure 3: Delay Effect

The delay block implements the data path shown in Figure 3. Some audio data is stored in FIFO to be delayed (wet) and are mixed with samples that have not been delayed (dry). The mixing factor K determines how much wet signal is added to the output, which can be set by software/UI.

Resource Budget

On-Chip BRAM Budget					
	INPUT FIFO LEFT	**INPUT FIFO RIGHT**	**FIR FIFO**	**FIR COEFF**	**VGA SPRITE**
SAMPLES (WORD)	128	128	500	500	640x480
MEMORY (BIT)	128x16	128x16	500x16	500x16	640x480x8
			TOTAL	**2478/4460Kb**	**55.6%**

Table 1: BRAM Budget

DSP BLOCK Budget			
		FIR	**BIQUAD**
BLOCKS USED		2	20
	TOTAL	**22/87**	**25.29%**

Table 2: DSP BLOCK BUDGET

Hardware/Software Interface

Each effect block has Avalon Memory-Mapped registers.

Cabinet IR

- Address: 0x0000_1000 - 0x0000_13ff
- 500 FIR Coefficients

Biquad Chain

- Address: 0x0000_0100 - 0x0000_013f
- Reg 0~4: BIQUAD 1 COEFF
- Reg 5~9: BIQUAD 2 COEFF
- Reg 10~14: BIQUAD 3 COEFF
- Reg 15~19: BIQUAD 4 COEFF
- Reg 20: BYPASS

Limiter

- Address: 0x0000_0010 - 0x0000_001f
- Reg 0: CLIP THRESHOLD POS
- Reg 1: CLIP THRESHOLD NEG

Delay

- Address: 0x0000_0020 - 0x0000_002f
- Reg 0: BYPASS
- Reg 1: DELAY LENGTH
- Reg 2: MIX

VGA Ball

- Address: 0x0000_2000 - 0x0000_200f
- Reg 0: BYPASS SWITCH POSITION
- Reg 1: PRESET SELECT POSITION
- Reg 2: SLIDER 1 POSITION
- Reg 3: SLIDER 2 POSITION
- Reg 4: SLIDER 3 POSITION
- Reg 5: SLIDER 4 POSITION
- Reg 6: SLIDER 5 POSITION
- Reg 7: SLIDER 6 POSITION