Processors, FPGAs, and ASICs
Part 1: Full Custom to PLDs

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Spring 2020
<table>
<thead>
<tr>
<th>Spectrum of IC choices</th>
<th>You choose</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Flexible, efficient</strong></td>
<td></td>
</tr>
<tr>
<td>Full Custom</td>
<td>Polygons (Intel)</td>
</tr>
<tr>
<td>ASIC</td>
<td>Circuit (Sony)</td>
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<tr>
<td>Gate Array</td>
<td>Wires</td>
</tr>
<tr>
<td>FPGA</td>
<td>Logic network</td>
</tr>
<tr>
<td>PLD</td>
<td>Logic function</td>
</tr>
<tr>
<td>GP Processor</td>
<td>Program (e.g., ARM)</td>
</tr>
<tr>
<td>SP Processor</td>
<td>Program (e.g., DSP)</td>
</tr>
<tr>
<td>Multifunction</td>
<td>Settings (e.g., Ethernet Ctrl.)</td>
</tr>
<tr>
<td>Fixed-function</td>
<td>Part number (e.g., 74HCT00)</td>
</tr>
<tr>
<td><strong>Cheap, quick to design</strong></td>
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</table>
An N-Channel MOS Transistor
An N-Channel MOS Transistor

Oxide (SiO$_2$)

Gate

Drain (n)  Source (n)

Channel (p)
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO₂)

Drain (n)  Source (n)

Channel (p)

Ammeter

3 V
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO\textsubscript{2})

Gate

Drain (n) 

Source (n)

Channel (p)

3 V

Ammeter

Gate at 0V: Off
An N-Channel MOS Transistor

Gate at 0V: Off

Oxide (SiO$_2$)

Drain (n) Source (n)

Channel (p)

Ammeter

3 V

0 V
An N-Channel MOS Transistor

Gate positive: On

Oxide (SiO₂)

Drain (n)  Source (n)

Channel (p)

Ammeter

3 V
CMOS Inverter Layout
CMOS Inverter Layout

Cross Section Through N-channel FET
The CMOS NAND Gate

Two-input NAND gate:

A
B

Y
Two-input NAND gate:
Two n-FETs in series;
The CMOS NAND Gate

Two-input NAND gate:
- two n-FETs in series;
- two p-FETs in parallel
The CMOS NAND Gate

Both inputs 1:
- Both n-FETs turned on
- Output pulled low
- Both p-FETs turned off
The CMOS NAND Gate

One input 1, the other 0:
One p-FET turned on
Output pulled high
One n-FET turned on, but does not control output
The CMOS NAND Gate

Both inputs 0:
Both p-FETs turned on
Output pulled high
Full Custom: Intel 4004 Masks (2,250 Transistors)
Full Custom: Intel 4004 Die Photograph
Standard Cell ASICs
## Channeled Gate Arrays

<table>
<thead>
<tr>
<th>Underpasses</th>
<th>NFETs PFETs</th>
<th>Gates</th>
<th>Ground/Power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{ss}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{dd}$</td>
</tr>
</tbody>
</table>

**Diagram:**

- **Underpasses**
- **NFETs PFETs**
- **Gates**
- **Ground/Power**
- **Protection Diode**
- **Bonding Pad**
- **Big N**
- **Big P**
Channeled Gate Arrays
Sea-of-Gates
Gate
Arrays
FPGAs: Floorplan
FPGAs: CLB

Diagram showing the CLB (Configurable Logic Block) with inputs and outputs labeled.
FPGAs: Routing

Single-length line Switch Matrix connections

Six pass transistors per switch matrix interconnect point

Double-length lines in CLB array

Switch matrices
PLAs/CPLDs: The 22v10

Asynchronous Reset (to all registers)