Hardware-Software Interfaces
CSEE W4840

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Processor System Block Diagram

- Processor
- Address Bus
- Data Bus
- Memory
- Peripheral
- Peripheral
Simple Bus Timing

### Read Cycle

- **R/W**: Switch signal
- **Enable**: Enable signal
- **Addr**: Address signal
- **Data**: Data signal

### Write Cycle

- **R/W**: Switch signal
- **Enable**: Enable signal
- **Addr**: Address signal
- **Data**: Data signal
Strobe vs. Handshake

Strobe

Req

Data

Handshake

Req

Ack

Data
1982: The IBM PC/XT
The ISA Bus: Memory Read
The ISA Bus: Memory Write
The PC/104 Form Factor: ISA Lives

Embedded System Legos. Stack ’em and go.
Memory-Mapped I/O

- To a processor, everything is memory.
- Peripherals appear as magical memory locations.
- Status registers: when read, report state of peripheral
- Control registers: when written, change state of peripheral
Typical Peripheral: PC Parallel Port

At Standard TTL Levels

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Adapter Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strobe</td>
<td>1</td>
</tr>
<tr>
<td>E</td>
<td>2</td>
</tr>
<tr>
<td>X</td>
<td>3</td>
</tr>
<tr>
<td>T</td>
<td>4</td>
</tr>
<tr>
<td>E</td>
<td>5</td>
</tr>
<tr>
<td>R</td>
<td>6</td>
</tr>
<tr>
<td>N</td>
<td>7</td>
</tr>
<tr>
<td>A</td>
<td>8</td>
</tr>
<tr>
<td>L</td>
<td>9</td>
</tr>
<tr>
<td>Acknowledge</td>
<td>10</td>
</tr>
<tr>
<td>Busy</td>
<td>11</td>
</tr>
<tr>
<td>E</td>
<td>12</td>
</tr>
<tr>
<td>V</td>
<td>13</td>
</tr>
<tr>
<td>I</td>
<td>14</td>
</tr>
<tr>
<td>C</td>
<td>15</td>
</tr>
<tr>
<td>E</td>
<td>16</td>
</tr>
<tr>
<td>Select Input</td>
<td>17</td>
</tr>
<tr>
<td>Ground</td>
<td>18-25</td>
</tr>
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</table>

Strobe

Busy

Ack

Data
Parallel Port Registers

<table>
<thead>
<tr>
<th></th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Busy</td>
<td>Ack</td>
<td>Paper</td>
<td>Sel</td>
<td>Err</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x378</td>
</tr>
<tr>
<td>Sel</td>
<td>Init</td>
<td>Auto</td>
<td>Strobe</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x379</td>
</tr>
<tr>
<td></td>
<td>Sel</td>
<td>Init</td>
<td>Auto</td>
<td>Strobe</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x37A</td>
</tr>
</tbody>
</table>

1. Write Data
2. Assert Strobe
3. Wait for Busy to clear
4. Wait for Acknowledge
A Parallel Port Driver

```
#define DATA       0x378
#define STATUS     0x379
#define CONTROL    0x37A
#define NBSY       0x80
#define NACK       0x40
#define OUT        0x20
#define SEL        0x10
#define NERR       0x08
#define STROBE     0x01

#define INVERT     (NBSY | NACK | SEL | NERR)
#define MASK       (NBSY | NACK | OUT | SEL | NERR)
#define NOT_READY(x) ((inb(x)^INVERT)&MASK)

void write_single_character(char c) {
  while (NOT_READY(STATUS)) ;
  outb(DATA, c);
  outb(CONTROL, control | STROBE); /* Assert STROBE */
  outb(CONTROL, control ); /* Clear STROBE */
}
```
The Parallel Port Schematic
Interrupts and Polling

Two ways to get data from a peripheral:

- Polling: “Are we there yet?”
- Interrupts: Ringing Telephone
Interrupts

Basic idea:

1. Peripheral asserts a processor’s interrupt input
2. Processor temporarily transfers control to interrupt service routine
3. ISR gathers data from peripheral and acknowledges interrupt
4. ISR returns control to previously-executing program
Many Different Interrupts

What’s a processor to do?
Many Different Interrupts

What’s a processor to do? ISR polls all potential interrupt sources, then dispatches handler.
Prioritizes incoming requests & notifies processor
ISR reads 8-bit interrupt vector number of winner
IBM PC/AT: two 8259s; became standard