CDP1802 COSMAC Microprocessor

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Overview

- 1802 ISA, Memory, CPU
- Timing Diagrams
- Hardware-Software interface
- Testing & Debugging
ISA

- Memory reference
- Register operations
- Logic operations
- Arithmetic operations
- Control flow (branch, long branch, skip, long skip)
- (I/O byte transfer) -- not implemented
# 1802 Instruction Matrix

<table>
<thead>
<tr>
<th>N</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>IDL</td>
<td>1</td>
<td>INCREMENT RN (INC)</td>
<td>2</td>
<td>DECREMENT RN (DEC)</td>
<td>3</td>
<td>BRANCH ON Q, Z, DF</td>
<td>4</td>
<td>LOAD-ADVANCE RN (LDA)</td>
<td>5</td>
<td>STORE VIA RN (STR)</td>
<td>6</td>
<td>OUTPUT</td>
<td>INPUT</td>
<td>7</td>
</tr>
<tr>
<td>I</td>
<td>8</td>
<td>GET LOW BYTE OF RN (GLO)</td>
<td>9</td>
<td>GET HIGH BYTE OF RN (GHI)</td>
<td>A</td>
<td>SET LOW BYTE OF RN (PLO)</td>
<td>B</td>
<td>SET HIGH BYTE OF RN (PHI)</td>
<td>C</td>
<td>LONG BRANCH</td>
<td>9</td>
<td>NOP</td>
<td>LONG SKIP</td>
<td>LONG BRANCH</td>
<td>LONG SKIP</td>
<td>1</td>
</tr>
</tbody>
</table>
Memory

- Dual-port RAM (4KB)
  - using Altera Megawizard
  - Single clock
  - single-cycle access
  - new data on same-port read-during-write
- 32 16-bit all-purpose registers
- D, N, I, P, T, X, DF, ALU
- We used more flip-flops...
CPU design

- 4 clock cycles per machine cycle
- LOAD, RESET, RUN, PAUSE modes
  - In run mode: FETCH, EXECUTE, EXECUTE2 states
Graphics

- (incomplete)
- VGA displays 64x32 resolution
- Framebuffer implemented with Megawizard dual-port RAM
- Requires 1x2048-bit RAM
  - use only 1 bit for on/off, rather than 8-bit luminance
Timing diagrams
Original CDP1802 timing, Group 1 instructions
Instruction set timing: Group 1 Read/Non-memory, Group 2 Read/Read
Instruction set timing: Group 3 Read/Write
Instruction set timing: Group 4 Read/Read/Read, Group 2 Read/Non-memory/Non-memory
Hardware-software interface

- Avalon Memory-Mapped Port reads from/writes to RAM
- Linux Device driver
  - dtb specification generated from sopc file
  - ioctls for 8-bit read/write and burst 32-bit read/write
- User-space programs using device driver
Debugging & Testing

Test program

- DE1-SoC via LEDs, device driver
  - View register, address line, memory before and after execution

- TinyELF
  - Check verilator behavior against 1802 emulator
  - Step through memory state, registers, address/bus lines

- debug implementation
E4 :: x = 4
24 :: R(4) = FF
84 :: D = R(4).0 = FF
B3 :: R(3) = FF00
22 :: R(2) = FEFF
93 :: D = R(3).1 = FE
E0 : D = 0
1a : R(a) = 1
1a : R(a) = 2
8a : D = R(a) = 2
5a : M(2) = 2