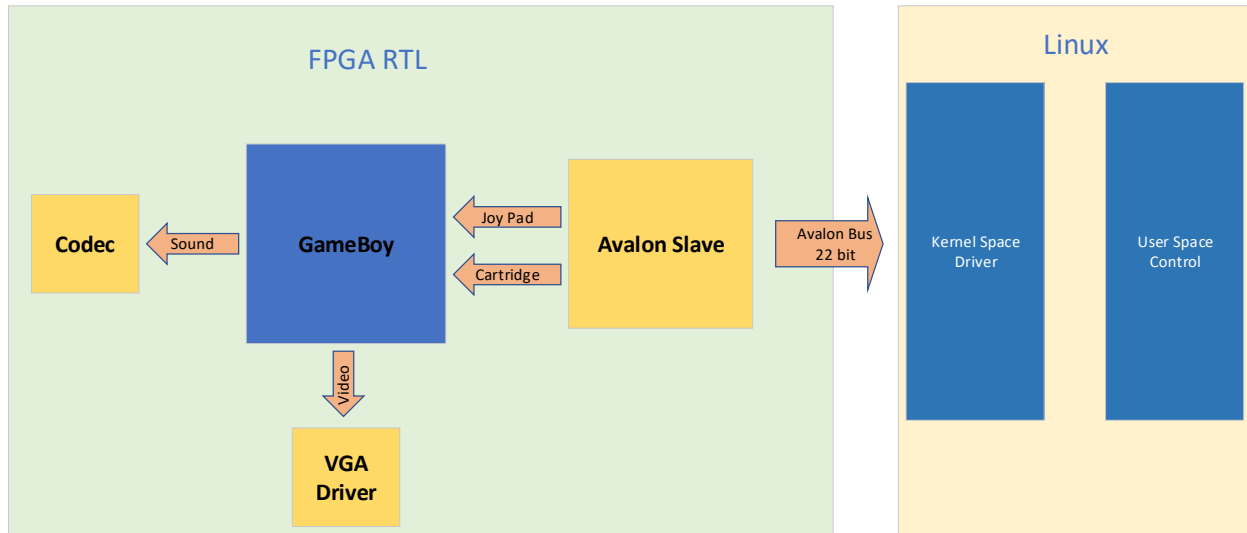


GameBoy – Project Design

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Top level block diagram



Hardware part:

1. Gameboy CPU (GB-Z80)
2. Sound Peripheral + Codec
3. Pixel Processing Unit + VGA Driver
4. Avalon Interface for receiving Joy Pad control and Cartridge Data

GameBoy game cartridge roms are 14-bit wide plus joypad control and other functions, a 22-bit wide Avalon Bus should be enough.

Software side on linux should handle controller input and load the game cartridge into FPGA's block ram.

GameBoy Technical Data

CPU: Z80 Like 8 bit

Main RAM: 8K Byte

Video RAM: 8K Byte

Screen Size 2.6" Resolution: 160x144 (20x18 tiles) **(We map this to 4x: 640x576)**

Max # of sprites: 40 Max

sprites/line: 10 Max

sprite size: 8x16

Min sprite size: 8x8

Clock Speed: 4.194304 MHz (2^{22} Hz)

Horiz Sync: 9198 KHz

Vert Sync: 59.73 Hz

Sound: 4 channels with stereo sound

GameBoy Internal MMIO

Interrupt Enable Register

----- FFFF

Internal RAM

----- FF80

Empty but unusable for I/O

----- FF4C

I/O ports

----- FF00

Empty but unusable for I/O

----- FEA0

Sprite Attribute Memory (OAM)

----- FE00

Echo of 8kB Internal RAM

----- E000

8kB Internal RAM

----- C000

8kB switchable RAM bank

----- A000

8kB Video RAM

----- 8000

16kB switchable ROM bank 6000

----- 4000

16kB ROM bank #0 2000

----- 0000

Reserved Memory Locations (After Bootstrap)

0000	Restart \$00 Address (RST \$00 calls this address. Where Boot Sequence starts)
0008	Restart \$08 Address (RST \$08 calls this address.)
0010	Restart \$10 Address (RST \$10 calls this address.)
0018	Restart \$18 Address (RST \$18 calls this address.)
0020	Restart \$20 Address (RST \$20 calls this address.)
0028	Restart \$28 Address (RST \$28 calls this address.)
0030	Restart \$30 Address (RST \$30 calls this address.)
0038	Restart \$38 Address (RST \$38 calls this address.)
0040	Vertical Blank Interrupt Start Address
0048	LCDC Status Interrupt Start Address
0050	Timer Overflow Interrupt Start Address
0058	Serial Transfer Completion Interrupt Start Address (Link)
0060	High-to-Low of P10-P13 Interrupt Start Address (Joy Pads)

An internal information area is located at 0100-014F in each cartridge. It contains the following values:

0100-0103 This is the begin code execution point in a cart. Usually there is a NOP and a JP instruction here but not always.

0104-0133 Scrolling Nintendo graphic:

```
CE ED 66 66 CC 0D 00 0B 03 73 00 83 00 0C 00 0D
```

```
00 08 11 1F 88 89 00 0E DC CC 6E E6 DD DD D9 99
```

```
BB BB 67 63 6E 0E EC CC DD DC 99 9F BB B9 33 3E
```

(PROGRAM WON'T RUN IF CHANGED!!!)

0134-0142 Title of the game in UPPER CASE ASCII. If it is less than 16 characters then the remaining bytes are filled with 00's.

0143 \$80 = Color GB, \$00 or other = not Color GB **(Should be 00 in our case)**

- 0144 Ascii hex digit, high nibble of licensee code (new).
- 0145 Ascii hex digit, low nibble of licensee code (new). (These are normally \$00 if [\$014B] != \$33.)
- 0146 GB/SGB Indicator (00 = GameBoy, 03 = Super GameBoy functions)
(Super GameBoy functions won't work if != \$03.)
- 0147 Cartridge type:
- 0 - ROM ONLY
 - 1 - ROM+MBC1
 - 2 - ROM+MBC1+RAM
 - 3 - ROM+MBC1+RAM+BATT
 - 5 - ROM+MBC
 - 6 - ROM+MBC2+BATTERY
 - 8 - ROM+RAM
 - 9 - ROM+RAM+BATTERY
 - B - ROM+MMM01
 - C - ROM+MMM01+SRAM
 - D - ROM+MMM01+SRAM+BATT
 - F - ROM+MBC3+TIMER+BATT
 - 10 - ROM+MBC3+TIMER+RAM+BATT
 - 11 - ROM+MBC312 - ROM+MBC3+RAM
 - 13 - ROM+MBC3+RAM+BATT
 - 19 - ROM+MBC5 (MBC5 for Pokemon Yellow)
 - 1A - ROM+MBC5+RAM
 - 1B - ROM+MBC5+RAM+BATT
 - 1C - ROM+MBC5+RUMBLE
 - 1D - ROM+MBC5+RUMBLE+SRAM

1E - ROM+MBC5+RUMBLE+SRAM+BATT

1F - Pocket Camera

FD - Bandai TAMA5

FE - Hudson HuC-3

FF - Hudson HuC-1

0148 ROM size:

0 - 256Kbit = 32KByte = 2 banks

1 - 512Kbit = 64KByte = 4 banks

2 - 1Mbit = 128KByte = 8 banks

3 - 2Mbit = 256KByte = 16 banks

4 - 4Mbit = 512KByte = 32 banks

5 - 8Mbit = 1MByte = 64 banks

6 - 16Mbit = 2MByte = 128 banks

\$52 - 9Mbit = 1.1MByte = 72 banks

\$53 - 10Mbit = 1.2MByte = 80 banks

\$54 - 12Mbit = 1.5MByte = 96 banks

0149 RAM size:

0 - None

1 - 16kBit = 2kB = 1 bank

2 - 64kBit = 8kB = 1 bank

3 - 256kBit = 32kB = 4 banks

4 - 1MBit = 128kB = 16 banks

014A Destination code:

0 - Japanese

1 - Non-Japanese

014B Licensee code (old):

33 - Check 0144/0145 for Licensee code.

79 - Accolade

A4 – Konami

(Super GameBoy function won't work if != \$33.)

014C Mask ROM Version number (Usually \$00)

014D Complement check

(PROGRAM WON'T RUN ON GB IF NOT CORRECT!!!)

(It will run on Super GB, however, if incorrect.)

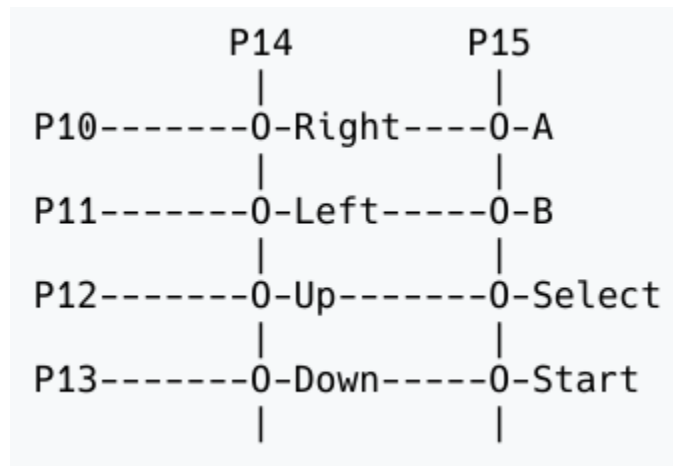
014E-014F Checksum (higher byte first) produced by adding all bytes of a cartridge except for two checksum bytes and taking two lower bytes of the result. (GameBoy ignores this value.)

MMIO Registers

FF00

Name	- P1
Contents	- Register for reading joy pad info and determining system type. (R/W)
Bit 7	- Not used
Bit 6	- Not used
Bit 5	- P15 out port
Bit 4	- P14 out port
Bit 3	- P13 in port
Bit 2	- P12 in port
Bit 1	- P11 in port
Bit 0	- P10 in port

This is the matrix layout for register \$FF00:



FF01

Name	- SB
Contents	- Serial transfer data (R/W)
	8 Bits of data to be read/written

FF02 SC Serial IO control

FF02

Name	- SC
------	------

Contents - SIO control (R/W)

Bit 7 - Transfer Start Flag

0: Non transfer

1: Start transfer

Bit 0 - Shift Clock

0: External Clock (500KHz Max.)

1: Internal Clock (8192Hz)

FF04

Name - DIV

Contents - Divider Register (R/W)

FF05

Name - TIMA

Contents - Timer counter (R/W)

FF06

Name - TMA

Contents - Timer Modulo (R/W)

FF07

Name - TAC

Contents - Timer Control (R/W)

Bit 2 - Timer Stop

0: Stop Timer

1: Start Timer

Bits 1+0 - Input Clock Select

00: 4.096 KHz (~4.194 KHz SGB)

01: 262.144 KHz (~268.4 KHz SGB)

10: 65.536 KHz (~67.11 KHz SGB)

11: 16.384 KHz (~16.78 KHz SGB)

FF0F

Name - IF

Contents - Interrupt Flag (R/W)

Bit 4: Transition from High to Low of Pin number P10-P13

Bit 3: Serial I/O transfer complete

Bit 2: Timer Overflow

Bit 1: LCDC (see STAT)

Bit 0: V-Blank

FF10

Name - NR 10

Contents - Sound Mode 1 register, Sweep register (R/W)

Bit 6-4 - Sweep Time

Bit 3 - Sweep Increase/Decrease

0: Addition (frequency increases)

1: Subtraction (frequency decreases)

Bit 2-0 - Number of sweep shift (n: 0-7)

FF11

Name - NR 11

Contents - Sound Mode 1 register, Sound length/Wave pattern duty (R/W)

Only Bits 7-6 can be read.

Bit 7-6 - Wave Pattern Duty

Bit 5-0 - Sound length data (t1: 0-63)

```
Wave Duty: 00: 12.5% ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ )
            01: 25%  ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ )
            10: 50%  ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ ) (default)
            11: 75%  ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ )
```

FF12

Name - NR 12

Contents - Sound Mode 1 register, Envelope (R/W)

Bit 7-4 - Initial volume of envelope

Bit 3 - Envelope UP/DOWN

0: Attenuate

1: Amplify

Bit 2-0 - Number of envelope sweep (n: 0-7)

(If zero, stop envelope operation.)

FF13

Name - NR 13

Contents - Sound Mode 1 register, Frequency lo (W)

Lower 8 bits of 11 bit frequency (x).

Next 3 bit are in NR 14 (\$FF14)

FF14

Name - NR 14

Contents - Sound Mode 1 register, Frequency hi (R/W)

Only Bit 6 can be read.

Bit 7 - Initial (when set, sound restarts)

Bit 6 - Counter/consecutive selection

Bit 2-0 - Frequency's higher 3 bits (x)

FF16

Name - NR 21

Contents - Sound Mode 2 register, Sound Length; Wave Pattern Duty (R/W)

Only bits 7-6 can be read.

Bit 7-6 - Wave pattern duty

Bit 5-0 - Sound length data (t1: 0-63)

```
Wave Duty: 00: 12.5% ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ )
           01: 25%  ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ )
           10: 50%  ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ ) (default)
           11: 75%  ( _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ )
```

FF17

Name - NR 22

Contents - Sound Mode 2 register, envelope (R/W)

Bit 7-4 - Initial volume of envelope

Bit 3 - Envelope UP/DOWN

0: Attenuate

1: Amplify

Bit 2-0 - Number of envelope sweep (n: 0-7)

(If zero, stop envelope operation.)

FF18

Name - NR 23

Contents - Sound Mode 2 register, frequency lo data (W)

Frequency's lower 8 bits of 11 bit data (x).

Next 3 bits are in NR 14 (\$FF19).

FF19

Name - NR 24

Contents - Sound Mode 2 register, frequency hi data (R/W)

Only bit 6 can be read.

Bit 7 - Initial (when set, sound restarts)

Bit 6 - Counter/consecutive selection

Bit 2-0 - Frequency's higher 3 bits (x)

FF1A

Name - NR 30

Contents - Sound Mode 3 register, Sound on/off (R/W)

Only bit 7 can be read

Bit 7 - Sound OFF

0: Sound 3 output stop

1: Sound 3 output OK

FF1B

Name - NR 31

Contents - Sound Mode 3 register, sound length (R/W)

Bit 7-0 - Sound length (t1: 0 - 255)

FF1C

Name - NR 32

Contents - Sound Mode 3 register, Select output level (R/W)

Only bits 6-5 can be read

Bit 6-5 - Select output level

00: Mute

01: Produce Wave Pattern RAM Data as it is (4 bit length)

10: Produce Wave Pattern RAM data shifted once to the RIGHT (1/2)
(4 bit length)

11: Produce Wave Pattern RAM data shifted twice to the RIGHT (1/4)
(4 bit length)

FF1D

Name - NR 33

Contents - Sound Mode 3 register, frequency's lower data (W)

Lower 8 bits of an 11 bit frequency (x).

FF1E

Name - NR 34

Contents - Sound Mode 3 register, frequency's higher data (R/W)

Only bit 6 can be read.

Bit 7 - Initial (when set, sound restarts)

Bit 6 - Counter/consecutive flag

Bit 2-0 - Frequency's higher 3 bits (x).

FF20

Name - NR 41

	Contents	- Sound Mode 4 register, sound length (R/W) Bit 5-0 - Sound length data (t1: 0-63)
FF21	Name	- NR 42
	Contents	- Sound Mode 4 register, envelope (R/W) Bit 7-4 - Initial volume of envelope Bit 3 - Envelope UP/DOWN 0: Attenuate 1: Amplify Bit 2-0 - Number of envelope sweep (n: 0-7) (If zero, stop envelope operation.)
FF22	Name	- NR 43
	Contents	- Sound Mode 4 register, polynomial counter (R/W) Bit 7-4 - Selection of the shift clock frequency of the polynomial counter Bit 3 - Selection of the polynomial counter's step Bit 2-0 - Selection of the dividing ratio of frequencies
FF23	Name	- NR 44
	Contents	- Sound Mode 4 register, counter/consecutive; initial (R/W) Only bit 6 can be read. Bit 7 - Initial (when set, sound restarts) Bit 6 - Counter/consecutive selection
FF24	Name	- NR 50
	Contents	- Channel control / ON-OFF / Volume (R/W) Bit 7 - Vin->SO2 ON/OFF

Bit 6-4 - SO2 output level (volume) (# 0-7)

Bit 3 - Vin->SO1 ON/OFF

Bit 2-0 - SO1 output level (volume) (# 0-7)

FF25

Name - NR 51

Contents - Selection of Sound output terminal (R/W)

Bit 7 - Output sound 4 to SO2 terminal

Bit 6 - Output sound 3 to SO2 terminal

Bit 5 - Output sound 2 to SO2 terminal

Bit 4 - Output sound 1 to SO2 terminal

Bit 3 - Output sound 4 to SO1 terminal

Bit 2 - Output sound 3 to SO1 terminal

Bit 1 - Output sound 2 to SO1 terminal

Bit 0 - Output sound 1 to SO1 terminal

FF26

Name - NR 52 (Value at reset: \$F1-GB, \$F0-SGB)

Contents - Sound on/off (R/W)

Bit 7 - All sound on/off

0: stop all sound circuits

1: operate all sound circuits

Bit 3 - Sound 4 ON flag

Bit 2 - Sound 3 ON flag

Bit 1 - Sound 2 ON flag

Bit 0 - Sound 1 ON flag

FF30 - FF3F

Name - Wave Pattern RAM

Contents - Waveform storage for arbitrary sound data

FF40

Name - LCDC (value \$91 at reset)

Contents - LCD Control (R/W)

Bit 7 - LCD Control Operation *

0: Stop completely (no picture on screen)

1: operation

Bit 6 - Window Tile Map Display Select

0: \$9800-\$9BFF

1: \$9C00-\$9FFF

Bit 5 - Window Display

0: off

1: on

Bit 4 - BG & Window Tile Data Select

0: \$8800-\$97FF

1: \$8000-\$8FFF <- Same area as OBJ

Bit 3 - BG Tile Map Display Select

0: \$9800-\$9BFF

1: \$9C00-\$9FFF

Bit 2 - OBJ (Sprite) Size

0: 8*8

1: 8*16 (width*height)

Bit 1 - OBJ (Sprite) Display

0: off

1: on

Bit 0 - BG Display

0: off

1: on

Name - STAT

Contents - LCDC Status (R/W)

Bits 6-3 - Interrupt Selection By LCDC Status

Bit 6 - LYC=LY Coincidence (Selectable)

Bit 5 - Mode 10

Bit 4 - Mode 01

Bit 3 - Mode 00

0: Non Selection

1: Selection

Bit 2 - Coincidence Flag

0: LYC not equal to LCDC LY

1: LYC = LCDC LY

Bit 1-0 - Mode Flag

00: During H-Blank

01: During V-Blank

10: During Searching OAM-RAM

11: During Transferring Data to LCD Driver

FF42

Name - SCY

Contents - Scroll Y (R/W)

8 Bit value \$00-\$FF to scroll BG Y screen position.

FF43

Name - SCX

Contents - Scroll X (R/W)

8 Bit value \$00-\$FF to scroll BG X screen position.

FF44

Name - LY

Contents - LCDC Y-Coordinate (R)

FF45

Name - LYC

Contents - LY Compare (R/W)

FF46

Name - DMA

Contents - DMA Transfer and Start Address (W)

FF47

Name - BGP

Contents - BG & Window Palette Data (R/W)

Bit 7-6 - Data for Dot Data 11 (Normally darkest color)

Bit 5-4 - Data for Dot Data 10

Bit 3-2 - Data for Dot Data 01

Bit 1-0 - Data for Dot Data 00 (Normally lightest color)

FF48

Name - OBPO

Contents - Object Palette 0 Data (R/W)

FF49

Name - OBP1

Contents - Object Palette 1 Data (R/W)

FF4A

Name - WY

Contents - Window Y Position (R/W)

FF4B

Name - WX

Contents - Window X Position (R/W)

FFFF

Name - IE

Contents - Interrupt Enable (R/W)

Bit 4: Transition from High to Low of Pin number P10-P13.

Bit 3: Serial I/O transfer complete

Bit 2: Timer Overflow

Bit 1: LCDC (see STAT)

Bit 0: V-Blank

0: disable

1: enable