

Proposal

Hardware Accelerated Image Compression

Xinyi Chang(xc2323), Yuxiang Chen(yc3096)
Song Wang(sw2996), Nan Zhao(nz2250)

1. Overview

The increasing megapixels in smartphone camera motivates the need for high-speed image compression of raw data files. In this project, we will build specialized hardware to accelerate the JPEG image compression process. There are four main steps in JPEG compression: divide an image into 8-pixel by 8-pixel blocks, DCT on image blocks, quantization, and inverse DCT. We will build a dedicated DCT, quantization, and inverse DCT processor on the FPGA board, in hopes of speeding up the compression process when compared to running solely on the ARM CPU core.

2. DCT/inverse DCT

Discrete Cosine transformation is the mostly frequently used algorithm to transform image data into frequency domain. To optimize the computation speed, we will try to implement the DCT using CSD encoding to minimize the amount of multipliers used as mentioned in [1].

3. Quantization

Quantization is an integer division of each DCT coefficient by the corresponding constant, and rounding the result to the nearest whole number. For image compression, different transformed coefficients have different value significance, so different quantization step sizes are used for each coefficient. JPEG has a suggested table specifying the quantization step sizes for each coefficient.

4. Hardware Architecture

For this project, we will use the software running on the Linux processor to preprocess the image data and send it to the FPGA board. Then we will be using the FPGA as an accelerator for DCT, quantization and inverse DCT computation.

For 2-D DCT implementation , we plan to use 2 DCT-I modules and a transpose buffer combined to achieve its function . Once eight row DCTs have completed , the data can be streamed out from the transpose buffer in column order for the column DCT .

5.Reference

[1] M. Jridi, A. Alfalou, "A low-power, high-speed DCT architecture for image compression: Principle and implementation," 18th IEEE/IFIP VLSI System on Chip Conference (VLSI-SoC), 2010, pp. 304-309.

[2] Marcus, Matt, JPEG Image Compression,
["http://www.cs.dartmouth.edu/~mgm/Final%20Report.pdf"](http://www.cs.dartmouth.edu/~mgm/Final%20Report.pdf), 2014