

Project Proposal: FPGgram

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Overview:

We plan to make a photo booth that is able to render the images in the style of well-known artists. Artificial neural networks are used to transfer the style of one image onto another. A user would take a picture of themselves. The system would take in that image as an input and apply a user-specified style to it. The resulting image would then be displayed on the screen.

Design:

- a) Gather image data as input from camera or webcam: The device would have to interface with a camera or webcam in order to get the image data, most likely using a usb camera.
- b) Image processing/art generation: Convolutional neural networks are used to create the desired image. Many layers are needed to perform object recognition, identify the style of the artist, and then apply this style as a texture layer. We hope to speed up this process by implementing the backpropagation algorithm on the hardware of the fpga and by using a custom memory design to use matrix blocking for the convolutions. We also need to do more research on how to implement the deep neural network efficiently using the board's resources.
- c) Display the output of the network: The resulting image would then be displayed on a VGA screen.

Timeline:

Milestone 1:

Hardware Implementation of the backpropagation algorithm on the fpga board

- Finalize deep neural network design to recognize image content and apply style

Milestone 2:

Implementation of the complete convolutional neural network for image recognition and art generation

- Combination of software and optimized hardware for calculations

Milestone 3:

Finishing up the "photo booth" and finalize user interface

- Taking input data from usb camera and displaying results on VGA.

Resources:

A Neural Algorithm of Artistic Style

<http://arxiv.org/abs/1508.06576>

Implementation of Neural Network Back Propagation Training Algorithm on FPGA

<http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.258.7519&rep=rep1&type=pdf>

Efficient implementation of the Backpropagation algorithm in FPGAs and microcontrollers

<http://www.lcc.uma.es/~lfranco/A40-Ortega+Jerez++2015.pdf>