CSEE W3827

Fundamentals of Computer Systems
Homework Assignment 2

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Columbia University

Due Monday, June 13th, 2016 at 5:30 PM

Name: Solutions

Uni:

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

You may use Logisim to draw your circuits. We also suggest you use Logisim to verify them.

1. (20 pts.) A sequential circuit with two D flip-flops S_0 and S_1, two inputs X and Y, and one output Z behaves according to these equations:

$$S_0' = X\overline{Y} + XS_0 \quad S_1' = \overline{X}S_1 + XS_0 \quad Z = \overline{X}S_0$$

   (a) Draw the corresponding circuit. Label each of the signals mentioned above.

   (b) Derive the state table (next state and output as a function of present state and input).

   (c) Draw the corresponding bubble-and-arc diagram.
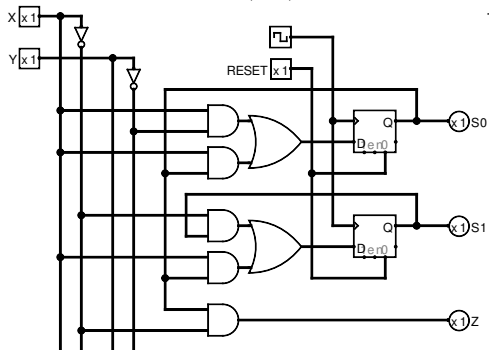
$S_1 S_0$	X	Y	$S_1' S_0'$	Z
00	0	0	00	0
00	0	1	00	0
00	1	0	01	0
00	1	1	00	0
01	0	0	00	1
01	0	1	00	1
01	1	0	11	0
01	1	1	11	0
10	0	0	10	0
10	0	1	10	0
10	1	0	01	0
10	1	1	00	0
11	0	0	10	1
11	0	1	10	1
11	1	0	11	0
11	1	1	11	0
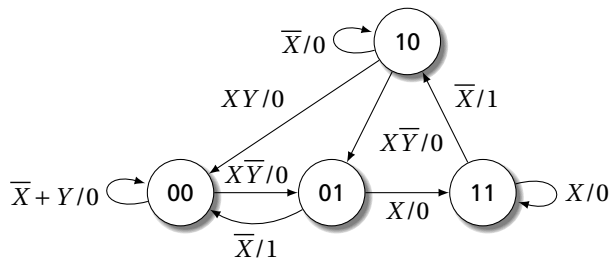
2. (20 pts.) Determine the logic for a synchronous 4-bit decimal counter that counts $0, 1, \ldots, 9, 0, 1, \ldots$ in binary. It should have four outputs Q_1, Q_2, Q_4, Q_8, (the subscripts indicate the value of each bit) each driven directly by a flip-flop.

Write Boolean expressions of the form $D_i = Q_i \oplus (\cdots)$ for each flip-flop's input. ($\oplus$ is XOR). Implement your circuit in Logisim to verify it and include a schematic.
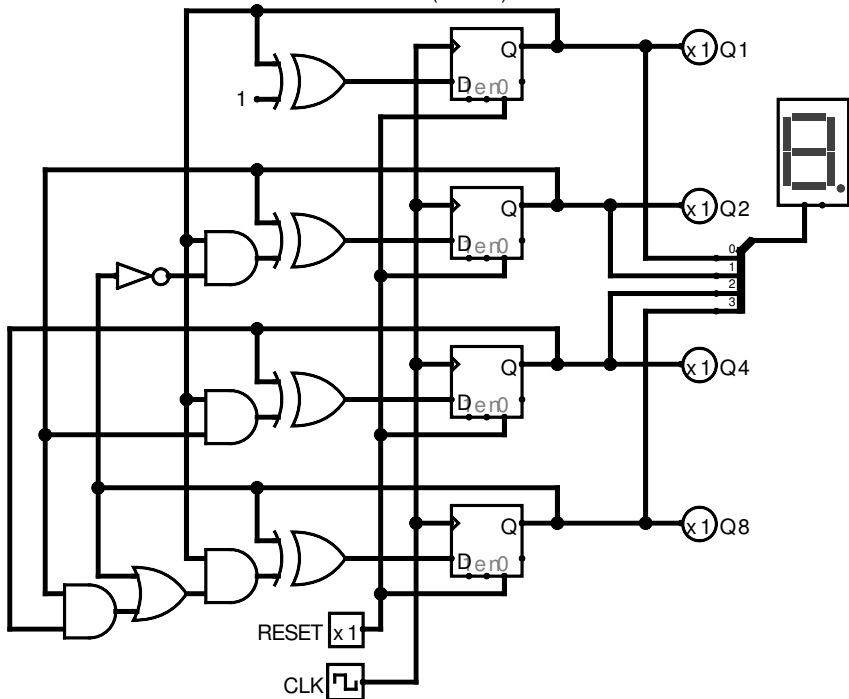
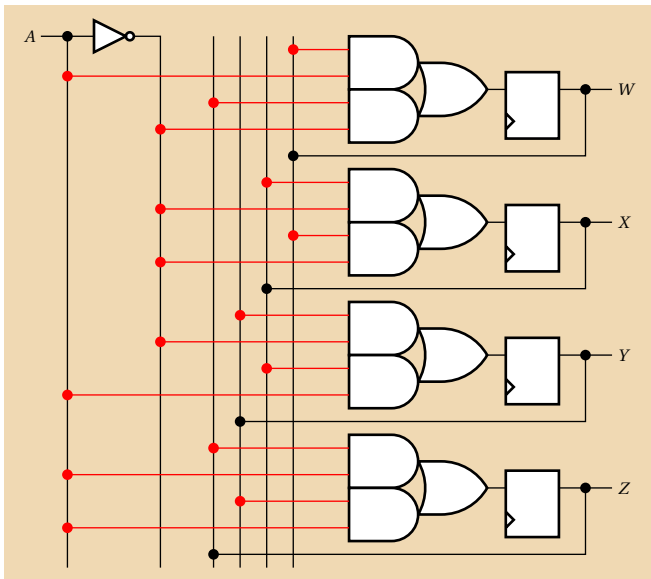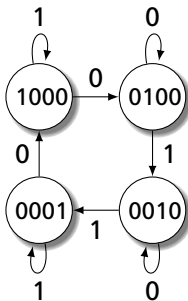$D_8 = Q_8 \oplus$

$D_4 = Q_4 \oplus$

$D_2 = Q_2 \oplus$

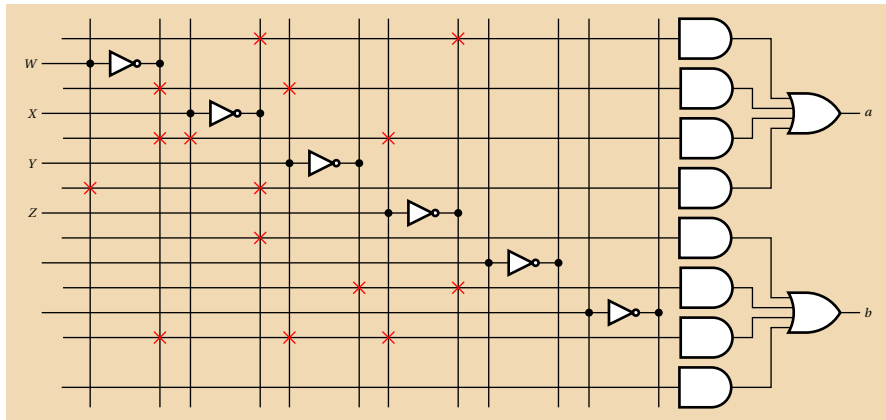$D_1 = Q_1 \oplus$

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
0000
0001

3. (20 pts.) Add wires to the inputs of the AND gates to implement the following Moore state machine. Assume it resets to the "1000" state.

4. (20 pts.) Use the PLA below to implement a decoder for the "a" and "b" segments of a seven-segment display. Indicate connections with an "X."

The segment functions:

$a = \overline{X}\,\overline{Z} + \overline{W}\,Y + \overline{W}\,X\,Z + W\,\overline{X}$

$b = \overline{X} + \overline{Y}\,\overline{Z} + \overline{W}\,Y\,Z$

a

	Z		
1	0	1	1
0	1	1	1
X	X	0	X
1	1	X	X

X { } W, Y

b

	Z		
1	1	1	1
1	0	1	0
X	X	0	X
1	1	X	X

X { } W, Y

5. (20 pts.) The circuit below is called a linear-feedback shift register. Fill in the bubble-and-arc diagram representing its behavior. Start from both the $ABC = 000$ and $ABC = 100$ states.