Ticker Plant System
Implemented in MaxCompiler

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Receives data from the Exchange, calculates all possible implied values, then outputs them in a Machine Readable and sanitized format.
• Simulated market data is parsed CSV received through Ethernet (UDP)
• Kernel computes implied market data from real market data and stores them in respective registers
• Register data is transferred to order book through Ethernet (UDP)
Max Compiler

- Development Environment for writing *optimized* hardware code
- Compiles the .maxj (DFE engine and manager) to VHDL
- The MaxCompiler uses an extension of Java and a proprietary version of the Eclipse IDE
- Compile -> Quartus Compile
  Run -> Hardware Implementation
Software and Hardware Interface

- Communication between the CPU and the FPGA done with a networking approach rather than shared memory.

- UDP Streams sent through Ethernet
Hardware: Platform

- Max4N FPGA platform
- PCIE express bus
- 24GB DDR3 offchip memory
Hardware: FPGA

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Platform</th>
<th>ALMS</th>
<th>Block Memory Bits</th>
<th>DSP Blocks</th>
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<tbody>
<tr>
<td>Altera Cyclone V 5CSXFC6D6F31C8ES</td>
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<td>Max4N Platform</td>
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</tbody>
</table>

- Stratix V FPGA
- Higher count of ALMs
- On-Chip memory (M20k memory blocks)
Hardware: Networking

- 2 QSFP Ports
- 4x10 Gbps Ethernet
- Avalon-ST 64-bit wide client interface
- Operating Frequency: 156.25 MHz with 10-Gbps full-duplex throughput rate (Fmax = 203.6 Mhz)
Conclusion

• MaxCompiler used a simulation engine that executed in a significantly shorter amount of time than a normal Quartus compile.

• Documentation on the Maxeler IDE was sparse and heavily controlled by Maxeler, making it very hard to learn the language.
THANKS $TE(pH)EN and DAVID! =D