10Gb/s Ethernet Platform Implementation

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APPLICATIONS

- DATA Centers
- Finance
- Clusters
Motivation / Significance

- $1.6k – $3.2k
- $300 + Low Power
- $3.6k
- Dev Kit Unavailable
- Dev Kit Unavailable
Architecture of the Design
I. **HSMC** - 4 lanes @ 3.125Gb/s

II. **XAUI/XGMII** - 8 Bytes with 8bits control signals

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**Interfaces**
III. Avalon ST - Unidirectional flow of data @ 156.25MHz.

IV. Avalon MM - A standard address-based read/write interface typical of master-slave connections.
Pin Assignment Matching

Stratix IV Top Level -> Stratix IV Schematic -> HSMC PORT NUMBER -> SoCKit Schematic -> SoCKit Top Level
assign CONFIG0_1 = 1'b1;
assign CONFIG1_1 = 1'b0;
assign CONFIG0_2 = 1'b1;
assign CONFIG1_2 = 1'b0;
assign SS338_CLKIN = 1'b0;
assign SER_BOOT = 1'b0;
assign SMBSPDSEL1 = 1'b0;
assign SMBSPDSEL2 = 1'b0;
assign SMBWEN = 1'b1;
assign GPIO0_1 = 1'b0;
assign GPIO1_1 = 1'b0;
assign GPIO0_2 = 1'b0;
assign GPIO1_2 = 1'b0;
assign NVMA1SEL = 1'b1;
assign NVMPROT = 1'b0;
assign MDOI1 = !MDOEN1? MDO1 : 1'bz;
assign MDIN1 = MDOI1;
assign MDC2 = 1'bz;
assign MDIO2 = 1'bz;
assign PHYRESET = KEY[1];
assign STOPMON = ~KEY[2];

{PRTAD4,PRTAD3,PRTAD2,PRTAD1,PRTAD0} = 5'b00000;
assign PRTAD2 = 1'b0;
assign TXONOFF1 = 1'b1;
assign TXONOFF2 = 1'b1;
assign OPOUTLVL = 1'b0;
assign OPINLVL = 1'b1;
assign USER_LED_R = 8'b00001111;
assign USER_LED_G = 8'b11110000;

--- Diagram ---
### MAC

- Convert between XGMII and Avalon ST Interfaces
- Calculate Checksum
- Check or Append Checksum

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### Fast/Transparent MAC
- 3 clock cycle latency rx
- 2 clock cycle latency tx
MAC
For parallel computing refer to [www.cypress.com/?docID=31573](http://www.cypress.com/?docID=31573) and easics.com

**CRC-32**
Connections
Problem: Data is received and transmitted with a bus width of 64 bits of data, MM interface supports only 32 bits with no control signals.

Solution for Control:
- 7a7a7a7a = SOP
- 7b7b7b7b = EOP
- 7d7d7d7d = escape
- 7e7e7e7e = no data

Dual Clock FIFO
Challenges / Roadblocks

No/Incorrect documentation
New Board / incompatible IP cores
Burnt Daughter board
Dual Port cant be compiled
CRC computation
Timing constraints
MM and HPS
Unreliable Cables