Hardware Acceleration of Market Order Decoding
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What is Hardware Acceleration of Market Order Decoding (HAMOD)
Motivation
System Overview
Hardware
  ◦ Read/Write, Multiplexer
  ◦ Controller
Software
Results
Acknowledgement
What is a HAMOD

- Accelerate the reading of Market Order Data using FPGA.
- Decrease the latency involved in reading data from Ethernet.
- Market data order similar to NASDAQ standard.
- UDP packets.
- Software processes orders and makes sample deals.
Motivation

- Low latency network systems
  - Application in finance
  - Data Centers
- Reconfigurable hardware systems
- Application in current industry.
System
Hardware

- IO_Read with timing Diagram
- IO_Write with timing Diagram
## SignalTap Analyzer

<table>
<thead>
<tr>
<th>Signal</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENET_CLK</td>
<td>0</td>
</tr>
<tr>
<td>ENET_CMD</td>
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</tr>
<tr>
<td>ENET_CS_N</td>
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<tr>
<td>+ENET_DATA</td>
<td>0GF7h</td>
</tr>
<tr>
<td></td>
<td>0C07h</td>
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<td></td>
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</tr>
<tr>
<td></td>
<td>00F7h</td>
</tr>
<tr>
<td>ENET_INT</td>
<td>1</td>
</tr>
<tr>
<td>ENET_RD_N</td>
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<tr>
<td>ENET_RST_N</td>
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<tr>
<td>ENET_WR_N</td>
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<td>+tom_controller[1]</td>
<td>1</td>
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<td>X</td>
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<tr>
<td>+controller[DOUT]</td>
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<td>&quot;&quot;</td>
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<td>+tom_controller[EN0]</td>
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<tr>
<td>+tom_controller[EN1]</td>
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<tr>
<td>+rte_data_reg[DONE]</td>
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Hardware (conti)

- Controller
**Software**

1. **S0**: Initialize DM9000 PHY
2. **S1**: Sends a test packet
3. **S2**: Set custom HW in receive mode
4. **S3**: Waits for INT
5. **S4**: Read flag
6. **S5**: Store order in 2 linked list
7. **S6**: Display packet length
8. **S7**: Make decision on deal
9. **S8**: Send ACK

Flow:
- S0 → S1 → S2 → S3
- S4 → S5 → S6
- S7 → S8

States:
- Int
- Market data
- Non market data
- Deal made
Result/Performance Benchmark

- Successfully receive Market Order Packet and Extract the fields.
- Clock Cycles for HW read and decode = 982
- Clock Cycles for HW + SW read and decode: 14562
- Clock Frequency 50MHz
- We are off-course better than lab2.
Hurdles

- On-chip debugging
- Interrupt management
- Software Memory Constraints
- Poor documentation of DM9000a PHY
Special Thanks

- Professor Stephen Edwards
- David Lariviere (TA)
Questions