Fundamentals of Computer Systems
Transistors, Gates, and ICs

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Semiconductor

sem·i·con·duc·tor
noun
1. a substance, such as silicon or germanium, with electrical conductivity intermediate between that of an insulator and a conductor
2. a semiconductor device
Sand into Silicon

Silica a.k.a. SiO$_2$ a.k.a. Quartz

$\text{SiO}_2 + 2 \text{ C} \rightarrow \text{Si} + 2 \text{ CO}$

Elemental, amorphous silicon

Monocrystalline Silicon Ingot
Doping Silicon Makes It a Better Conductor

Undoped (pure) silicon crystal: Not a good conductor

p-type (doped) silicon: boron atom steals a nearby electron

n-type (doped) silicon: extra electron on arsenic atom jump loose
A PN Junction aka A Diode

Depletion region

\[ \text{p (holes)} \quad \text{n (electrons)} \]
A PN Junction aka A Diode

Forward biased: current flows
A PN Junction aka A Diode

Depletion region

Reverse biased: no current flow
An N-Channel MOS Transistor

Gate positive: On

SiO₂

Drain

Source

n

p (holes)

Ammeter

3 V

Gate
The CMOS Inverter

An inverter is built from two MOSFETs:
An n-FET connected to ground
A p-FET connected to the power supply
The CMOS Inverter

When the input is near the power supply voltage ("1"),
the p-FET is turned off;
the n-FET is turned on, connecting the output to ground ("0”).
n-FETs are only good at passing 0’s
The CMOS Inverter

When the input is near ground ("0"), the p-FET is turned on, connecting the output to the power supply ("1"); the n-FET is turned off. p-FETs are only good at passing 1’s.
The CMOS NAND Gate

Two-input NAND gate:
- two n-FETs in series;
- two p-FETs in parallel
Both inputs 0:
Both p-FETs turned on
Output pulled high
One input 1, the other 0:
One p-FET turned on
Output pulled high
One n-FET turned on, but does not control output
The CMOS NAND Gate

Both inputs 1:
Both n-FETs turned on
Output pulled low
Both p-FETs turned off
The CMOS NOR Gate

Two-input NOR gate:
- two n-FETs in parallel;
- two p-FETs in series.
Not as fast as the NAND gate because n-FETs are faster than p-FETs
A CMOS AND-OR-INVERT Gate
Static CMOS Gate Structure

Pull-up and Pull-down networks must be complementary; exactly one should be connected for each input combination.

Series connection in one should be parallel in the other.
CMOS Inverter Layout

Cross Section Through N-channel FET

Top View
Full Adder Layouts

fa_ly_mini_jk size: 60
- 40 μm (1.2 μm CMOS)

fa_ly_opt1 size: 63
- 50 μm (1.2 μm CMOS)

fa_ly_itt size: 117
- 31 μm (1.2 μm CMOS)

Fulladd.L size: 37
- 25 μm (0.5 μm CMOS)

4001: 256-byte ROM + 4-bit IO port
4002: 40-byte RAM
4003: 10-bit shift register
4004: 740 kHz 4-bit CPU w/ 45 instructions (2300 transistors)
Intel 4004 Masks
Intel 4004 Die Photograph