Fundamentals of Computer Systems
The MIPS Instruction Set

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00010000100001010000000000000111
000000001010010000100001010010
00010100010000000000000000000111
000000001011000010100001000011
0000010000000000111111111111100
00000000100001010000000100011
00000100000000001111111111111010
000000001000010100000000100011
00000100000000001111111111111010
000000000000010000000100000001
00000011111000000000000000000100

beq  $4, $5, 28
slt  $2, $5, $4
bne  $2, $0, 12
subu  $5, $5, $4
bgez  $0 -16
subu  $4, $4, $5
bgez  $0 -24
addu  $2, $0, $4
jr  $31

gcd:
beq  $a0, $a1, .L2
slt  $v0, $a1, $a0
bne  $v0, $zero, .L1
subu  $a1, $a1, $a0
b
gcd
.L1:
subu  $a0, $a0, $a1
b
gcd
.L2:
move  $v0, $a0
j  $ra

int gcd(int a, int b) {
    while (a != b) {
        if (a > b) a = a - b;
        else b = b - a;
    }
    return a;
}
Machine, Assembly, and C Code

```c
int gcd(int a, int b) {
    while (a != b) {
        if (a > b) a = a - b;
        else b = b - a;
    }
    return a;
}
```

beq $4, $5, 28
slt $2, $5, $4
bne $2, $0, 12
subu $5, $5, $4
bgez $0 -16
subu $4, $4, $5
bgez $0 -24
addu $2, $0, $4
jr $31
Machine, Assembly, and C Code

```
gecd:
    beq $a0, $a1, .L2
    slt $v0, $a1, $a0
    bne $v0, $zero, .L1
    subu $a1, $a1, $a0
    b  gcd
.L1:
    subu $a0, $a0, $a1
    b  gcd
.L2:
    move $v0, $a0
    j  $ra
```
Machine, Assembly, and C Code

```assembly
00010000100001010000000000000111  beq   $4, $5, 28
000000010100100000100000101010  slt   $2, $5, $4
00010100010000100000000000000011  bne   $2, $0, 12
000000010100100000100001000111  subu  $5, $5, $4
00000100000000001111111111111100  bgez  $0 -16
00000000100001010010000000100011  subu  $4, $4, $5
00000100000000001111111111111101  bgez  $0 -24
00000000000001000000100000100001  addu  $2, $0, $4
0000001111100000000000100000001000  jr    $31

gcd:
  beq   $a0, $a1, .L2
  slt   $v0, $a1, $a0
  bne   $v0, $zero, .L1
  subu  $a1, $a1, $a0
  b     gcd .L1:
  subu  $a0, $a0, $a1
  b     gcd .L2:
  move  $v0, $a0
  j     $ra
```

```c
int gcd(int a, int b)
{
    while (a != b) {
        if (a > b) a = a - b;
        else b = b - a;
    }
    return a;
}
```
al·go·rithm

a procedure for solving a mathematical problem (as of finding the greatest common divisor) in a finite number of steps that frequently involves repetition of an operation; broadly : a step-by-step procedure for solving a problem or accomplishing some end especially by a computer

Merriam-Webster
The Stored-Program Computer


“Since the device is primarily a computer, it will have to perform the elementary operations of arithmetics most frequently. [...] It is therefore reasonable that it should contain *specialized organs for just these operations*.

“If the device is to be [...] as nearly as possible all purpose, then a distinction must be made between the specific instructions given for and defining a particular problem, and the general control organs which see to it that these instructions [...] are carried out. The former must be *stored in some way* [...] the latter are represented by definite operating parts of the device.

“Any device which is to carry out long and complicated sequences of operations (specifically of calculations) *must have a considerable memory*.
Instruction Set Architecture (ISA)

ISA: The interface or contact between the hardware and the software

Rules about how to code and interpret machine instructions:

- Execution model (program counter)
- Operations (instructions)
- Data formats (sizes, addressing modes)
- Processor state (registers)
- Input and Output (memory, etc.)
Architecture vs. Microarchitecture

Architecture: The interface the hardware presents to the software

Microarchitecture: The detailed implementation of the architecture
MIPS

Microprocessor without Interlocked Pipeline Stages

RISC vs. CISC Architectures

MIPS is a Reduced Instruction Set Computer. Others include ARM, PowerPC, SPARC, HP-PA, and Alpha.

A Complex Instruction Set Computer (CISC) is one alternative. Intel’s x86 is the most prominent example; also Motorola 68000 and DEC VAX.

RISC’s underlying principles, due to Hennessy and Patterson:

- Simplicity favors regularity
- Make the common case fast
- Smaller is faster
- Good design demands good compromises
The GCD Algorithm

Euclid, *Elements*, 300 BC.

The greatest common divisor of two numbers does not change if the smaller is subtracted from the larger.

1. Call the two numbers $a$ and $b$
2. If $a$ and $b$ are equal, stop: $a$ is the greatest common divisor
3. Subtract the smaller from the larger
4. Repeat steps 2–4
Let’s be a little more explicit:

1. Call the two numbers \( a \) and \( b \)
2. If \( a \) equals \( b \), go to step 8
3. if \( a \) is less than \( b \), go to step 6
4. Subtract \( b \) from \( a \)  \( a > b \) here
5. Go to step 2
6. Subtract \( a \) from \( b \)  \( a < b \) here
7. Go to step 2
8. Declare \( a \) the greatest common divisor
9. Go back to doing whatever you were doing before
Euclid’s Algorithm in MIPS Assembly

gcd:

```
beq $a0, $a1, .L2  # if a = b, go to exit
sgt $v0, $a1, $a0  # Is b > a?
bne $v0, $zero, .L1  # Yes, goto .L1

subu $a0, $a0, $a1  # Subtract b from a (b < a)
gcd  # and repeat
```

```
.L1:
subu $a1, $a1, $a0  # Subtract a from b (a < b)
gcd  # and repeat
```

```
.L2:
move $v0, $a0  # return a
j $ra  # Return to caller
```

Instructions
Euclid’s Algorithm in MIPS Assembly

```assembly
gcd:
   beq $a0, $a1, .L2       # if a = b, go to exit
   sgt $v0, $a1, $a0       # Is b > a?
   bne $v0, $zero, .L1     # Yes, goto .L1
   subu $a0, $a0, $a1      # Subtract b from a (b < a)
   b gcd                    # and repeat

.L1:
   subu $a1, $a1, $a0      # Subtract a from b (a < b)
   b gcd                    # and repeat

.L2:
   move $v0, $a0           # return a
   j $ra                   # Return to caller
```

Operands: Registers, etc.
Euclid’s Algorithm in MIPS Assembly

```mips
gcd:  
    beq $a0, $a1, .L2  # if a = b, go to exit
    sgt $v0, $a1, $a0  # Is b > a?
    bne $v0, $zero, .L1 # Yes, goto .L1

    subu $a0, $a0, $a1  # Subtract b from a (b < a)
    b gcd  # and repeat

.L1:
    subu $a1, $a1, $a0  # Subtract a from b (a < b)
    b gcd  # and repeat

.L2:
    move $v0, $a0  # return a
    j $ra  # Return to caller
```

Labels
Euclid’s Algorithm in MIPS Assembly

```mips
gcd:
    beq $a0, $a1, .L2     # if a = b, go to exit
    sgt $v0, $a1, $a0     # Is b > a?
    bne $v0, $zero, .L1   # Yes, goto .L1
    subu $a0, $a0, $a1    # Subtract b from a (b < a)
    # and repeat
    b gcd

.L1:
    subu $a1, $a1, $a0    # Subtract a from b (a < b)
    # and repeat
    b gcd

.L2:
    move $v0, $a0         # return a
    j $ra                 # Return to caller
```

Comments
Euclid’s Algorithm in MIPS Assembly

```asm
gcd:
   beq $a0, $a1, .L2  # if a = b, go to exit
   sgt $v0, $a1, $a0  # Is b > a?
   bne $v0, $zero, .L1 # Yes, goto .L1

   subu $a0, $a0, $a1  # Subtract b from a (b < a)
   b  gcd  # and repeat

.L1:
   subu $a1, $a1, $a0  # Subtract a from b (a < b)
   b  gcd  # and repeat

.L2:
   move $v0, $a0  # return a
   j  $ra  # Return to caller
```

Arithmetic Instructions
Euclid’s Algorithm in MIPS Assembly

gcd:
    beq $a0, $a1, .L2     # if a = b, go to exit
    sgt $v0, $a1, $a0    # Is b > a?
    bne $v0, $zero, .L1  # Yes, goto .L1

    subu $a0, $a0, $a1    # Subtract b from a (b < a)
    b gcd
    # and repeat

.L1:
    subu $a1, $a1, $a0    # Subtract a from b (a < b)
    b gcd
    # and repeat

.L2:
    move $v0, $a0         # return a
    j $ra                 # Return to caller

Control-transfer instructions
### General-Purpose Registers

<table>
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<tr>
<th>Name</th>
<th>Number</th>
<th>Usage</th>
<th>Preserved?</th>
</tr>
</thead>
<tbody>
<tr>
<td>$zero</td>
<td>0</td>
<td>Constant zero</td>
<td></td>
</tr>
<tr>
<td>$at</td>
<td>1</td>
<td>Reserved (assembler)</td>
<td></td>
</tr>
<tr>
<td>$v0–$v1</td>
<td>2–3</td>
<td>Function result</td>
<td></td>
</tr>
<tr>
<td>$a0–$a3</td>
<td>4–7</td>
<td>Function arguments</td>
<td></td>
</tr>
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<td>$t0–$t7</td>
<td>8–15</td>
<td>Temporaries</td>
<td></td>
</tr>
<tr>
<td>$s0–$s7</td>
<td>16–23</td>
<td>Saved</td>
<td>yes</td>
</tr>
<tr>
<td>$t8–$t9</td>
<td>24–25</td>
<td>Temporaries</td>
<td></td>
</tr>
<tr>
<td>$k0–$k1</td>
<td>26-27</td>
<td>Reserved (OS)</td>
<td></td>
</tr>
<tr>
<td>$gp</td>
<td>28</td>
<td>Global pointer</td>
<td>yes</td>
</tr>
<tr>
<td>$sp</td>
<td>29</td>
<td>Stack pointer</td>
<td>yes</td>
</tr>
<tr>
<td>$fp</td>
<td>30</td>
<td>Frame pointer</td>
<td>yes</td>
</tr>
<tr>
<td>$ra</td>
<td>31</td>
<td>Return address</td>
<td>yes</td>
</tr>
</tbody>
</table>

Each 32 bits wide
Only 0 truly behaves differently; usage is convention
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<th>Examples</th>
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<td>Writing and reading data to/from memory</td>
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<tr>
<td>Jump and branch</td>
<td>Control transfer, often conditional</td>
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<tr>
<td>Miscellaneous</td>
<td>Everything else</td>
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</tbody>
</table>
## Computational Instructions

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</thead>
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<tr>
<td><strong>Arithmetic</strong></td>
<td></td>
</tr>
<tr>
<td><code>add</code> Add</td>
<td><code>sll</code> Shift left logical</td>
</tr>
<tr>
<td><code>addu</code> Add unsigned</td>
<td><code>srl</code> Shift right logical</td>
</tr>
<tr>
<td><code>sub</code> Subtract</td>
<td><code>sra</code> Shift right arithmetic</td>
</tr>
<tr>
<td><code>subu</code> Subtract unsigned</td>
<td><code>sllv</code>  Shift left logical variable</td>
</tr>
<tr>
<td><code>slt</code> Set on less than</td>
<td><code>srlv</code> Shift right logical variable</td>
</tr>
<tr>
<td><code>sltu</code> Set on less than unsigned</td>
<td><code>srav</code> Shift right arith. variable</td>
</tr>
<tr>
<td><code>and</code> AND</td>
<td></td>
</tr>
<tr>
<td><code>or</code> OR</td>
<td></td>
</tr>
<tr>
<td><code>xor</code> Exclusive OR</td>
<td></td>
</tr>
<tr>
<td><code>nor</code> NOR</td>
<td></td>
</tr>
<tr>
<td><strong>Arithmetic (immediate)</strong></td>
<td></td>
</tr>
<tr>
<td><code>addi</code> Add immediate</td>
<td><code>mult</code> Multiply</td>
</tr>
<tr>
<td><code>addiu</code> Add immediate unsigned</td>
<td><code>multu</code> Multiply unsigned</td>
</tr>
<tr>
<td><code>slti</code> Set on l. t. immediate</td>
<td><code>div</code> Divide</td>
</tr>
<tr>
<td><code>sltiu</code> Set on less than unsigned</td>
<td><code>divu</code> Divide unsigned</td>
</tr>
<tr>
<td><code>andi</code> AND immediate</td>
<td><code>mfhi</code> Move from HI</td>
</tr>
<tr>
<td><code>ori</code> OR immediate</td>
<td><code>mthi</code> Move to HI</td>
</tr>
<tr>
<td><code>xori</code> Exclusive OR immediate</td>
<td><code>mflo</code> Move from LO</td>
</tr>
<tr>
<td><code>lui</code> Load upper immediate</td>
<td><code>mtlo</code> Move to LO</td>
</tr>
</tbody>
</table>
Computational Instructions

Arithmetic, logical, and other computations. Example:

```
add $t0, $t1, $t3
```

“Add the contents of registers $t1 and $t3; store the result in $t0”

Register form:

```
operation R_D, R_S, R_T
```

“Perform operation on the contents of registers $R_S$ and $R_T$; store the result in $R_D$”

Passes control to the next instruction in memory after running.
Arithmetic Instruction Example

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>c</th>
<th>f</th>
<th>g</th>
<th>h</th>
<th>i</th>
<th>j</th>
</tr>
</thead>
<tbody>
<tr>
<td>$s0</td>
<td>$s1</td>
<td>$s2</td>
<td>$s3</td>
<td>$s4</td>
<td>$s5</td>
<td>$s6</td>
<td>$s7</td>
</tr>
</tbody>
</table>

a = b - c;

f = (g + h) - (i + j);

\text{subu} \ $s0, \ $s1, \ $s2
\text{addu} \ $t0, \ $s4, \ $s5
\text{addu} \ $t1, \ $s6, \ $s7
\text{subu} \ $s3, \ $t0, \ $t1

“Signed” addition/subtraction (\text{add/sub}) throw an exception on a two’s-complement overflow; “Unsigned” variants (\text{addu/subu}) do not. Resulting bit patterns otherwise identical.
Bitwise Logical Operator Example

li $t0, 0xFFFF0000  # "Load immediate"
li $t1, 0xF0F0F0F0  # "Load immediate"

nor $t2, $t0, $t1   # Puts 0x000F000F in $t2

li $v0, 1           # print_int
move $a0, $t2       # print contents of $t2
syscall
Immediate Computational Instructions

Example:

```
addiu $t0, $t1, 42
```

"Add the contents of register $t1 and 42; store the result in register $t0"

In general,

```
operation R_D, R_S, I
```

"Perform operation on the contents of register R_S and the signed 16-bit immediate I; store the result in R_D"

Thus, I can range from −32768 to 32767.
32-Bit Constants and lui

It is easy to load a register with a constant from −32768 to 32767, e.g.,

\[
\text{ori} \; \$t0, \; 0, \; 42
\]

Larger numbers use “load upper immediate,” which fills a register with a 16-bit immediate value followed by 16 zeros; an OR handily fills in the rest. E.g., Load \$t0 with 0xC0DEFACE:

\[
\text{lui} \; \$t0, \; 0x\text{CODE} \\
\text{ori} \; \$t0, \; \$t0, \; 0xFACE
\]

The assembler automatically expands the \text{li} pseudo-instruction into such an instruction sequence

\[
\text{li} \; \$t1, \; 0x\text{CAFE0BOE} \rightarrow \text{lui} \; \$t1, \; 0x\text{CAFE} \\
\text{ori} \; \$t1, \; \$t1, \; 0x0BOE
\]
Multiplication and Division

Multiplication gives 64-bit result in two 32-bit registers: HI and LO. Division: LO has quotient; HI has remainder.

```c
int multdiv(
    int a,    // $a0
    int b,    // $a1
    unsigned c, // $a2
    unsigned d) // $a3
{
    a = a * b + c;
    c = c * d + a;

    a = a / c;
    b = b % a;
    c = c / d;
    d = d % c;

    return a + b + c + d;
}
```

```assembly
multdiv:
    mult $a0,$a1      # a * b
    mflo $t0
    addu $a0,$t0,$a2 # a = a*b + c
    mult $a2,$a3     # c * d
    mflo $t1
    addu $a2,$t1,$a0 # c = c*d + a
    divu $a0,$a2     # a / c
    mflo $a0         # a = a/c
    div $0,$a1,$a0   # b % a
    mfhi $a1         # b = b%a
    divu $a2,$a3     # c / d
    mflo $a2         # c = c/d
    addu $t2,$a0,$a1 # a + b
    addu $t2,$t2,$a2 # (a+b) + c
    divu $a3,$a2     # d % c
    mfhi $a3         # d = d%c
    addu $v0,$t2,$a3 # ((a+b)+c) + d
    j $ra
```
Shift Left

Shifting left amounts to multiplying by a power of two. Zeros are added to the least significant bits. The constant form explicitly specifies the number of bits to shift:

\[
\text{sll} \ $a0, $a0, 1
\]

The variable form takes the number of bits to shift from a register (mod 32):

\[
\text{sllv} \ $a1, $a0, $t0
\]
Shift Right Logical

The logical form of right shift adds 0’s to the MSB.

\[ \text{sr}l \ \$a0, \ \$a0, \ 1 \]

```
31  30  ...  2  1  0
```

```
The “arithmetic” form of right shift sign-extends the word by copying the MSB.

```
sra $a0, $a0, 2
```
### Set on Less Than

```
set_on_less_than
```

```
slt $t0, $t1, $t2
```

Set $t0 to 1 if the contents of $t1 < $t2; 0 otherwise.
$t1$ and $t2$ are treated as 32-bit signed two’s complement numbers.

```c
int compare(int a, // $a0
             int b, // $a1
             unsigned c, // $a2
             unsigned d) // $a3
{
    int r = 0; // $v0
    if (a < b) r += 42;
    if (c < d) r += 99;
    return r;
}
```

```assembly
compare:
    move $v0, $zero
    slt $t0, $a0, $a1
    beq $t0, $zero, .L1
    addi $v0, $v0, 42
.L1:
    sltu $t0, $a2, $a3
    beq $t0, $zero, .L2
    addi $v0, $v0, 99
.L2:
    j $ra
```
## Load and Store Instructions

<table>
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<th>Instruction</th>
<th>Description</th>
<th>MIPS Architecture</th>
<th>x86 Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>lb</td>
<td>Load byte</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lbu</td>
<td>Load byte unsigned</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lh</td>
<td>Load halfword</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lhu</td>
<td>Load halfword unsigned</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lw</td>
<td>Load word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lwl</td>
<td>Load word left</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lwr</td>
<td>Load word right</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sb</td>
<td>Store byte</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sh</td>
<td>Store halfword</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sw</td>
<td>Store word</td>
<td></td>
<td></td>
</tr>
<tr>
<td>swl</td>
<td>Store word left</td>
<td></td>
<td></td>
</tr>
<tr>
<td>swr</td>
<td>Store word right</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The MIPS is a load/store architecture: data must be moved into registers for computation.

Other architectures e.g., (x86) allow arithmetic directly on data in memory.
Memory on the MIPS

Memory is byte-addressed. Each byte consists of eight bits:

7 6 5 4 3 2 1 0

Bytes have non-negative integer addresses. Byte addresses on the 32-bit MIPS processor are 32 bits; 64-bit processors usually have 64-bit addresses.

0: 7 6 5 4 3 2 1 0
1: 7 6 5 4 3 2 1 0
2: 7 6 5 4 3 2 1 0

\[2^{32} - 1: \quad 7 6 5 4 3 2 1 0\]

4 Gb total
Base Addressing in MIPS

There is only one way to refer to what address to load/store in MIPS: base + offset.

\[
\text{lb } \$t0, 34(\$t1)
\]

\[
\begin{align*}
\text{42: } & \quad \text{EF} \\
\text{\$t0: } & \quad \text{FFFFFFFEF}
\end{align*}
\]

\[-32768 < \text{offset} < 32767\]
MIPS registers are 32 bits (4 bytes). Loading a byte into a register either clears the top three bytes or sign-extends them.

\[
\begin{align*}
42: & \quad \text{F0} \\
\text{lbu} & \quad \text{t0}, 42(0) \\
\text{t0:} & \quad 000000F0
\end{align*}
\]

\[
\begin{align*}
42: & \quad \text{F0} \\
\text{lb} & \quad \text{t0}, 42(0) \\
\text{t0:} & \quad FFFFFFFF0
\end{align*}
\]
The Endian Question

MIPS can also load and store 4-byte words and 2-byte halfwords.

The *endian* question: when you read a word, in what order do the bytes appear?

Little Endian: Intel, DEC, et al.

Big Endian: Motorola, IBM, Sun, et al.

MIPS can do either

SPIM adopts its host’s convention
Testing Endianness

.data # Directive: ‘‘this is data’’
myword:
  .word 0 # Define a word of data (=0)

.text # Directive: ‘‘this is program’’
main:
  la $t1, myword # pseudoinstruction: load address
  li $t0, 0x11
  sb $t0, 0($t1) # Store 0x11 at byte 0
  li $t0, 0x22
  sb $t0, 1($t1) # Store 0x22 at byte 1
  li $t0, 0x33
  sb $t0, 2($t1) # Store 0x33 at byte 2
  li $t0, 0x44
  sb $t0, 3($t1) # Store 0x44 at byte 3
  lw $t2, 0($t1) # 0x11223344 or 0x44332211?
  j $ra
Alignment

Word and half-word loads and stores must be aligned: words must start at a multiple of 4 bytes; halfwords on a multiple of 2.

Byte load/store has no such constraint.

```
lw $t0,  4($0)  # OK
lw $t0,  5($0)  # BAD: 5 mod 4 = 1
lw $t0,  8($0)  # OK
lw $t0, 12($0)  # OK
lh $t0,  2($0)  # OK
lh $t0,  3($0)  # BAD: 3 mod 2 = 1
lh $t0,  4($0)  # OK
```
### Jump and Branch Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>j</code></td>
<td>Jump</td>
</tr>
<tr>
<td><code>jal</code></td>
<td>Jump and link</td>
</tr>
<tr>
<td><code>jr</code></td>
<td>Jump to register</td>
</tr>
<tr>
<td><code>jalr</code></td>
<td>Jump and link register</td>
</tr>
<tr>
<td><code>beq</code></td>
<td>Branch on equal</td>
</tr>
<tr>
<td><code>bne</code></td>
<td>Branch on not equal</td>
</tr>
<tr>
<td><code>blez</code></td>
<td>Branch on less than or equal to zero</td>
</tr>
<tr>
<td><code>bgtz</code></td>
<td>Branch on greater than zero</td>
</tr>
<tr>
<td><code>bltz</code></td>
<td>Branch on less than zero</td>
</tr>
<tr>
<td><code>bgez</code></td>
<td>Branch on greater than or equal to zero</td>
</tr>
<tr>
<td><code>bltzal</code></td>
<td>Branch on less than zero and link</td>
</tr>
<tr>
<td><code>bgezal</code></td>
<td>Branch on greater than or equal to zero and link</td>
</tr>
</tbody>
</table>
Jumps

The simplest form,

    j  mylabel
    # ...

mylabel:
    # ...

sends control to the instruction at `mylabel`. Instruction holds a 26-bit constant multiplied by four; top four bits come from current PC. Uncommon.

Jump to register sends control to a 32-bit absolute address in a register:

    jr  $t3

Instructions must be four-byte aligned; the contents of the register must be a multiple of 4.
Jump and Link

Jump and link stores a return address in $ra for implementing subroutines:

```assembly
jal mysub
# Control resumes here after the jr
# ...
```

`mysub:
# ...

jr $ra  # Jump back to caller
```

`jalr` is similar; target address supplied in a register.
Branches

Used for conditionals or loops. E.g., “send control to myloop if the contents of $t0 is not equal to the contents of $t1.”

myloop:
  # ...

  bne $t0, $t1, myloop
  # ...

beq is similar “branch if equal”

A “jump” supplies an absolute address; a “branch” supplies an offset to the program counter.

On the MIPS, a 16-bit signed offset is multiplied by four and added to the address of the next instruction.
Branches

Another family of branches tests a single register:

```
bgez $t0, myelse  # Branch if $t0 positive
    # ...
```

```
myelse:
    # ...
```

Others in this family:

- `blez` Branch on less than or equal to zero
- `bgtz` Branch on greater than zero
- `bltz` Branch on less than zero
- `bltzal` Branch on less than zero and link
- `bgez` Branch on greater than or equal to zero
- `bgezal` Branch on greater than or equal to zero and link

“and link” variants also (always) put the address of the next instruction into $ra, just like `jal`.
Other Instructions

syscall causes a system call exception, which the OS catches, interprets, and usually returns from.

SPIM provides simple services: printing and reading integers, strings, and floating-point numbers, sbrk() (memory request), and exit().

```
# prints "the answer = 5"
.data
str:
 .asciiz "the answer = "
.text
li $v0, 4  # system call code for print_str
la $a0, str # address of string to print
syscall  # print the string

li $v0, 1  # system call code for print_int
li $a0, 5  # integer to print
syscall  # print it
```
### Other Instructions

#### Exception Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>tge tlt</td>
<td>Conditional traps</td>
</tr>
<tr>
<td>break</td>
<td>Breakpoint trap, for debugging</td>
</tr>
<tr>
<td>eret</td>
<td>Return from exception</td>
</tr>
</tbody>
</table>

#### Multiprocessor Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ll sc</td>
<td>Load linked/store conditional for atomic operations</td>
</tr>
<tr>
<td>sync</td>
<td>Read/Write fence: wait for all memory loads/stores</td>
</tr>
</tbody>
</table>

#### Coprocessor 0 Instructions (System Mgmt)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>lwr lw1</td>
<td>Cache control</td>
</tr>
<tr>
<td>tlbr tblwi</td>
<td>TLB control (virtual memory)</td>
</tr>
<tr>
<td>...</td>
<td>Many others (data movement, branches)</td>
</tr>
</tbody>
</table>

#### Floating-point Coprocessor Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>add.d sub.d</td>
<td>Arithmetic and other functions</td>
</tr>
<tr>
<td>lwcl swcl</td>
<td>Load/store to (32) floating-point registers</td>
</tr>
<tr>
<td>bctlt</td>
<td>Conditional branches</td>
</tr>
</tbody>
</table>
Instruction Encoding

Register-type: **add, sub, xor, ...**

<table>
<thead>
<tr>
<th>op:6</th>
<th>rs:5</th>
<th>rt:5</th>
<th>rd:5</th>
<th>shamt:5</th>
<th>funct:6</th>
</tr>
</thead>
</table>

Immediate-type: **addi, subi, beq, ...**

<table>
<thead>
<tr>
<th>op:6</th>
<th>rs:5</th>
<th>rt:5</th>
<th>imm:16</th>
</tr>
</thead>
</table>

Jump-type: **j, jal ...**

<table>
<thead>
<tr>
<th>op:6</th>
<th>addr:26</th>
</tr>
</thead>
</table>
**Register-type Encoding Example**

<table>
<thead>
<tr>
<th>op:6</th>
<th>rs:5</th>
<th>rt:5</th>
<th>rd:5</th>
<th>shamt:5</th>
<th>funct:6</th>
</tr>
</thead>
</table>

**add** $t0, $s1, $s2

**add** encoding from the MIPS instruction set reference:

<table>
<thead>
<tr>
<th>SPECIAL 000000</th>
<th>rs</th>
<th>rt</th>
<th>rd</th>
<th>000000</th>
<th>ADD 100000</th>
</tr>
</thead>
</table>

Since $t0 is register 8; $s1 is 17; and $s2 is 18,

<table>
<thead>
<tr>
<th>000000</th>
<th>10001</th>
<th>10010</th>
<th>01000</th>
<th>00000</th>
<th>100000</th>
</tr>
</thead>
</table>
Register-type Shift Instructions

\[
\begin{array}{cccccc}
\text{op:6} & \text{rs:5} & \text{rt:5} & \text{rd:5} & \text{shamt:5} & \text{funct:6} \\
\hline
\end{array}
\]

sra $t0, $s1, 5

sra encoding from the MIPS instruction set reference:

\[
\begin{array}{cccccc}
\text{SPECIAL} & 0 & 0 & 0 & 0 & 0 \\
000000 & 000000 & \text{rt} & \text{rd} & \text{sa} & \text{SRA} \\
000011 & 000011 & 000011 & 000011 \\
\end{array}
\]

Since $t0 is register 8 and $s1 is 17,

\[
\begin{array}{cccccc}
000000 & 000000 & 10010 & 01000 & 00101 & 000011 \\
\end{array}
\]
Immediate-type Encoding Example

```
op:6 | rs:5  | rt:5 | imm:16
```

```
addiu $t0, $s1, -42
```

**addiu** encoding from the MIPS instruction set reference:

```
ADDIU 001001 | rs  | rt  | immediate
```

Since $t0 is register 8 and $s1 is 17,

```
001001 10001 01000 1111 1111 1101 0110
```
Jump-Type Encoding Example

<table>
<thead>
<tr>
<th>op:6</th>
<th>addr:26</th>
</tr>
</thead>
</table>

\texttt{jal 0x5014}

\texttt{jal} encoding from the MIPS instruction set reference:

<table>
<thead>
<tr>
<th>JAL</th>
<th>instr_index</th>
</tr>
</thead>
<tbody>
<tr>
<td>000011</td>
<td></td>
</tr>
</tbody>
</table>

Instruction index is a word address

| 000011 | 00 0000 0000 0001 0100 0000 0101 |
### Assembler Pseudoinstructions

<table>
<thead>
<tr>
<th>Branch Type</th>
<th>Pseudoinstruction</th>
<th>Equivalent Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Branch always</td>
<td>\textit{b} \textit{label}</td>
<td>\textit{beq} $0, 0, \textit{label}$</td>
</tr>
<tr>
<td>Branch if equal zero</td>
<td>\textit{beqz} \textit{s, label}</td>
<td>\textit{beq s, 0, label}$</td>
</tr>
</tbody>
</table>
| Branch greater or equal                  | \textit{bge} \textit{s, t, label} | \textit{slt} $1, s, t$
|                                           |                                | \textit{beq} $1, 0, \textit{label}$ |
| Branch greater or equal unsigned         | \textit{bgeu} \textit{s, t, label} | \textit{slt} $1, t, s$
|                                           |                                | \textit{bne} $1, 0, \textit{label}$ |
| Branch greater than                      | \textit{bgt} \textit{s, t, label} | \textit{slt} $1, t, s$
|                                           |                                | \textit{bne} $1, 0, \textit{label}$ |
| Branch greater than unsigned             | \textit{bgtu} \textit{s, t, label} | \textit{slt} $1, t, s$
|                                           |                                | \textit{bne} $1, 0, \textit{label}$ |
| Branch less than                         | \textit{blt} \textit{s, t, label} | \textit{slt} $1, s, t$
|                                           |                                | \textit{bne} $1, 0, \textit{label}$ |
| Branch less than unsigned                | \textit{bltu} \textit{s, t, label} | \textit{slt} $1, s, t$
|                                           |                                | \textit{bne} $1, 0, \textit{label}$ |
### Assembler Pseudoinstructions

<table>
<thead>
<tr>
<th>Operation</th>
<th>ASSEMBLER</th>
<th>REPLACED BY</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Load immediate</strong></td>
<td>\textbf{li} \textit{d,j}</td>
<td>\textbf{ori} \textit{d,$0,j}</td>
</tr>
<tr>
<td>$0 \leq j \leq 65535$</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Load immediate</strong></td>
<td>\textbf{li} \textit{d,j}</td>
<td>\textbf{addiu} \textit{d,$0,j}</td>
</tr>
<tr>
<td>$-32768 \leq j &lt; 0$</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Load immediate</strong></td>
<td>\textbf{li} \textit{d,j}</td>
<td>\textbf{liu} \textit{d,hi16(j)} \textbf{ori} \textit{d,d,lo16(j)}</td>
</tr>
<tr>
<td><strong>Move</strong></td>
<td>\textbf{move} \textit{d,s}</td>
<td>\textbf{or} \textit{d,s,$0}</td>
</tr>
<tr>
<td><strong>Multiply</strong></td>
<td>\textbf{mul} \textit{d,s,t}</td>
<td>\textbf{mult} \textit{s,t} \textbf{mflo} \textit{d}</td>
</tr>
<tr>
<td><strong>Negate unsigned</strong></td>
<td>\textbf{negu} \textit{d,s}</td>
<td>\textbf{subu} \textit{d,$0,s}</td>
</tr>
<tr>
<td><strong>Set if equal</strong></td>
<td>\textbf{seq} \textit{d,s,t}</td>
<td>\textbf{xor} \textit{d,s,t} \textbf{sltiu} \textit{d,d,1}</td>
</tr>
<tr>
<td><strong>Set if greater or equal</strong></td>
<td>\textbf{sge} \textit{d,s,t}</td>
<td>\textbf{slt} \textit{d,s,t} \textbf{xori} \textit{d,d,1}</td>
</tr>
<tr>
<td><strong>Set if greater or equal unsigned</strong></td>
<td>\textbf{sgeu} \textit{d,s,t}</td>
<td>\textbf{sltu} \textit{d,s,t} \textbf{xori} \textit{d,d,1}</td>
</tr>
<tr>
<td><strong>Set if greater than</strong></td>
<td>\textbf{sgt} \textit{d,s,t}</td>
<td>\textbf{slt} \textit{d,t,s}</td>
</tr>
</tbody>
</table>
Expressions

Initial expression:

\[
x + y + z \times (w + 3)
\]

Reordered to minimize intermediate results; fully parenthesized to make order of operation clear.

\[
(((w + 3) \times z) + y) + x
\]

```
addiu $t0, $a0, 3  # w: $a0
mul $t0, $t0, $a3   # x: $a1
addu $t0, $t0, $a2  # y: $a2
addu $t0, $t0, $a1  # z: $a3
```

Consider an alternative:

\[
(x + y) + ((w + 3) \times z)
\]

```
addu $t0, $a1, $a2  
addiu $t1, $a0, 3    # Need a second temporary
mul $t1, $t1, $a3    
addu $t0, $t0, $t1
```
if ((x + y) < 3)
x = x + 5;
else
  y = y + 4;

addu $t0, $a0, $a1 # x + y
slti $t0, $t0, 3  # (x+y)<3
beq  $t0, $0, ELSE
addiu $a0, $a0, 5  # x += 5
b    DONE

ELSE:
  addiu $a1, $a1, 4  # y += 4
DONE:
Do-While Loops

Post-test loop: body always executes once

\[
a = 0; \\
b = 0; \\
do \{ \\
    \quad a = a + b; \\
    \quad b = b + 1; \\
\} \text{ while } (b \neq 10);
\]

```
move $a0, $0 # a = 0
move $a1, $0 # b = 0
li $t0, 10 # load constant

TOP:
addu $a0, $a0, $a1 # a = a + b
addiu $a1, $a1, 1 # b = b + 1
bne $a1, $t0, TOP # b != 10?
```
While Loops

Pre-test loop: body may never execute

```
a = 0;
b = 0;
while (b != 10) {
a = a + b;
b = b + 1;
}
```

```
move $a0, $0  # a = 0
move $a1, $0  # b = 0
li $t0, 10
b TEST       # test first

BODY:
addu $a0, $a0, $a1  # a = a + b
addiu $a1, $a1, 1  # b = b + 1

TEST:
bne $a1, $t0, BODY  # b != 10?
```
For Loops

“Syntactic sugar” for a while loop

```plaintext
for (a = b = 0 ; b != 10 ; b++)
    a += b;
```

is equivalent to

```plaintext
a = b = 0;
while (b != 10) {
    a = a + b;
    b = b + 1;
}
```

```plaintext
move $a1, $0  # b = 0
move $a0, $a1  # a = b
li $t0, 10
b TEST  # test first
BODY:
addu $a0, $a0, $a1  # a = a + b
addiu $a1, $a1, 1  # b = b + 1
TEST:
bne $a1, $t0, BODY  # b != 10?
```
Arrays

```c
int a[5];

void main() {
    a[1] = a[0] = 3;
}
```

```assembly
.text
    .comm a, 20 # Allocate 20
    main:
        la $t0, a # Address of a
        li $t1, 3
        sw $t1, 0($t0) # a[0]
        sw $t1, 4($t0) # a[1]
        sw $t1, 8($t0) # a[2]
        sw $t1, 12($t0) # a[3]
        sw $t1, 16($t0) # a[4]
        lw $t1, 8($t0) # a[2]
        sll $t1, $t1, 2 # * 4
        sw $t1, 4($t0) # a[1]
        lw $t1, 16($t0) # a[4]
        sll $t1, $t1, 1 # * 2
        sw $t1, 12($t0) # a[3]
        jr $ra
```
Summing the contents of an array

```c
int i, s, a[10];
for (s = i = 0 ; i < 10 ; i++)
    s = s + a[i];
move $a1, $0 # i = 0
move $a0, $a1 # s = 0
li $t0, 10
la $t1, a # base address of array
b TEST
BODY:
sll $t3, $a1, 2 # i * 4
addu $t3, $t1, $t3 # &a[i]
lw $t3, 0($t3) # fetch a[i]
addu $a0, $a0, $t3 # s += a[i]
addiu $a1, $a1, 1
TEST:
sltu $t2, $a1, $t0 # i < 10?
bne $t2, $0, BODY
```
Summing the contents of an array

```c
int s, *i, a[10];
for (s=0, i = a+9 ; i >= a ; i--)
    s += *i;
```

```assembly
move $a0, $0       # s = 0
la     $t0, a     # &a[0]
addiu $t1, $t0, 36 # i = a + 9
b       TEST
BODY:      
lw     $t2, 0($t1) # *i
addu $a0, $a0, $t2 # s += *i
addiu $t1, $t1, -4 # i--
TEST:    
sltu $t2, $t1, $t0 # i < a
beq    $t2, $0, BODY
```
Strings: Hello World in SPIM

# For SPIM: "Enable Mapped I/O" must be set
# under Simulator/Settings/MIPS

.data
hello:
    .asciiz "Hello World!\n"

.text
main:
    la  $t1, 0xfffff0000  # I/O base address
    la  $t0, hello
wait:
    lw  $t2, 8($t1)      # Read Transmitter control
    andi $t2, $t2, 0x1   # Test ready bit
    beq  $t2, $0, wait
    lbu  $t2, 0($t0)     # Read the byte
    beq  $t2, $0, done   # Check for terminating 0
    sw  $t2, 12($t1)     # Write transmit data
    addiu $t0, $t0, 1    # Advance to next character
    b  wait
done:
    jr  $ra
Hello World in SPIM: Memory contents

```
[00400024] 3c09ffffff lui $9, -1
[00400028] 3c081001 lui $8, 4097 [hello]
[0040002c] 8d2a0008 lw $10, 8($9)
[00400030] 314a0001 andi $10, $10, 1
[00400034] 1140ffe e beq $10, $0, -8 [wait]
[00400038] 910a0000 lbu $10, 0($8)
[0040003c] 11400004 beq $10, $0, 16 [done]
[00400040] ad2a000c sw $10, 12($9)
[00400044] 25080001 addiu $8, $8, 1
[00400048] 0401fff9 bgez $0 -28 [wait]
[0040004c] 03e00008 jr $31

[10010000] 6c6c6548 6f57206f Hello Wo
[10010008] 21646c72 0000000a rld!
```
<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0:</td>
<td>NUL</td>
<td>P</td>
<td>P</td>
<td>P</td>
<td>P</td>
<td>P</td>
<td>P</td>
<td>P</td>
</tr>
<tr>
<td>1:</td>
<td>SOH</td>
<td>A</td>
<td>Q</td>
<td>a</td>
<td>q</td>
<td>q</td>
<td>q</td>
<td>q</td>
</tr>
<tr>
<td>2:</td>
<td>STX</td>
<td>B</td>
<td>R</td>
<td>b</td>
<td>r</td>
<td>r</td>
<td>r</td>
<td>r</td>
</tr>
<tr>
<td>3:</td>
<td>ETX</td>
<td>C</td>
<td>S</td>
<td>c</td>
<td>s</td>
<td>s</td>
<td>s</td>
<td>s</td>
</tr>
<tr>
<td>4:</td>
<td>EOT</td>
<td>D</td>
<td>T</td>
<td>d</td>
<td>t</td>
<td>t</td>
<td>t</td>
<td>t</td>
</tr>
<tr>
<td>5:</td>
<td>ENQ</td>
<td>E</td>
<td>U</td>
<td>e</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
</tr>
<tr>
<td>6:</td>
<td>ACK</td>
<td>F</td>
<td>V</td>
<td>f</td>
<td>v</td>
<td>v</td>
<td>v</td>
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</tbody>
</table>
Subroutines

a.k.a. procedures, functions, methods, et al.
Code that can run by itself, then *resume whatever invoked it*.

Exist for three reasons:

- **Code reuse**
  Recurring computations aside from loops
  Function libraries

- **Isolation/Abstraction**
  Think Vegas:
  What happens in a function stays in the function.

- **Enabling Recursion**
  Fundamental to divide-and-conquer algorithms
Calling Conventions

# Call mysub: args in $a0,...,$a3
jal mysub
# Control returns here
# Return value in $v0 & $v1
# $s0,...,$s7, $gp, $sp, $fp, $ra unchanged
# $a0,...,$a3, $t0,...,$t9 possibly clobbered

mysub:  # Entry point: $ra holds return address
# First four args in $a0, $a1, .., $a3

# ... body of the subroutine ...

# $v0, and possibly $v1, hold the result
# $s0,...,$s7 restored to value on entry
# $gp, $sp, $fp, and $ra also restored
jr $ra  # Return to the caller
The Stack

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>0x7FFFFFFFC</td>
<td>0x32640128</td>
</tr>
<tr>
<td>0x7FFFFFF8</td>
<td>0xCAFE0B0E</td>
</tr>
<tr>
<td>0x7FFFFFF4</td>
<td>0xDEADBEEF</td>
</tr>
<tr>
<td>0x7FFFFFF0</td>
<td>0xCODEFACE</td>
</tr>
<tr>
<td>0x7FFFFFFEC</td>
<td></td>
</tr>
</tbody>
</table>

$sp$ grows down
void move(int src, int tmp, int dst, int n)
{
    if (n) {
        move(src, dst, tmp, n-1);
        printf("%d->%d\n", src, dst);
        move(tmp, src, dst, n-1);
    }
}
hmove:
  addiu $sp, $sp, -24
  beq $a3, $0, L1
  sw $ra, 0($sp)
  sw $s0, 4($sp)
  sw $s1, 8($sp)
  sw $s2, 12($sp)
  sw $s3, 16($sp)

Allocate 24 stack bytes:
multiple of 8 for alignment

Check whether n == 0

Save $ra, $s0, ..., $s3 on the stack
hmove:
  addiu $sp, $sp, -24
  beq $a3, $0, L1
  sw $ra, 0($sp)
  sw $s0, 4($sp)
  sw $s1, 8($sp)
  sw $s2, 12($sp)
  sw $s3, 16($sp)

move $s0, $a0
move $s1, $a1
move $s2, $a2
addiu $s3, $a3, -1

Save src in $s0
Save tmp in $s1
Save dst in $s2
Save n – 1 in $s3
hmove:
  addiu $sp, $sp, -24
  beq $a3, $0, L1
  sw $ra, 0($sp)
  sw $s0, 4($sp)
  sw $s1, 8($sp)
  sw $s2, 12($sp)
  sw $s3, 16($sp)
  move $s0, $a0
  move $s1, $a1
  move $s2, $a2
  addiu $s3, $a3, -1
  move $a1, $s2
  move $a2, $s1
  move $a3, $s3
  jal hmove

Call
hmove(src, dst, tmp, n-1)
hmove:
  addiu $sp, $sp, -24
  beq $a3, $0, L1
  sw $ra, 0($sp)
  sw $s0, 4($sp)
  sw $s1, 8($sp)
  sw $s2, 12($sp)
  sw $s3, 16($sp)
  move $s0, $a0
  move $s1, $a1
  move $s2, $a2
  addiu $s3, $a3, -1
  move $a1, $s2
  move $a2, $s1
  move $a3, $s3
  jal hmove
  li $v0, 1 # print_int
  move $a0, $s2
  syscall
  li $v0,4 # print_str
  la $a0, newline
  syscall

Print src -> dst
hmove:
  addiu $sp, $sp, -24
  beq $a3, $0, L1
  sw $ra, 0($sp)
  sw $s0, 4($sp)
  sw $s1, 8($sp)
  sw $s2, 12($sp)
  sw $s3, 16($sp)
  move $s0, $a0
  move $s1, $a1
  move $s2, $a2
  addiu $s3, $a3, -1
  move $a1, $s2
  move $a2, $s1
  move $a3, $s3
  jal hmove

li $v0, 1 # print_int
move $a0, $s2
syscall
li $v0,4 # print_str
la $a0, newline
syscall
move $a0, $s1
move $a1, $s0
move $a2, $s2
move $a3, $s3
jal hmove

Call
hmove(tmp, src, dst, n-1)
hmove:
  addiu $sp, $sp, -24
  beq $a3, $0, L1
  sw $ra, 0($sp)
  sw $s0, 4($sp)
  sw $s1, 8($sp)
  sw $s2, 12($sp)
  sw $s3, 16($sp)
  move $s0, $a0
  move $s1, $a1
  move $s2, $a2
  addiu $s3, $a3, -1
  move $a1, $s2
  move $a2, $s1
  move $a3, $s3
  jal hmove
li $v0, 1 # print_int
move $a0, $s2
syscall
li $v0, 4 # print_str
la $a0, newline
syscall
move $a0, $s1
move $a1, $s0
move $a2, $s2
move $a3, $s3
jal hmove
lw $ra, 0($sp)
lw $s0, 4($sp)
lw $s1, 8($sp)
lw $s2, 12($sp)
lw $s3, 16($sp)

Restore variables
hmove:
    addiu $sp, $sp, -24
    beq $a3, $0, L1
    sw $ra, 0($sp)
    sw $s0, 4($sp)
    sw $s1, 8($sp)
    sw $s2, 12($sp)
    sw $s3, 16($sp)
    move $s0, $a0
    move $s1, $a1
    move $s2, $a2
    addiu $s3, $a3, -1
    move $a1, $s2
    move $a2, $s1
    move $a3, $s3
    jal hmove
    li $v0, 1  # print_int
    move $a0, $s2
    syscall
    li $v0, 4  # print_str
    la $a0, newline
    syscall
    move $a0, $s1
    move $a1, $s0
    move $a2, $s2
    move $a3, $s3
    jal hmove
    lw $ra, 0($sp)
    lw $s0, 4($sp)
    lw $s1, 8($sp)
    lw $s2, 12($sp)
    lw $s3, 16($sp)
L1:
    addiu $sp, $sp, 24  # free
    jr $ra  # return
.data
    li $v0, 1  # print_int
    move $a0, $s0
    syscall
    li $v0, 4  # print_str
    la $a0, arrow
    syscall
    arrow: .ascii "->"
    newline: .ascii "\n"
Factorial Example

```c
int fact(int n) {
    if (n < 1) return 1;
    else return (n * fact(n - 1));
}
```

fact:

```
addiu $sp, $sp, -8  # allocate 2 words on stack
sw $ra, 4($sp)    # save return address
sw $a0, 0($sp)    # and n
slti $t0, $a0, 1  # n < 1?
beq $t0, $0, ELSE
li $v0, 1         # Yes, return 1
addiu $sp, $sp, 8 # Pop 2 words from stack
jr $ra             # return

ELSE:
    addiu $a0, $a0, -1 # No: compute n-1
    jal fact          # recurse (result in $v0)
    lw $a0, 0($sp)    # Restore n and
    lw $ra, 4($sp)    # return address
    mul $v0, $a0, $v0 # Compute n * fact(n-1)
    addiu $sp, $sp, 8 # Pop 2 words from stack
    jr $ra            # return
```
Memory Layout

0x7FFF FFFC

Stack

0x1000 8000

Heap

0x1000 0000

Static Data

0x0040 0000

Program Text

0x0000 0000

Reserved

$sp

$gp

pc
Differences in Other ISAs

More or fewer general-purpose registers (E.g., Itanium: 128; 6502: 3)

Arithmetic instructions affect condition codes (e.g., zero, carry); conditional branches test these flags

Registers that are more specialized (E.g., x86)

More addressing modes (E.g., x86: 6; VAX: 20)

Arithmetic instructions that also access memory (E.g., x86; VAX)

Arithmetic instructions on other data types (E.g., bytes and halfwords)

Variable-length instructions (E.g., x86; ARM)

Predicated instructions (E.g., ARM, VLIW)

Single instructions that do much more (E.g., x86 string move, procedure entry/exit)