Memory

Prof. Stephen A. Edwards
sedwards@cs.columbia.edu

Columbia University
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Early Memories

Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.
Mercury acoustic delay line. Used in the EDASC, 1947. $32 \times 17$ bits
Early Memories

Magnetic core memory, 1952. IBM.
Early Memories

Magnetic drum memory. 1950s & 60s. Secondary storage.
## Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>$\infty$</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>$\infty$</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>$\infty$</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>$\infty$</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>$\infty$</td>
<td>64 ms</td>
</tr>
</tbody>
</table>
EPROMs
EEPROM and FLASH

- Slow write
  - Fowler-Nordheim Tunneling
  - EEPROM: bit at a time
  - FLASH: block at a time

Source: SST
Static RAM Cell

Word

Bit

\overline{\text{Bit}}
Standard SRAM: 6264

8K × 8

Can be very fast:
Cypress sells a 55ns version

Simple, asynchronous interface
Standard SRAM: 6264
Standard SRAM: 6264

The CY6264 is a high-performance CMOS RAM optimized for speed and power efficiency. It is characterized by:

- Low access time of 70 ns
- CMOS technology for optimum speed and power consumption
- Memory expansion capability
- Fully compatible inputs and outputs
- Power-down feature when deselected
- Automatic power-down feature reducing power by over 70% when deselected

An active low signal on the CE line controls the write operation. Reading the memory is accomplished by selecting the address and enabling the outputs. CE and WE inputs are active HIGH, while OE remains inactive or GND. In these conditions, the contents of the selected row are output on the pins (A0 to A7). The input/output pins remain high-impedance states when outputs are enabled, and when data is written into the memory.

The CY6264 is designed for high-performance applications requiring fast access times and low power consumption.
Toshiba TC55V16256J 256K × 16

12 or 15 ns access time
Asynchronous interface
UB, LB select bytes
Dynamic RAM Cell

Basic problem: Leakage

Solution: Refresh
Ancient DRAM: 4164

64K × 1
Apple IIe vintage

9,13,10–12,6,7,5

Addr[7:0]
DIN  DOUT
WE
CAS
RAS

Memory – p. 17
Basic DRAM read and write cycles
Page mode read cycle

RAS

CAS

Addr

WE

Din

Dout
Samsung 8M × 16 SDRAM

Synchronous interface
Designed for burst-mode operation
Four separate banks; pipelined operation
**SDRAM: Control Signals**

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write
SDRAM: Timing with 2-word bursts

- Clk
- RAS
- CAS
- WE
- Addr
- BA
- DQ