Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.
1. (10 pts.) Draw the circuit for a 2-to-4 decoder using AND gates and inverters.
   It should have two inputs \( X \) and \( Y \) and four outputs \( A \), \( B \), \( C \), and \( D \). Only one of the outputs should be true at one time.
2. (a) (10 pts.) Show how to implement an inverter using just a two-input mux (no additional gates).

(b) Show how your solution, when the mux2 is implemented as shown below, can be simplified into a single inverter.
3. (20 pts.) Consider the following circuit for a two-input mux.

(a) Under what conditions could the output of this circuit glitch low? I.e., for what assignment of input values would changing one input’s value cause the output to briefly transition from 1 to 0 to 1?

(b) Show how adding a two-input AND gate and widening the OR gate could eliminate this glitch.

(c) Draw the Karnaugh map corresponding to your new glitch-free circuit.
4. (15 pts.) Show how to implement \( F = XY + \overline{X} \overline{Y} Z + Y \overline{Z} \) using

(a) a 3-to-8 decoder and an OR gate;
(b) an 8 input mux; and
(c) a 4 input mux whose select inputs are \( X \) and \( Y \) and an inverter.
5. (10 pts.) Draw a circuit for an eight-input mux using seven two-input muxes and no other gates.
6. (20 pts.) Using AND, OR, and XOR gates only, draw the circuit for a three-bit two’s complement ripple carry adder with an overflow output. Your circuit should have six inputs (three bits for each addend) and four outputs (three results bits; one indicating overflow).
7. (15 pts.) Write the carry-out function in sum-of-products form for a five-bit binary adder in terms of

- $C_0$, the incoming carry;
- $G_0$ through $G_4$, the carry-generate signals for the five bits; and
- $P_0$ through $P_4$, the carry-propagate signals for the five bits.