Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.
Early Memories

Mercury acoustic delay line. Used in the EDASC, 1947. 32 \times 17 \text{ bits}
Early Memories

Magnetic core memory, 1952. IBM.
Early Memories

Magnetic drum memory. 1950s & 60s. Secondary storage.
# Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>∞</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>∞</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
<td>64 ms</td>
</tr>
</tbody>
</table>
ROMs

8 × 4 ROM

3×8 decoder

enable

A₀

A₁

A₂

word 0

word 1

word 2

word line

data line

programmable connection

wired-OR

Q₃

Q₂

Q₁

Q₀

Memory – p.
EPROMs
EEPROM and FLASH

- **Source**
- **Drain**
- **(bit line)**
- **Channel**
- **Word Line**
- **Floating gate**
- **Oxide**

### Slow write

Fowler-Nordheim Tunneling

EEPROM: bit at a time

FLASH: block at a time

Source: SST
Static RAM Cell
Standard SRAM: 6264

- Addr[12:0]: 10–2, 25–23, 21
- D[7:0]: 19–15, 13–11
- CS1: 20
- CS2: 26
- OE: 22
- WE: 27

8K × 8
Can be very fast:
Cypress sells a 55ns version
Simple, asynchronous interface
Standard SRAM: 6264

CS1

CS2

WE

OE

Addr

Data
Standard SRAM: 6264

The CY6264 is a high-performance CMOS RAM designed for memory expansion and ease of use. It features optimized speed and power consumption, compatible inputs and outputs, and an automatic power-down feature when deselected.

- **CMOS Technology**: Optimized for optimum speed and power efficiency.
- **Memory Expansion**: Capable of expanding memory systems.
- **Compatible Inputs and Outputs**: Ensures compatibility with standard interfaces.
- **Power-Down Feature**: Automatically reduces power consumption when deselected.

**Block Diagram**:

- **Row Decoder**: Activates the memory row based on address inputs.
- **Column Decoder**: Selects the memory column for read or write operations.
- **Input Buffer**: Prepares data for writing into the memory array.
- **Sense Amplifiers**: Enhance the data signals for accurate reading.
- **Power Down**: Enables automatic power reduction when not in use.

**Key Features**:

- **Access Time**: 70 ns
- **Compatibility**: Easy memory expansion
- **Power Consumption**: Low standby and active power consumption

The CY6264 is ideal for applications requiring high performance and low power, such as microprocessor systems and data acquisition systems.
Toshiba TC55V16256J 256K × 16

12 or 15 ns access time
Asynchronous interface
UB, LB select bytes
Toshiba TC55V16256J 256K × 16 Memory – p. 15
Dynamic RAM Cell

Basic problem: Leakage

Solution: Refresh
Ancient DRAM: 4164

64K × 1
Apple IIe vintage

9,13,10–12,6,7,5
2
3
15
4

Addr[7:0]
DIN   DOUT
WE
CAS
RAS
Basic DRAM read and write cycles
Page mode read cycle

- **RAS**
- **CAS**
- **Addr**
- **WE**
- **Din**
- **Dout**
Samsung 8M × 16 SDRAM

Synchronous interface
Designed for burst-mode operation
Four separate banks; pipelined operation
### SDRAM: Control Signals

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write
SDRAM: Timing with 2-word bursts

- **Clk**: Clock signal
- **RAS**: Row Address Strobe
- **CAS**: Column Address Strobe
- **WE**: Write Enable
- **Addr**: Address bus
- **BA**: Bank Address
- **DQ**: Data bus

**Operations**:
- **Load**: Load operation
- **Active**: Active operation
- **Write**: Write operation
- **Read**: Read operation
- **Refresh**: Refresh operation