Memory

Prof. Stephen A. Edwards
sedwards@cs.columbia.edu

Columbia University
Spring 2009
Early Memories

Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.
Early Memories

Mercury acoustic delay line. Used in the EDASC, 1947. 32 × 17 bits
Magnetic core memory, 1952. IBM.
Early Memories

Magnetic drum memory. 1950s & 60s. Secondary storage.
# Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>∞</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>∞</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>EEPROM</td>
<td>1000s, byte</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
<td>64 ms</td>
</tr>
</tbody>
</table>
ROMs
EPROMs
EEPROM and FLASH

Slow write
Fowler-Nordheim Tunneling

EEPROM: bit at a time
FLASH: block at a time

Source: SST
Static RAM Cell

Word

Bit

Bit
Standard SRAM: 6264

8K × 8

Can be very fast:
Cypress sells a 55ns version
Simple, asynchronous interface
Standard SRAM: 6264

- CS1
- CS2
- WE
- OE
- Addr
- Data
Standard SRAM: 6264

The CY6264 is a high-performance CMOS RAM optimized for speed and power efficiency. It features:
- 256 x 32 x 8 memory expansion capability
- Compatible inputs and outputs
- An active LOW enable (CE) and an active HIGH enable
- Low-power down feature when deselected

The device operates on a 3.3V power supply and has a maximum operating speed of 70 ns. It supports asynchronous memory expansion and has a power-down feature that reduces power consumption by over 70% when deselected.

The CY6264 is designed with advanced technology to provide high performance and reliability in memory applications.

[Diagram of CY6264 circuit]
Toshiba TC55V16256J 256K × 16

12 or 15 ns access time
Asynchronous interface
UB, LB select bytes
Dynamic RAM Cell

Basic problem: Leakage
Solution: Refresh
Ancient DRAM: 4164

64K \times 1
Apple IIe vintage

9,13,10–12,6,7,5

\begin{center}
\begin{tikzpicture}[node distance=1.5cm, auto]
  \node (addr) {Addr[7:0]};
  \node [below=of addr] (dout) {DOUT};
  \node [left=of dout] (din) {DIN};
  \node [below=of din] (we) {WE};
  \node [below=of we] (cas) {CAS};
  \node [below=of cas] (ras) {RAS};

  \draw [->] (addr) -- (dout);
  \draw [->] (addr) -- (din);
  \draw [->] (addr) -- (we);
  \draw [->] (addr) -- (cas);
  \draw [->] (addr) -- (ras);
\end{tikzpicture}
\end{center}
Basic DRAM read and write cycles
Page mode read cycle

- **RAS**
- **CAS**
- **Addr**: Row Col Col Col
- **WE**
- **Din**
- **Dout**
The Samsung 8M × 16 SDRAM is designed for burst-mode operation and has four separate banks, allowing for pipelined operation. The synchronous interface features the following signals:

- **BA[1:0]**: Bank address
- **Addr[11:0]**: Address (multiplexed)
- **DQ[15:0]**: Data I/O
- **UDQM**: Upper byte enable
- **LDQM**: Lower byte enable
- **WE**: Write enable
- **CAS**: Column Address Strobe
- **RAS**: Row Address Strobe
- **CKE**: Clock Enable
- **CLK**: Clock

The figure illustrates the pin layout and signal functions, emphasizing the importance of each in the operation of the SDRAM.
### SDRAM: Control Signals

<table>
<thead>
<tr>
<th>RAS</th>
<th>CAS</th>
<th>WE</th>
<th>action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>NOP</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Load mode register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Active (select row)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Read (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Write (select column, start burst)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Terminate Burst</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Precharge (deselect row)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Auto Refresh</td>
</tr>
</tbody>
</table>

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write
SDRAM: Timing with 2-word bursts