Early Memories

Williams Tube CRT-based random access memory, 1946. Used on the Manchester Mark I. 2048 bits.

Mercury acoustic delay line. Used in the EDASC, 1947. 32 × 17 bits.

Magnetic core memory, 1952. IBM.

Magnetic drum memory. 1950s & 60s. Secondary storage.

Early Memories

Modern Memory Choices

<table>
<thead>
<tr>
<th>Family</th>
<th>Programmed</th>
<th>Persistence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask ROM</td>
<td>at fabrication</td>
<td>∞</td>
</tr>
<tr>
<td>PROM</td>
<td>once</td>
<td>∞</td>
</tr>
<tr>
<td>EPROM</td>
<td>1000s, UV</td>
<td>10 years</td>
</tr>
<tr>
<td>FLASH</td>
<td>1000s, block</td>
<td>10 years</td>
</tr>
<tr>
<td>NVRAM</td>
<td>∞</td>
<td>5 years</td>
</tr>
<tr>
<td>SRAM</td>
<td>∞</td>
<td>while powered</td>
</tr>
<tr>
<td>DRAM</td>
<td>∞</td>
<td>64 ms</td>
</tr>
</tbody>
</table>

Armor Memory

EPROMs

EEPROM and FLASH

Slow write
Fowler-Nordheim Tunneling
EEPROM: bit at a time
FLASH: block at a time
Source: SST
**Static RAM Cell**

- Word
- Bit

**Standard SRAM: 6264**

- 19–15, 13–11
- 10–2, 25–23, 22
- Addr[12:0]
- D[7:0]
- 8K × 8

Can be very fast:
Cypress sells a 55ns version

Simple, asynchronous interface

**Toshiba TC55V16256J 256K × 16**

- 38–35, 32–29, 16–13, 10–7
- Addr[17:0]
- D[15:0]
- 12 or 15 ns access time

Asynchronous interface

UB, LB select bytes

**Dynamic RAM Cell**

- Row
- Column

Basic problem: Leakage

Solution: Refresh

**Ancient DRAM: 4164**

- 64K × 1
- Apple IIe vintage
- Addr[7:0]
- 9, 13, 10–12, 6, 7, 5
- DIN, DOUT
- WE
- CAS
- RAS

**Basic DRAM read and write cycles**

- RAS
- CAS
- Addr
- Row, Col
- WE
- Din
- Dout
Page mode read cycle

Samsung 8M × 16 SDRAM

21, 20 BA[1:0] Bank address
19 Addr[11:0] Address (multiplexed)
18 DQ[15:0] Data I/O
17 UDOM Upper byte enable
15 LDQM Lower byte enable
13 WE Write enable
12 Column Address Strobe
11 Row Address Strobe
10 Clock Enable
9 Clock

Synchronous interface
Designed for burst-mode operation
Four separate banks; pipelined operation

SDRAM: Control Signals

RAS | CAS | WE | action
---|---|---|---
1  | 1  | 1  | NOP
0  | 0  | 0  | Load mode register
0  | 1  | 1  | Active (select row)
1  | 0  | 1  | Read (select column, start burst)
1  | 0  | 0  | Write (select column, start burst)
1  | 1  | 0  | Terminate Burst
0  | 1  | 0  | Precharge (deselect row)
0  | 0  | 1  | Auto Refresh

Mode register: selects 1/2/4/8-word bursts, CAS latency, burst on write

SDRAM: Timing with 2-word bursts